HITACHI

Semiconductor

Description

high performance, cost-effective 32-bit RISC microprocessors with integrated peripheral functions optimized for embedded applications.

The SH-3 Series processors make an excellent choice for consumer, communication, data processing, industrial and transportation applications. These include digital cameras, protocol converters, cable modems, cellular phones, handheld PCs, Internet appliances, hard disk drives, industrial controllers, and auto PC. Designers can pair SH-3 processors with Hitachi or third party off-the-shelf companion chips or user-defined ASIC devices to design a low cost, low chip count, and differentiated system. All of these applications benefit from the SH-3 series:

- performance roadmap with CPU running from 60 MHz to 200 MHz
- small code size, low power dissipation and high performance/cost ratio
- highly integrated peripheral functions forming single-chip or two-chip solutions
- multiple vendor operating system support and multiple vendor development tool support

Hitachi and third parties provide a choice of first-class development tools to speed up system development. These include evaluation kits, emulators, companion chips, reference design platforms, software board support, real time operating system, middleware, and application packages.

SH-3 Series SuperH[®] RISC Processors



Support

Hardware:

• Emulators:

- Hitachi E10A emulator
- Wind River
- Yokagawa
- Sophia Systems
- Development and Reference boards
 - Hitachi HARP and Solution
 Engine with support for a wide range of RTOS
 - Densan

Software:

- Project Builders, C, C++ compilers, assemblers, simulator/debuggers
 - Hitachi
 - Redhat GNU
 - Green Hills Software
 - Microsoft® VC++ for Windows®CE
 - Diab SDS

Real-Time Operating System (RTOS):

- Microsoft (WindowsCE)
- Wind River (VxWorks)
- ATI (Nucleus+)
- QSSL (QNX/Neutrino)
- Microware (OS9)
- Lineo (Linux)
- CMX (CMX-RTX)

Others

Middleware:

- V.90/V.34 (up to 56 Kbps) Data/V.17 FAX software modem (Lucent)
- Speech Codec (for SH7729 only, Hitachi)
- Line Echo Canceller (for SH7729 only, Hitachi)
- Caller ID (for SH7729 only, Hitachi)

Companion chips: Hitachi (HD6446x Series)

- Each of the Hitachi HD6446x companion chips offers a CPU interface, timer, general purpose I/O, power management unit (PMU), and clock pulse generator with phase locked loop (CPG/PLL).
- Depending on the device, additional peripherals may include a graphics controller, PCMCIA controller, serial bus controllers, IrDA channel, analog front end (AFE) interfaces, interrupt controller, A/D converter, audio CODEC interface, parallel port, keyboard controller interface, PS/2 interface, universal serial bus (USB) controller, and JTAG boundary-scan test interface.
- Refer to the HD6446x Companion Chip Family product briefs for details.

Third-Party Vendors with SuperH Software Driver Support

- Graphic chips: IGS (Cyber Pro 5xxx Series), Integrated Technology Express (IT818x), Seiko Epsen (SED135x, SED137x)
- PCI: PLX Technology, V3 Semiconductor
- GPS: SiRF Technology





SH-3 HARP (Hardware Architecture Reference Platform) Block Diagram



Comparison Chart				
Feature	SH7706 (under development; available 4Q01)	SH7708R	SH7709S/SH7729R	;
СРU	Share the same Hitachi SH-3 CPU core; 32-bit RISC architecture with 16-bit fixed instruction length and five-stage pipeline; Load/store architecture with 16 32-bit general registers, 5 32-bit control registers, and 4 32-bit system register	Share the same Hitachi SH-3 CPU core; 32-bit RISC architecture with 16-bit fixed instruction length and five-stage pipeline; Load/store architecture with 16 32-bit general registers, 5 32-bit control registers, and 4 32-bit system register	Hitachi SH3-DSP core; 32-bit RISC architecture with 16-bit fixed instruction length and five-stage pipeline; Load/store architecture with 16 32-bit general registers, 5 32-bit control registers, and 4 32-bit system register	
ММU	4 Gbytes of address space, 256 address space; 1-KB or 4-KB page sizes; 128-entry, 4-way set associative TLB	4 Gbytes of address space, 256 address space; 1-KB or 4-KB page sizes; 128-entry, 4-way set associative TLB	4 Gbytes of address space, 256 address space; 1-KB or 4-KB page sizes- 128-entry, 4-way set associative TLB	4
Coprocessor or Unique Peripherals	Ν/Α	N/A	 DSP Full featured 16-bit integer DSP capability Extended Harvard Architecture with 2 data buses and 1 instruction bus 16-KB RAM as X/Y memory Instruction and data for RISC and DSP can share memories and cache with a single address space Max. four parallel operations: ALU, Multiply, and two Load or Store Large DSP data register file with 6 32-bit data registers and two 40-bit data registers One-cycle 16 x 16 multiply operations, two-cycle 16 x 16 + 64 MAC operations Supports zero overhead looping, circular addressing, and guard bits 	
CPU Speed	Up to 133 MHz; x1, x2, x3, x4, x6, x8, x12, x16 of input clock or crystal oscillator frequency for SH7709A	Up to 100 MHz; x1, x2, x4, or x8 of input clock or crystal oscillator frequency	Up to 200 MHz; x1, x2, x3, x4, x6, x8, x12, x16 of input clock or crystal oscillator frequency	l >
Bus Speed (max.)	Up to 66 MHz x1 or x4 of input clock or crystal oscillator frequency	Up to 60 MHz; x1, or x4 of input clock or crystal oscillator frequency	Up to 66 MHz; x1 or x4 of input clock or crystal oscillator frequency	ι
Power Supply Voltage (V)	3.0 to 3.6 for I/O and 1.75 to 2.05 for CPU core	3.15 to 3.6	3.0 to 3.6 for I/O and 1.75 to 2.05 for CPU core	3
Power Dissipation (mW)	330/446 (Normal Operation, typ.)116 (at 40 MHz)/130 (Sleep, typ.) 0.05/0.26 (Standby, typ.)	644 (max.)/396/396 (Normal Operation, typ.) 248 (Sleep, typ.) 0.05/3.3(max.)/3.3(max.) (Standby, typ.)	446 (Normal Operation, typ.) 130 (Sleep, typ.) 0.26 (Standby, typ.)	6
Cache	Mixed instruction/data; 16 KB size; Write-back, write-through, LRU replacement algorithm support; 256 entries, 16-byte block length, 4-way set associative, and Way 2 and Way 3 are lockable	Mixed instruction/data; 8 KB size; Write-back, write-through, LRU replacement algorithm support; 128 entries, 16-byte block length, 4-way or 2-way set associative; Can be divided so half can be used as the internal RAM	Mixed instruction/data; 16 KB size; Write-back, write-through, LRU replacement algorithm support; 256 entries, 16-byte block length, 4-way set associative, and Way 2 and Way 3 are lockable	
Memory Interface	External memory interface can be either 8-bit, 16-bit, or 32-bit (16-bit or 32-bit only for SDRAM interface); Supports both big- or little-endian; Direct interface with DRAM, SRAM, SDRAM, and Burst ROM	External memory interface can be either 8-bit, 16-bit, or 32-bit (32-bit only for SDRAM interface); Supports both big- or little-endian; Direct interface with DRAM, SRAM, SDRAM, Burst ROM, and PSRAM	External memory interface can be either 8-bit, 16-bit, or 32-bit (16-bit or 32-bit only for SDRAM interface); Supports both big- or little-endian; Direct interface with DRAM, SRAM, SDRAM, and Burst ROM	E (3
General Purpose I/O	12 8-bit ports; Multiplexed with other pin functions	One 8-bit port; Multiplexed with other pin functions	12 8-bit ports; Multiplexed with other pin functions	•
Interrupt Controller	7 external interrupt pins; Noise canceler NMI; 16 levels of interrupt priority	5 external interrupt pins; Noise canceler NMI; 16 levels of interrupt priority	7 external interrupt pins; Noise canceler NMI; 16 levels of interrupt priority	1
Timer	3-channel auto-reload type 32-bit timer; Input capture function; 6 types of counter input clocks can be selected; 2 MHz max. resolution	3-channel auto-reload type 32-bit timer; Input capture function; 6 types of counter input clocks can be selected; 2 MHz max. resolution	3-channel auto-reload type 32-bit timer; Input capture function; 6 types of counter input clocks can be selected; 2 MHz max. resolution	(
Watchdog Timer	Choice of internal resets or interrupts for watchdog counter overflow; 9 kinds of watchdog counter clocks	Choice of internal resets or interrupts for watchdog counter overflow; 9 kinds of watchdog counter clocks	Choice of internal resets or interrupts for watchdog counter overflow; 9 kinds of watchdog counter clocks	(
Real-time Clock	BCD display of second, minutes, hours, date, day of the week, month, and year; 1-Hz to 64-Hz timer (binary display); Automatic leap year correction; Year counter range is 00 to 99 only	BCD display of second, minutes, hours, date, day of the week, month, and year; 1-Hz to 64-Hz timer (binary display); Automatic leap year correction; Year counter range is 00 to 99 only	BCD display of second, minutes, hours, date, day of the week, month, and year; 1-Hz to 64-Hz timer (binary display); Automatic leap year correction; Year counter range is 00 to 99 only	
Serial Communication Interface	 2 serial channels Channel 0 supports smart card interface, conforms to the ISO/IEC standard 7816-3 Channel 1 has 16-byte FIFO and DMA capability; IrDA interface based on the IrDA 1.0 system 	1 serial channel: Supports smart card interface, conforms to the ISO/IEC standard 7816-3; Selection of async. or synchronous mode; Full-duplex communication	 3 serial channels Channel 0 supports smart card interface, conforms to the ISO/IEC standard 7816-3 Channel 1 has 16-byte FIFO and DMA capability; IrDA interface based on the IrDA 1.0 system Channel 2 has 16-byte FIFO and DMA capability; hardware flow control; Selection of async. or synchronous mode; Full-duplex communication 	
A/D Converter	4 channels, 10 bits \pm 4 LSB; 10- μs conversion time; Input range: 0nVcc (max. 3.6 V)	N/A	8 channels, 10 bits ± 4 LSB; 10-µs conversion time; Input range: 0-Vcc (max. 3.6 V)	8
D/A Converter	2 channels, 10 bits \pm 4 LSB; 10- μs conversion time; Output range: 0nVcc (max. 3.6 V)Output range: 0-Vcc (max. 3.6 V)	N/A	2 channels, 10 bits \pm 4 LSB; 10- μ s conversion time; Output range: 0-Vcc (max. 3.6 V)	2
DMA Controller	4 channels; Selectable bus access: burst mode or cycle-steal mode; Dual address mode is supported; Transfer data width: 1/2/4/16 bytes Selectable channel priority levels: fixed mode or round-robin mode	N/A	4 channels; Selectable bus access: burst mode or cycle-steal mode; Dual address mode is supported; Transfer data width: 1/2/4/16 byte(s); Selectable channel priority levels: fixed mode or round-robin mode	2
Serial Debug Interface	JTAG standard pinout; Real time branch address trace; 1-KB on-chip RAM for fast emulation program execution; E-10A emulator support	N/A	JTAG standard pinout; Real time branch address trace; 1-KB on-chip RAM for fast emulation program execution; E-10A emulator support	

SH7727 (under development; available 4Q01)
Hitachi SH3-DSP core; 32-bit RISC architecture with 16-bit fixed instruction length and five-stage pipeline; Load/store architecture with 16 32-bit general registers, 5 32-bit control registers, and 4 32-bit system register
4 GB of address space, 256 address space; 1-KB or 4-KB page sizes; 128-entry, 4-way set associative TLB
LCD Controller • up to 640 x 480 VGA resolution, 16-bit color, TFT/DSTN/STN • USB host and function controller • Analog front end for software modem • Conforms to PCMCIA release 2.1/JEIDA ver. 4.2 ï 2 slot support (32 MB per slot) • DSP core (see SH7729R section)
Up to 160 MHz; x1, x2, x4, or x8 of input clock or crystal oscillator frequency
Up to 40 MHz; x1/2, x1 or x4 of input clock or crystal oscillator frequency
3.0 to 3.6 for I/O and 1.75 to 2.05 for CPU core
644 (max.) (Normal Operation, typ.) 248 (Sleep, typ.) 0.05 (Standby, typ.)
Mixed instruction/data; 16 KB size; Write-back, write-through, LRU replacement algorithm support; 256 entries, 16-byte block length, 4-way set associative, and Way 2 and Way 3 are lockable
External memory interface can be either 8-bit, 16-bit, or 32-bit (16-bit or 32-bit only for SDRAM interface); Supports both big- or little-endian; Direct interface with DRAM, SRAM, SDRAM, and Burst ROM
13 8-bit ports; Multiplexed with other pin functions
11 external interrupt pins; Noise canceler NMI; 16 levels of interrupt priority
3-channel auto-reload type 32-bit timer; Input capture function; 6 types of counter input clocks can be selected; 2 MHz max. resolution
Choice of internal resets or interrupts for watchdog counter overflow; 9 kinds of watchdog counter clocks
BCD display of second, minutes, hours, date, day of the week, month, and year; 1-Hz to 64-Hz timer (binary display); Automatic leap year correction; Year counter range is 00 to 99 only
 3 serial channels: Channel 0 supports smart card interface, conforms to the ISO/IEC standard 7816-3 Channel 1 has 16-byte FIFO and DMA capability; IrDA interface based on the IrDA 1.0 system Channel 2 has 16-byte FIFO and DMA capability; hardware flow control; Selection of async. or synchronous mode; Full-duplex communication
8 channels, 10 bits \pm 4 LSB; 10- μ s conversion time; Input range: 0-Vcc (max. 3.6 V)
2 channels, 10 bits ± 4 LSB; 10-µs conversion time; Output range: 0-Vcc (max. 3.6 V)
4 channels; Selectable bus access: burst mode or cycle-steal mode; Dual address mode is supported; Transfer data width: 1/2/4 byte(s); Selectable channel priority levels: fixed mode or round-robin mode
JTAG standard pinout; Real time branch address trace; 1-KB on-chip RAM for fast emulation program execution; E-10A emulator support



Ordering Information

Device	Package	Chip Order No.	CPU Speed (Max.)
SH7706	FP-176	HD6417706F133	133MHz
SH7706	TBP-208AV	HD6417706BP133V	133MHz
SH7708	FP-144F	HD6417708RF100A	100MHz
SH7708	FP-144F	HD6417708SF60	60MHz
SH7708	FP-144F	HD6417708SF60I	60MHz
SH7727	FP-240B	HD6417727F100	100MHz
SH7727	BP-240AV	HD6417727BP100V	100MHz
SH7727	FP-240B	HD6417727F160	160MHz
SH7727	BP-240AV	HD6417727BP160V	160MHz
SH7709S	BP-240AV	HD6417709SBP100V	100MHz
SH7709S	BP-240AV	HD6417709SBP133V	133MHz
SH7709S	BP-240AV	HD6417709SBP167V	167MHz
SH7709S	FP-208C	HD6417709SF100	100MHz
SH7709S	FP-208C	HD6417709SF133	133MHz
SH7709S	FP-208C	HD6417709SF167	167MHz
SH7709S	FP-208E	HD6417709SHF200	200MHz
SH7729R	BP-240AV	HD6417729RBP100V	100MHz
SH7729R	BP-240AV	HD6417729RBP133V	133MHz
SH7729R	BP-240AV	HD6417729RBP167V	167MHz
SH7729R	FP-208C	HD6417729RF100	100MHz
SH7729R	FP-208C	HD6417729RF133	133MHz
SH7729R	FP-208C	HD6417729RF167	167MHz
SH7729R	FP-208E	HD6417729RHF200	200MHz

Quad Flat Package (QFP)





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Distributors

Dimensions (in mm)

Symbol	FP-144	FP-176	FP-208C	FP-208E	FP-240B	TBP-208AV	BP-240AV
Α	22	26	30	30.6	34.6	12	13
В	20	24	28	28	32	10.4	11.7
С	22	26	30	30.6	34.6	12	13
D	20	24	28	28	32	10.4	11.7
E	0.2	0.2	0.2	0.2	0.2	0.65	0.65
F	1.7	1.7	1.7	3.56	3.95	1.2	1.4

Note: tolerances not shown

Contacts

U.S. Headquarters

179 East Tasman Drive, San Jose, CA 95134 www.hitachi.com/semiconductor To order literature: (800) 285-1601 Fax: (510) 683-9700

Regional/District Sales Offices

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(, , , , , , , , , , , , , , , , , , ,	(313) 271-4410	(919) 233-0800	()11)0))0000	(010) 091 1990
8885 Rio San Diego Dr.	· · ·	(),		Calgary
Suite 310	500 Park Boulevard, Suite 415			10655 Southport Road SW. Suite
San Diego, CA 92108	Itasca, IL 60143			Calgary, Alberta T2W 4Y1
(619) 299-6873	(630) 773-4864			(402) 279 1991
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