ft690

2W Mono BTL Audio Power Amplifier

General Description

The ft690 is an audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1.25 watts of continuous average power to an 8Ω BTL load and 2 watts of continuous average power (DFN only) to a 4Ω BTL load with less than 1% distortion (THD+N+N) from a 5VDC power supply.

The ft690 was designed specifically to provide high quality output power with a minimal amount of external components. The ft690 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The ft690 features a low-power consumption shutdown mode. To facilitate this, Shutdown may be enabled by either logic high or low depending on mode selection. Driving the shutdown mode pin either high or low enables the shutdown pin to be driven in a likewise manner to enable shutdown.

The ft690 contains advanced pop & click circuitry which eliminates noise which would otherwise occur during turn-on and turn-off transitions.

The ft690 is unity-gain stable and can be configured by external gain-setting resistors.

Key Specifications

- Improved PSRR at 217Hz & 1KHz 66dB
- Power Output at 5.0V, 1% THD+N, 4Ω (QFN only) 2W (typ)
- Power Output at 5.0V, 1% THD+N, 8Ω 1.25W (typ)
- Power Output at 3.0V, 1% THD+N, 4Ω 600mW (typ)
- Power Output at 3.0V, 1% THD+N, 8Ω 425mW (typ)
- Shutdown Current 0.1μA (typ)

Features

- Available in space-saving packages: DFN, MSOP, WCSP
- Ultra low current shutdown mode
- Improved pop & click circuitry eliminates noise during turn-on and turn-off transitions
- 2.2 - 5.5V operation
- No output coupling capacitors, snubber networks or bootstrap capacitors required
- Unity-gain stable
- External gain configuration capability
- User selectable shutdown High or Low logic Level

Applications

- Mobile Phones
- PDAs
- Portable electronic device

Application Circuit

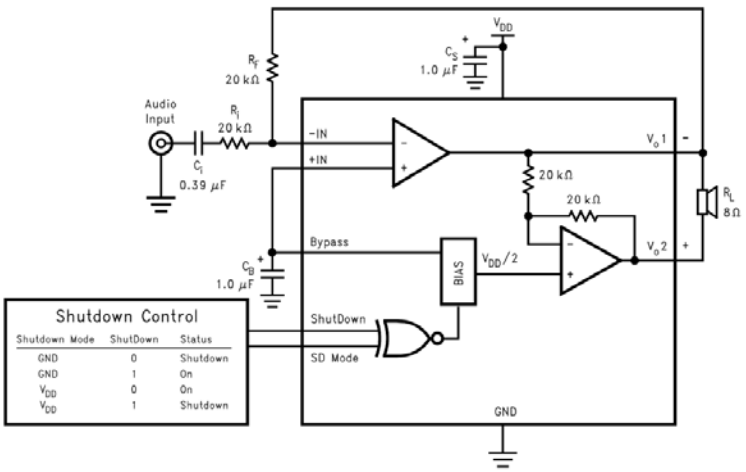


Figure 1.Typical Audio Amplifier Application Circuit (DFN)

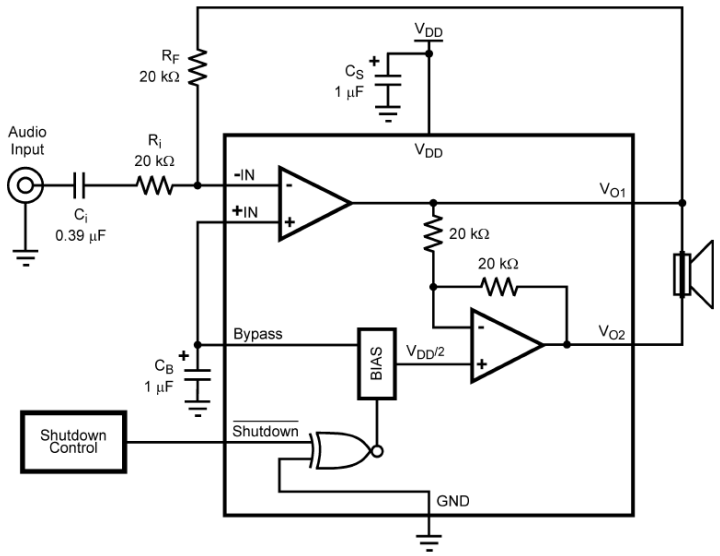


Figure 2.Typical Audio Amplifier Application Circuit (MSOP and WCSP)

ORDERING INFORMATION

P/N	TEMP RANGE	PIN-PACKAGE	GAIN(dB)
ft690D	-40°C to +85°C	10pin DFN	Adj.
ft690M	-40°C to +85°C	8pin MSOP	Adj.
Ft690W	-40°C to +85°C	9pin WCSP	Adj.

Ordering Information continued at end of data sheet.
Pin Configurations and Selector Guide appear at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

	Unit
Supply voltage, VDD	6.0 V
Storage Temperature	−65°C to +150°C
Input Voltage	−0.3V to VDD +0.3V
Power Dissipation	Internally Limited
ESD Susceptibility	2000V
Junction Temperature	150°C
θ_{JC} (MSOP)	56°C/W
θ_{JA} (MSOP)	190°C/W
θ_{JC} (WCSP)	180°C/W
θ_{JA} (DFN)	63°C/W
θ_{JC} (DFN)	12°C/W
Lead temperature 1,6 mm (1/16 Inch) from case for 10 seconds	260°C

RECOMMENDED OPERATING CONDITIONS

		MIN	YP	MAX	UNIT
Supply voltage, VDD		2.5		5.5	V
High-level input voltage, VIH	$\overline{\text{SHUTDOWN}}$	2			V
Low-level input voltage, VIL	$\overline{\text{SHUTDOWN}}$			0.8	V
Common-mode input voltage, VIC	VDD = 2.5 V, 5.5 V, CMRR ≤ -60 dB	0.5		VDD-0.8	V
Operating free-air temperature, TA		-40		85	°C
Load impedance, ZL		6.4		8	Ω

ELECTRICAL CHARACTERISTICS

V_{DD}=5V T_A=25°C

Symbol	Parameter	Conditions	Typical	Limit	Units(Limits)
I_{DD}	Quiescent Power Supply Current	V_{IN}=0V, I_O=0A, No Load	2.5	7	mA (max)
		V_{IN}=0V, I_O=0A, 8 Ω Load	3	10	mA (max)
I_{SD}	Shutdown Current	V_{SD}= $V_{SD\ MODE}$ (WCSP only)	0.1	2.0	μA (max)
V_{SDIH}	Shutdown Voltage Input High	$V_{SD\ MODE}$ = V_{DD}	1.5		V
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD\ MODE}$ = V_{DD}	1.3		V
V_{SDIH}	Shutdown Voltage Input High	$V_{SD\ MODE}$ = GND	1.5		V
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD\ MODE}$ = GND	1.3		V
V_{OS}	Output Offset Voltage		7	50	mV (max)
R_{OUT}	Resistor Output to GND		8.5	9.7	K Ω (max)
				7.0	K Ω (min)
P_O	Output Power (8 Ω)	THD+N=1% (max); f=1kHz	1.25	0.9	W (min)
	(4Ω)	THD+N=1% (max); f=1kHz	2		W
T_{WU}	Wake-up time		130		Ms
THD+N	Total Harmonic Distortion+Noise	P_O = 0.5Wrms; f=1kHz	0.2		%
PSRR	Power Supply Rejection Ratio	V_{ripple}=200mV sine p-p Input terminated with 10 Ω	66(f=217Hz) 76(f=1kHz)	55	dB (min)

V_{DD}=3V T_A=25°C

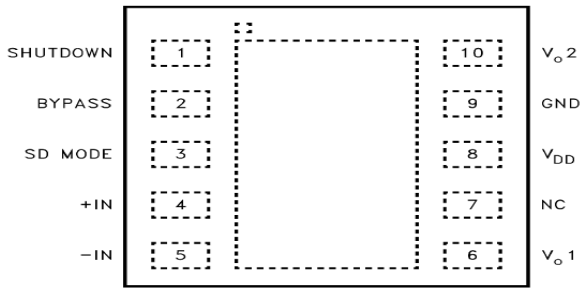
Symbol	Parameter	Conditions	Typical	Limit	Units(Limits)
I_{DD}	Quiescent Power Supply Current	V_{IN}=0V, I_O=0A, No Load	1.6	7	mA (max)
		V_{IN}=0V, I_O=0A, 8 Ω Load	2	9	mA (max)
I_{SD}	Shutdown Current	V_{SD}= $V_{SD\ MODE}$ (WCSP only)	0.1	2.0	μA (max)
V_{SDIH}	Shutdown Voltage Input High	$V_{SD\ MODE}$ = V_{DD}	1.1		V
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD\ MODE}$ = V_{DD}	0.9		V
V_{SDIH}	Shutdown Voltage Input High	$V_{SD\ MODE}$ = GND	1.3		V
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD\ MODE}$ = GND	1.0		V
V_{OS}	Output Offset Voltage		7	50	mV (max)
R_{OUT}	Resistor Output to GND		8.5	9.7	K Ω (max)
				7.0	K Ω (min)
P_O	Output Power (8 Ω)	THD+N=1% (max); f=1kHz	425		mW
	Output Power (4 Ω)	THD+N=1% (max); f=1kHz	600		mW
T_{WU}	Wake-up time		80		Ms
THD+N	Total Harmonic Distortion+Noise	P_O = 0.25Wrms; f=1kHz	0.1		%
PSRR	Power Supply Rejection Ratio	V_{ripple}=200mV sine p-p Input terminated with 10 Ω	66(f=217Hz) 76(f=1kHz)	55	dB (min)

V_{DD}=2.6V T_A=25°C

Symbol	Parameter	Conditions	Typical	Limit	Units(Limits)
I_{DD}	Quiescent Power Supply Current	V_{IN}=0V, I_O=0A, No Load	1.5		mA (max)
		V_{IN}=0V, I_O=0A, 8 Ω Load	2		mA (max)
I_{SD}	Shutdown Current	V_{SD}= $V_{SD\ MODE}$ (WCSP only)	0.1		μA (max)
V_{SDIH}	Shutdown Voltage Input High	$V_{SD\ MODE}$ = V_{DD}	1.0		V
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD\ MODE}$ = V_{DD}	0.9		V
V_{SDIH}	Shutdown Voltage Input High	$V_{SD\ MODE}$ = GND	1.2		V
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD\ MODE}$ = GND	1.0		V
V_{OS}	Output Offset Voltage		5	50	mV (max)
R_{OUT}	Resistor Output to GND		8.5	9.7	K Ω (max)
				7.0	K Ω (min)
P_O	Output Power (8 Ω)	THD+N=1% (max); f=1kHz	300		mW
	Output Power (4 Ω)	THD+N=1% (max); f=1kHz	400		mW
T_{WU}	Wake-up time		70		Ms
THD+N+N	Total Harmonic Distortion+Noise	P_O = 0.15Wrms; f=1kHz	0.1		%
PSRR	Power Supply Rejection Ratio	V_{ripple}=200mV sine p-p Input terminated with 10 Ω	66(f=217Hz) 76(f=1kHz)	55	dB (min)

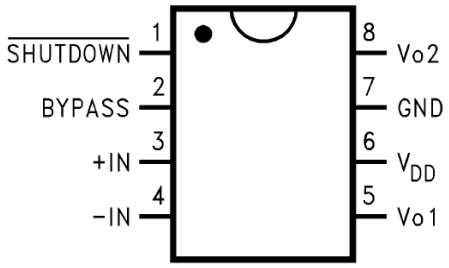
PIN DESCRIPTION

DFN Package



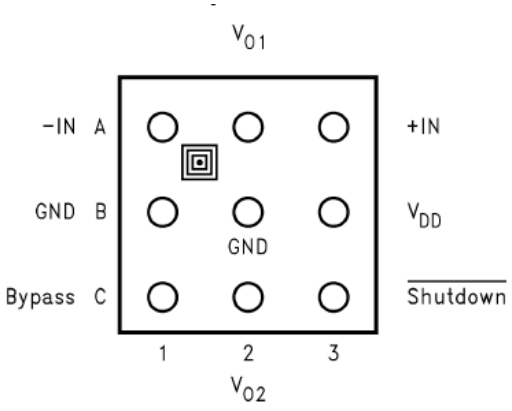
Top View
Order Number ft690D

MSOP Package



Top View
Order Number ft690M

WCSP Package



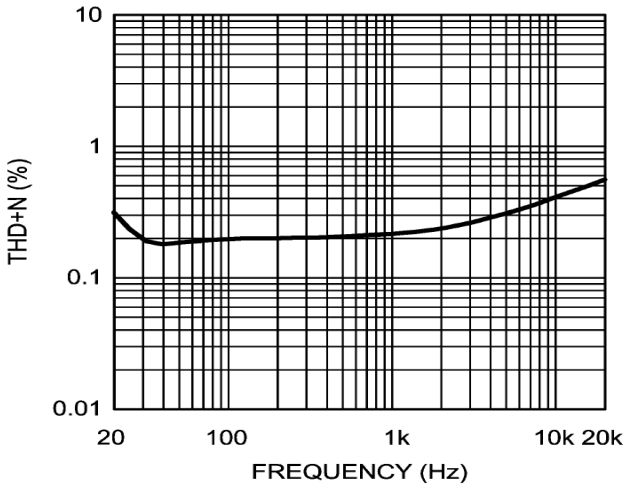
Top View
Order Number ft690W

Package	DFN	MSOP	WCSP
Shutdown Mode	Selectable	Low	Low
Typical Power Output at 5V, 1% THD+N	2W (R_L=4)	1.25W (R_L=8Ω)	1.25W (R_L=8)

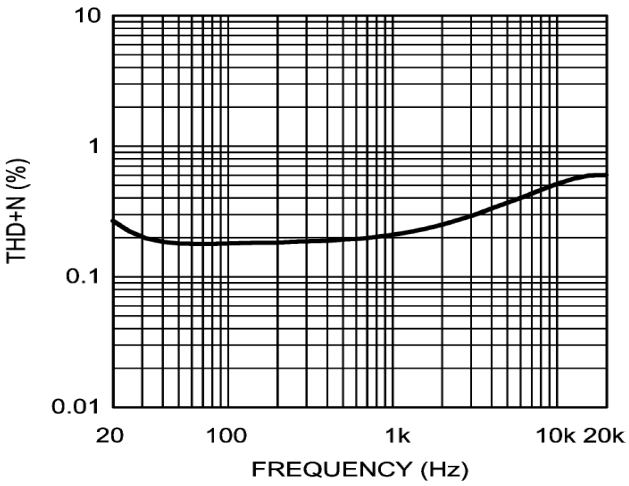
A SD_MODE select pin determines the Shutdown Mode for the DFN package, whether it is an Asserted High or an Asserted Low device, to activate shutdown.
The SD_MODE select pin is with the MSOP and WCSP packaged devices, shutdown occurs only with an low assertion.

Typical Performance Characteristics
LD and MH Specific Characteristics

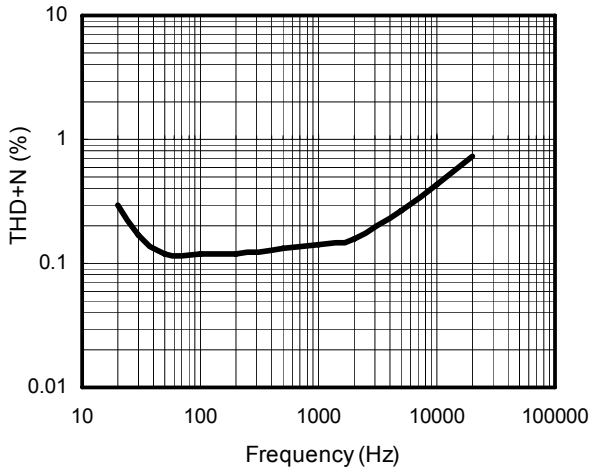
THD+N+N vs Frequency
V_{DD} = 5V, R_L = 4Ω, and P_O = 1W



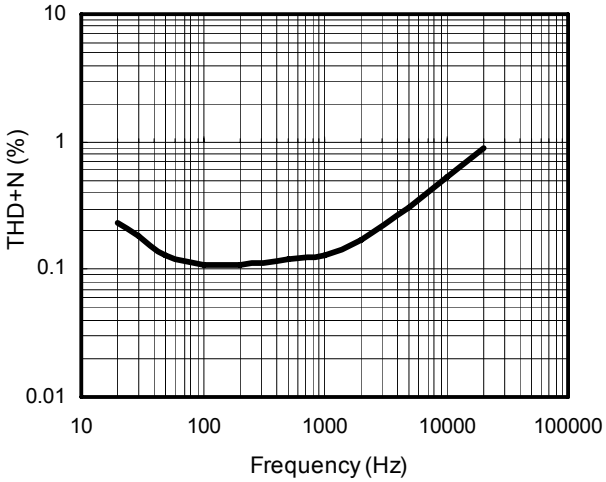
THD+N+N vs Frequency
V_{DD} = 3V, R_L = 4Ω, and P_O = 500mW



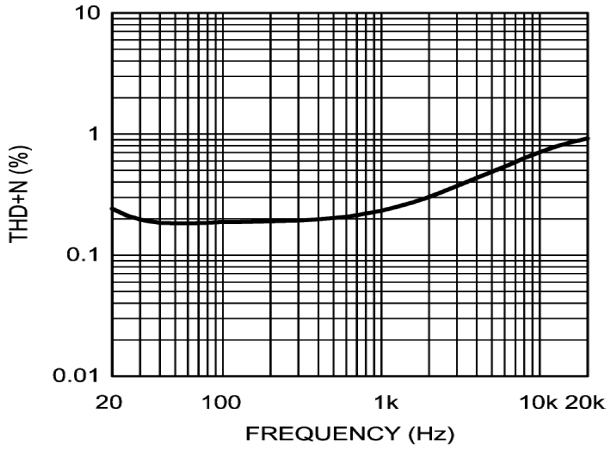
THD+N+N vs Frequency
Vdd=5V, RL=8 Ω , Po=0.5W



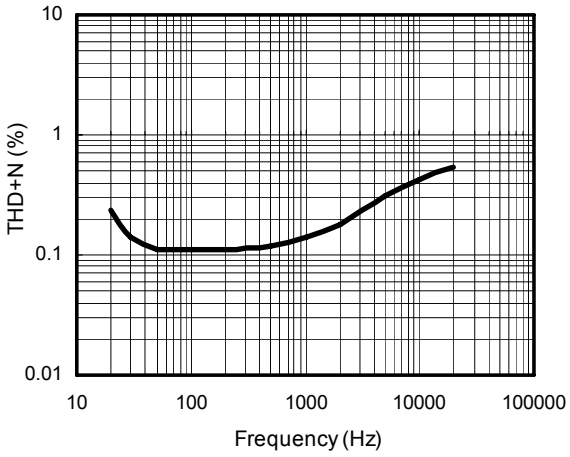
THD+N+N vs Frequency
Vdd=3V, RL=8 Ω , Po=0.25W



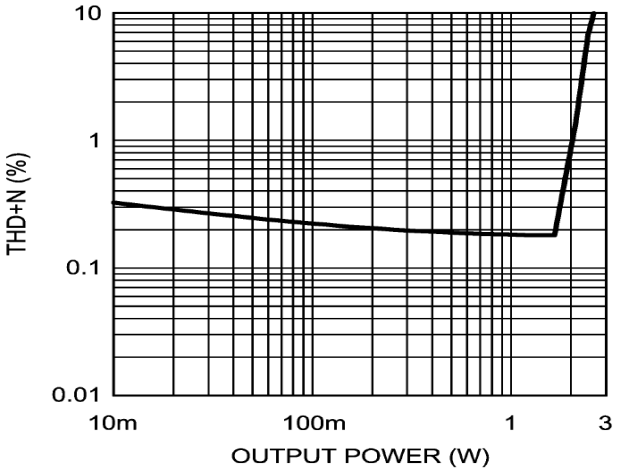
THD+N+N vs Frequency
V_{DD} = 2.6V, R_L = 4Ω, and P_O = 150mW



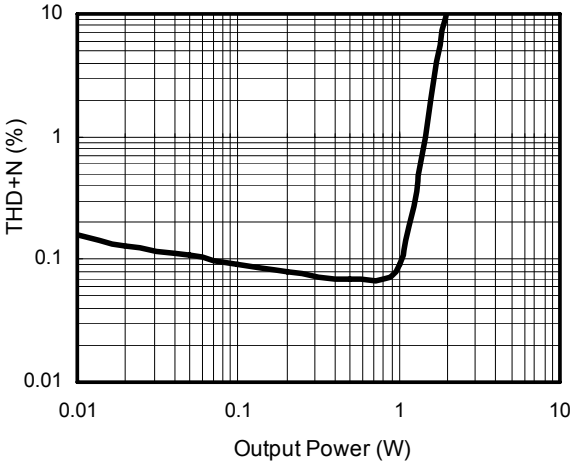
THD+N+N vs Frequency
Vdd=2.6V, RL=8 Ω , Po=0.15W



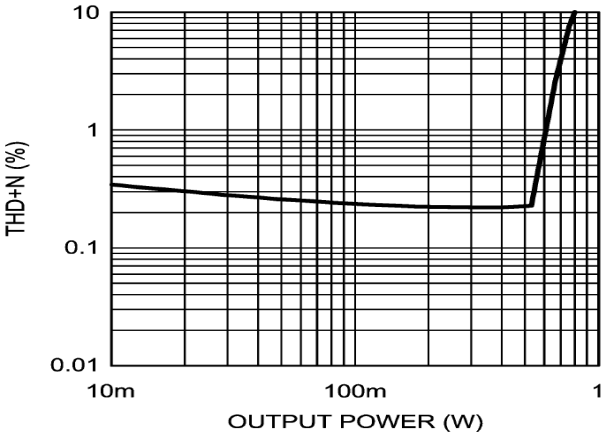
THD+N+N vs Output Power
V_{DD} = 5V, R_L = 4Ω, and f = 1 kHz



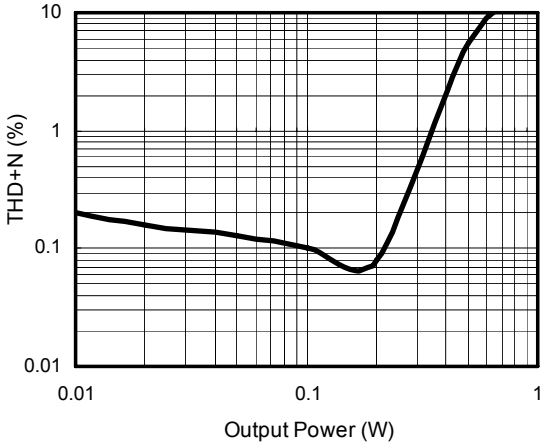
THD+N+N vs Output Power
Vdd=5V, RL=8 Ω , f=1KHz



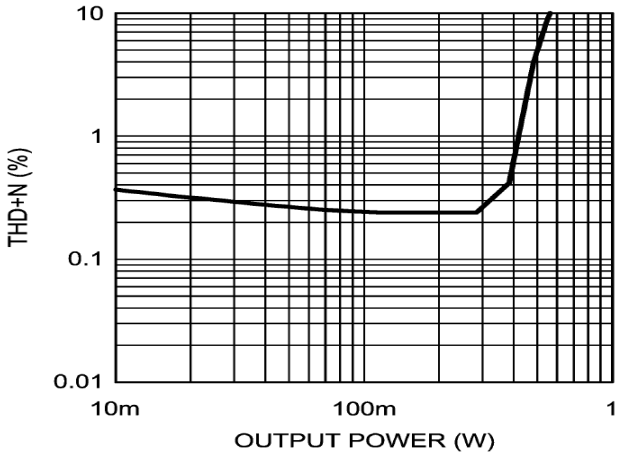
THD+N+N vs Output Power
V_{DD} = 3V, R_L = 4Ω, and f = 1kHz



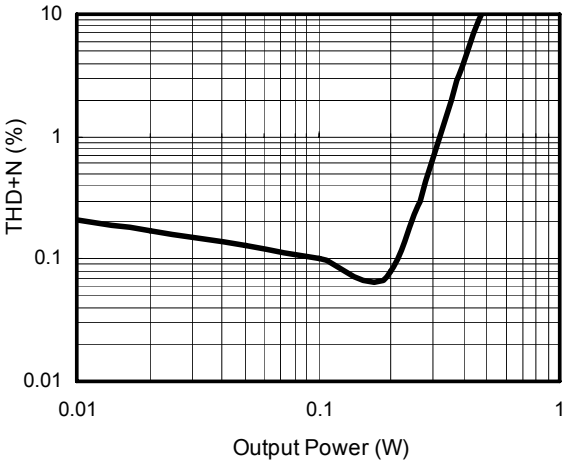
THD+N+N vs Output Power
Vdd=3V, RL=8 Ω , f=1KHz



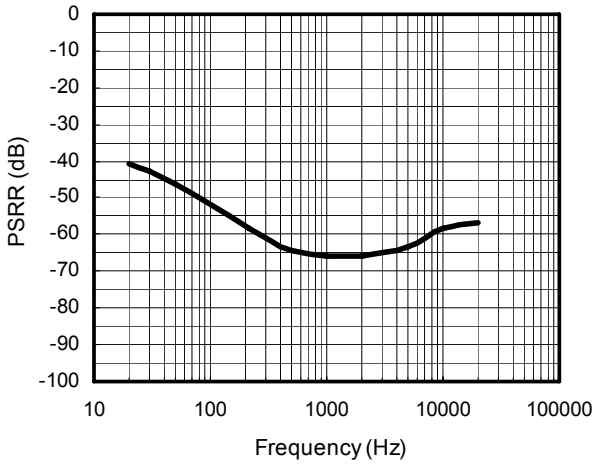
THD+N+N vs Output Power
V_{DD} = 2.6V, R_L = 4Ω, and f = 1kHz



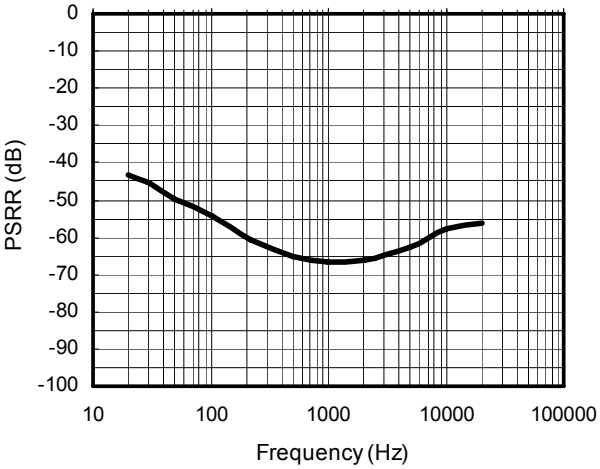
THD+N+N vs Output Power
Vdd=2.6V, RL=8 Ω , f=1KHz



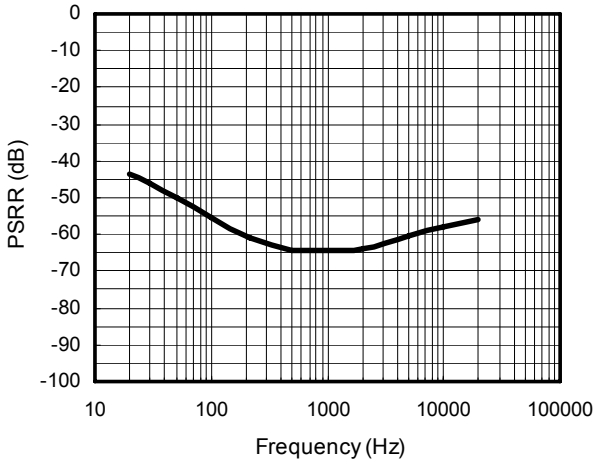
PSRR vs Frequency
Vdd=5V, RL=8 Ω , Input=10Ω



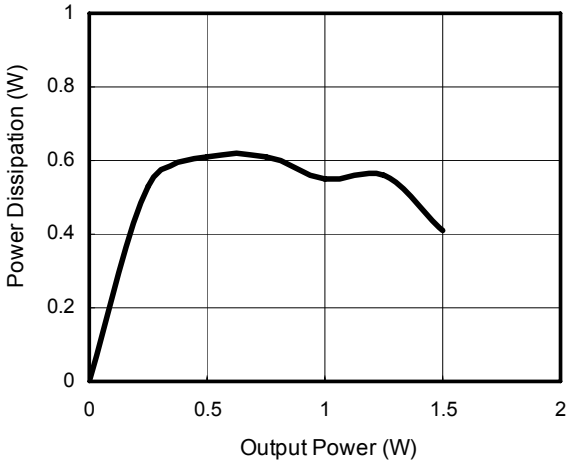
PSRR vs Frequency
Vdd=3V, RL=8 Ω , Input=10Ω



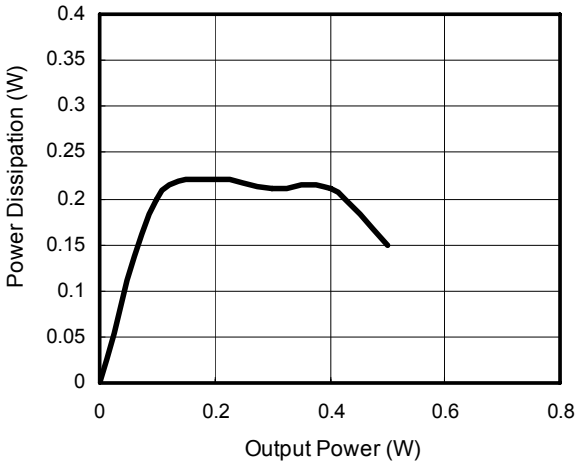
PSRR vs Frequency
Vdd=2.6V, RL=8 Ω , Input=10Ω



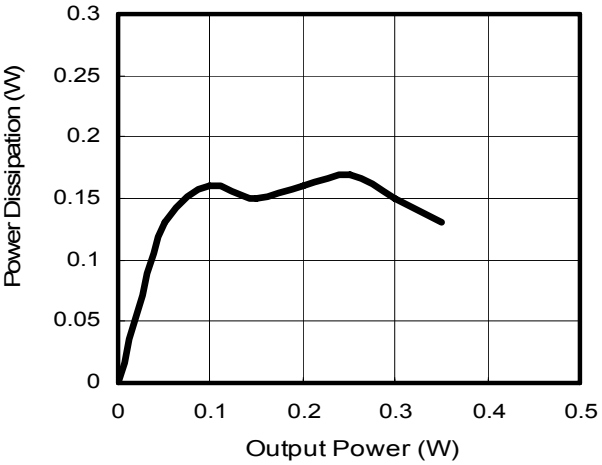
Power Dissipation vs Output Power
Vdd=5V, RL=8 Ω



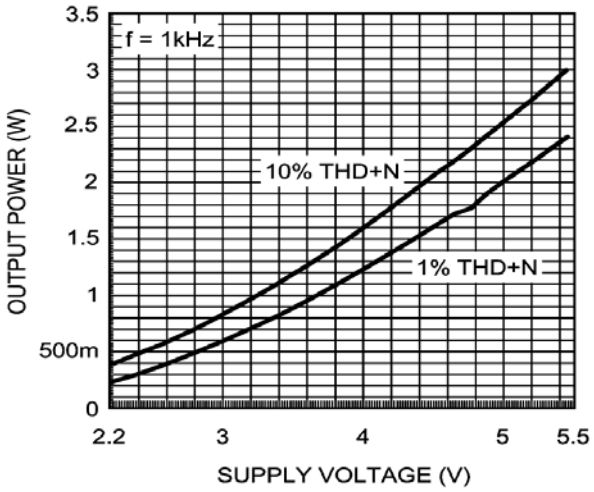
Power Dissipation vs Output Power
Vdd=3V, RL=8 Ω



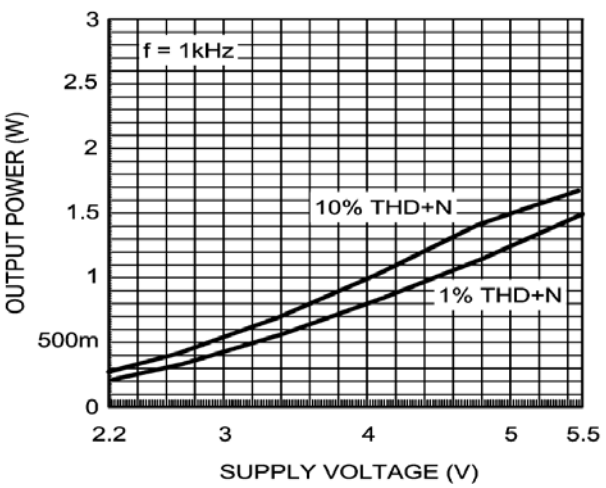
Power Dissipation vs Output Power
Vdd=2.6V, RL=8 Ω



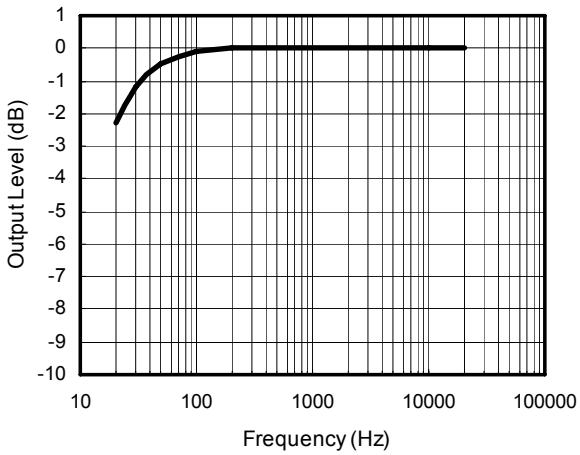
Output Power vs
Supply Voltage, R_L = 4Ω



Output Power vs
Supply Voltage, R_L = 8Ω



Frequency Response vs Input Capacitor Size
Vdd=5V, RL=8 Ω , Cap=0.44uF



Application Information

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 1, the ft690 has two internal operational amplifiers. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_f to R_i while the second amplifier's gain is fixed by the two internal 20kΩ resistors. Figure 1 shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180°. Consequently, the differential gain for the IC is

$$A_{VD} = 2 * (R_f/R_i)$$

By driving the load differentially through outputs Vo1 and Vo2, an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to **Audio Power Amplifier Design** section.

A bridge configuration, such as the one used in ft690, also creates a second advantage over single-ended amplifiers. Since the differential outputs, Vo1 and Vo2, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the ft690 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 1.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \quad (1)$$

It is critical that the maximum junction temperature T_{JMAX} of 150°C is not exceeded. T_{JMAX} can be determined from the power derating curves by using P_{DMAX} and the PC board foil area. By adding copper foil, the thermal resistance of the application can be reduced from the free air value of θ_{JA}, resulting in higher P_{DMAX} values without thermal shutdown protection circuitry being activated. Additional copper foil can be added to any of the leads connected to the ft690. It is especially effective when connected to V_{DD}, GND, and the output pins. Refer to the application information on the ft690 reference design board for an example of good heat sinking. If T_{JMAX} still exceeds 150°C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10μF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the ft690. The selection of a bypass capacitor, especially C_B, is dependent upon PSRR requirements, click and pop performance, system cost, and size constraints.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the ft690 contains shutdown circuitry that is used to turn off the amplifier's bias circuitry. In addition, the ft690 contains a Shutdown Mode pin (DFN only), allowing the designer to designate whether the part will be driven into shutdown with a high level logic signal or a low level logic signal. This allows the designer maximum flexibility in device use, as the Shutdown Mode pin may simply be tied permanently to either V_{DD} or GND to set the ft690 as either a "shutdown-high" device or a "shutdown-low" device, respectively. The device may then be placed into shutdown mode by toggling the Shutdown pin to the same state as the Shutdown Mode pin. For simplicity's sake, this is called "shutdown same", as the ft690 enters shutdown mode whenever the two pins are in the same logic state. The MSOP package lacks this Shutdown Mode feature, and is permanently fixed as a 'Shutdown-low' device. It is best to switch between ground and supply for maximum performance. While the device may be disabled with shutdown voltages in between ground and supply, the idle current

may be greater than the typical value of 0.1μA. In either case, the shutdown pin should be tied to a definite voltage to avoid unwanted state changes.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry, which provides a quick, smooth transition to shutdown. Another solution is to use a single-throw switch in conjunction with an external pull-up resistor (or pull-down, depending on shutdown high or low application). This scheme guarantees that the shutdown pin will not float, thus preventing unwanted state changes.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the ft690 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The ft690 is unity-gain stable which gives the designer maximum system flexibility. The ft690 should be used in low gain configurations to minimize THD+N+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1Vrms are available from sources such as audio codecs. Please refer to the section, **Audio Power Amplifier Design**, for a more complete explanation of proper gain selection.

Besides gain, one of the major considerations is the closed loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in Figure 1. The input coupling capacitor, C_i, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons.

SELECTION OF INPUT CAPACITOR SIZE

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large input capacitor may not increase actual system performance.

In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor, C_i. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Besides minimizing the input capacitor size, careful consideration should be paid to the bypass capacitor value. Bypass capacitor, C_B, is the most critical component to minimize turn-on pops since it determines how fast the ft690 turns on. The slower the ft690's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn-on pop. Choosing CB equal to 1.0μF along with a small value of C_i (in the range of 0.1μF to 0.39μF), should produce a virtually clickless and popless shutdown function. While the device will function properly, (no oscillations or motorboating), with C_B equal to 0.1μF, the device will be much more susceptible to turn-on clicks and pops. Thus, a value of C_B equal to 1.0μF is recommended in all but the most cost sensitive designs.

AUDIO POWER AMPLIFIER DESIGN

A 1W/8Ω Audio Amplifier

Given:

Power Output	1Wrms
Load Impedance	8Ω
Input Level	1Vrms
Input Impedance	20kΩ
Bandwidth	100Hz–20kHz ± 0.25dB

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the **Typical Performance Characteristics** section, the supply rail can be easily found.

5V is a standard voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the ft690 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the **Power Dissipation** section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 2.

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (2)$$

$$R_f/R_i = A_{VD}/2$$

From Equation 2, the minimum A_{VD} is 2.83; use A_{VD} = 3. Since the desired input impedance was 20kΩ, and with a A_{VD} impedance of 2, a ratio of 1.5:1 of R_f to R_i results in an allocation of R_i = 20kΩ and R_f = 30kΩ. The final design step is to address the bandwidth requirements

which must be stated as a pair of −3dB frequency points. Five times away from a −3dB point is 0.17dB down from passband response which is better than the required ±0.25dB specified.

f_L = 100Hz/5 = 20Hz

f_H = 20kHz * 5 = 100kHz

R_i in conjunction with C_i create a highpass filter.

$C_i \geq 1/(2\pi*20k\Omega*20Hz) = 0.397\mu F$; use 0.39µF

The high frequency pole is determined by the product of the desired frequency pole, f_H, and the differential gain, A_{VD}. With a A_{VD} = 3 and f_H = 100kHz, the resulting GBWP = 300kHz which is much smaller than the ft690 GBWP of 2.5MHz. This figure displays that if a designer has a need to design an amplifier with a higher differential gain, the ft690 can still be used without running into bandwidth limitations

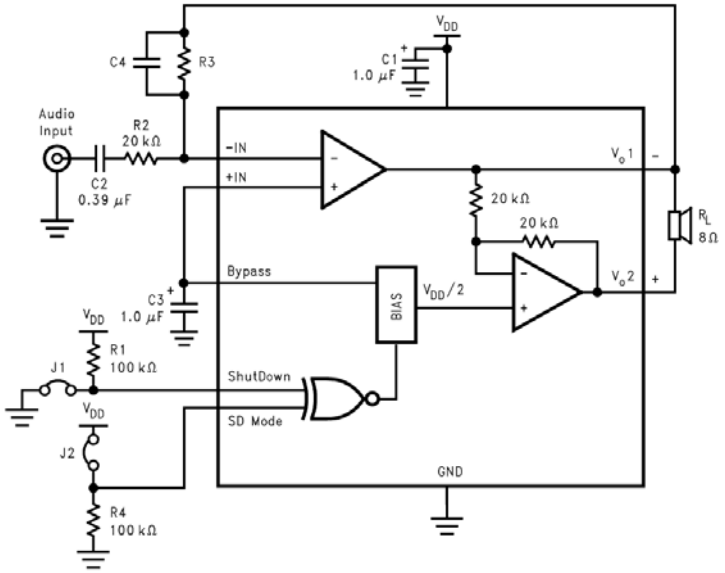


Figure 3. HIGHER GAIN AUDIO AMPLIFIER

The ft690 is unity-gain stable and requires no external components besides gain-setting resistors, an input coupling capacitor, and proper supply bypassing in the typical application. However, if a closed-loop differential gain of greater than 10 is required, a feedback capacitor (C4) may be needed as shown in Figure 2 to bandwidth limit the amplifier. This feedback capacitor creates a low pass filter that eliminates possible high frequency oscillations. Care should be taken when calculating the -3dB frequency in that an incorrect combination of R_3 and C_4 will cause rolloff before 20kHz. A typical combination of feedback resistor and capacitor that will not produce audio band high frequency rolloff is R_3 = 20kΩ and C_4 = 25pf. These components result in a -3dB point of approximately 320kHz.

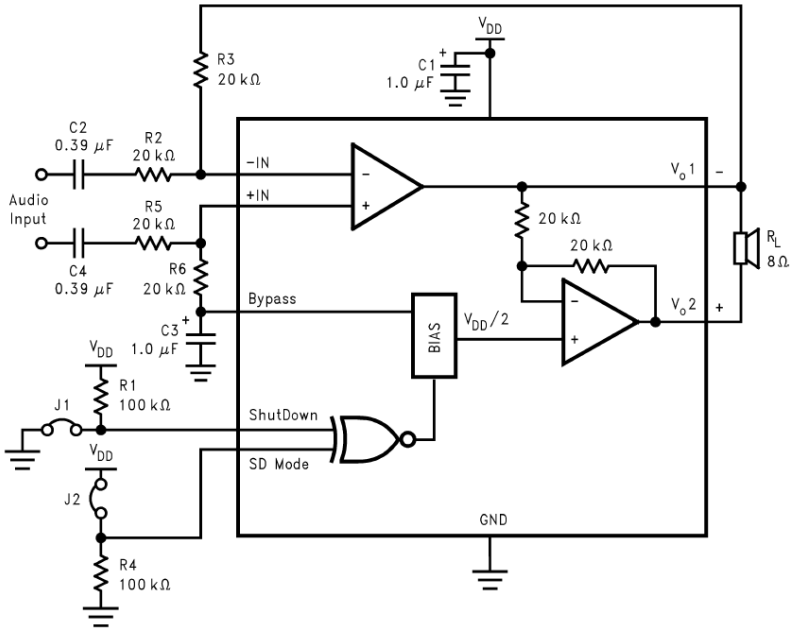
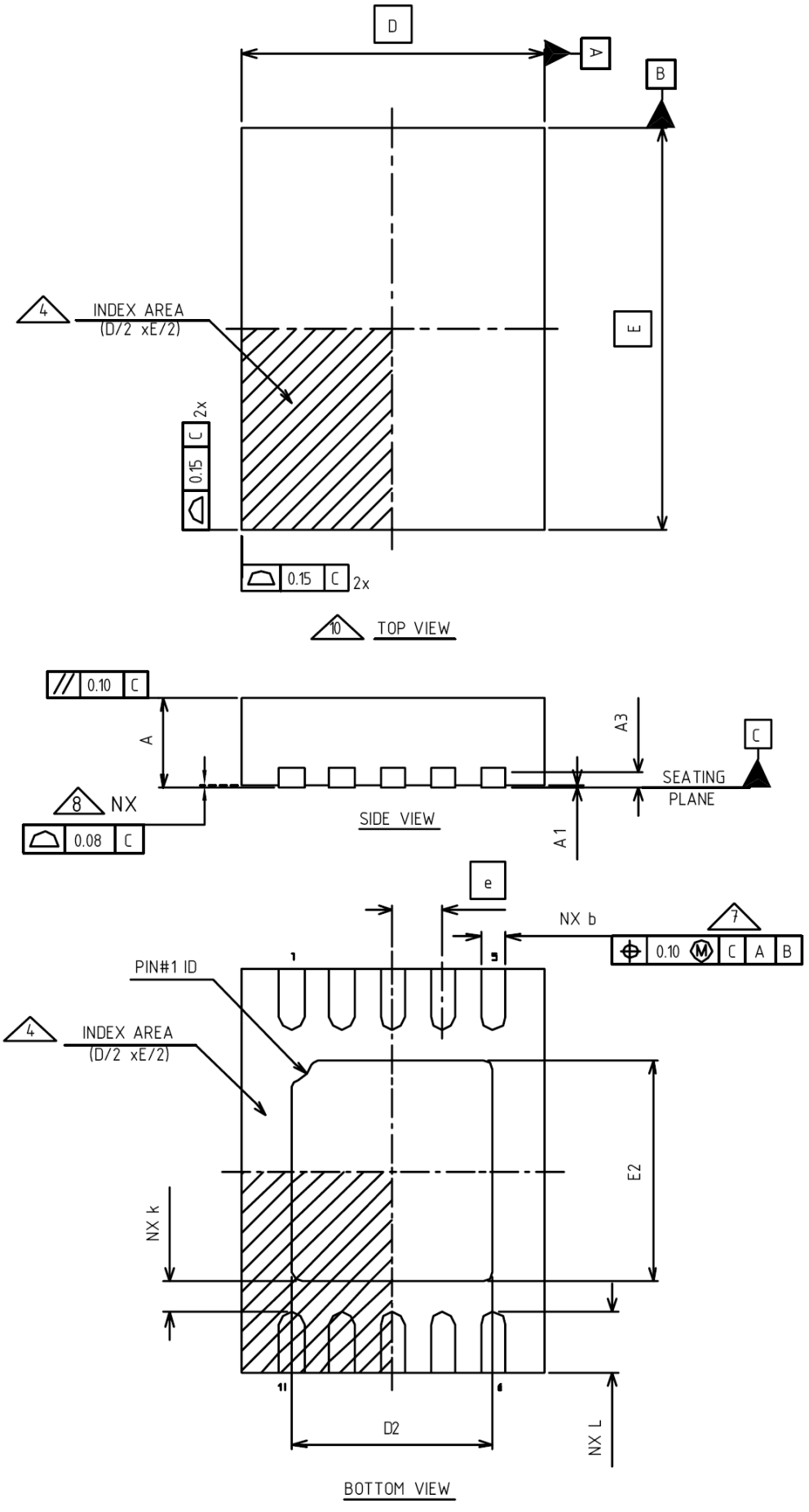


Figure 4. DIFFERENTIAL AMPLIFIER CONFIGURATION FOR ft690

PHYSICAL DIMENSIONS



Summary Table					
Lead Pitch	Lead Count	Body Size	Very Thin Variation	Very Very Thin Variation	Pin #1 ID
0.50	10	3X4	VNJR-1	WNJR-1	R0.20

COMMON DIMENSION						
SYMBOL	V : Very Thin			W : Very Very Thin		
	MIN	NOM	MAX	MIN	NOM	MAX
A				0.70	0.75	0.80
A1				0.00	0.02	0.05
A3				---	0.15 ref	---
NOTES						

VARIATIONS								
SYMBOL	VNJR-1 WNJR-1			NOTE				NOTE
	MIN	NOM	MAX		MIN	NOM	MAX	
b	0.18	0.25	0.35					
D	3.00 BSC							
D2	1.85	2.00	2.10					
E	4.00 BSC							
E2	2.05	2.20	2.30					
e	0.65 BSC							
L	0.50	0.60	0.70					
N	10							
ND	5							
NE	0							
NOTE	---							
REF	---							
ISSUE	---							

Figure 5. DFN Package Physical Dimension

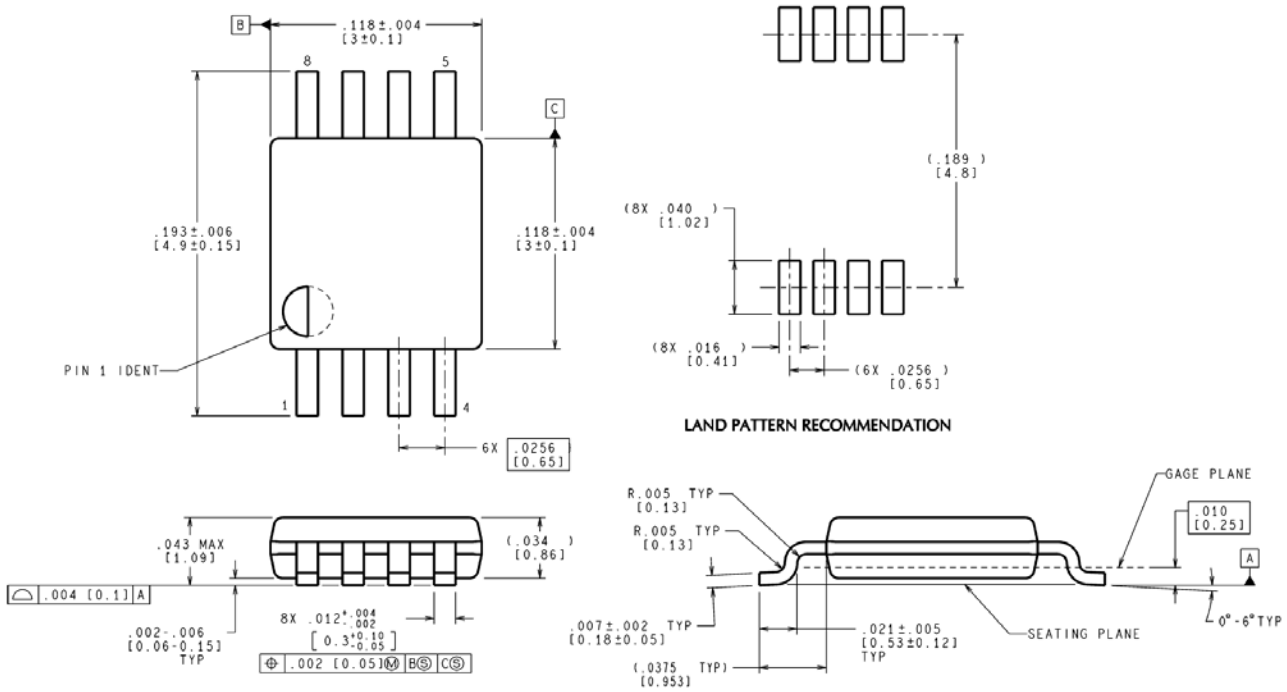


Figure 6. MSOP Package Physical Dimension

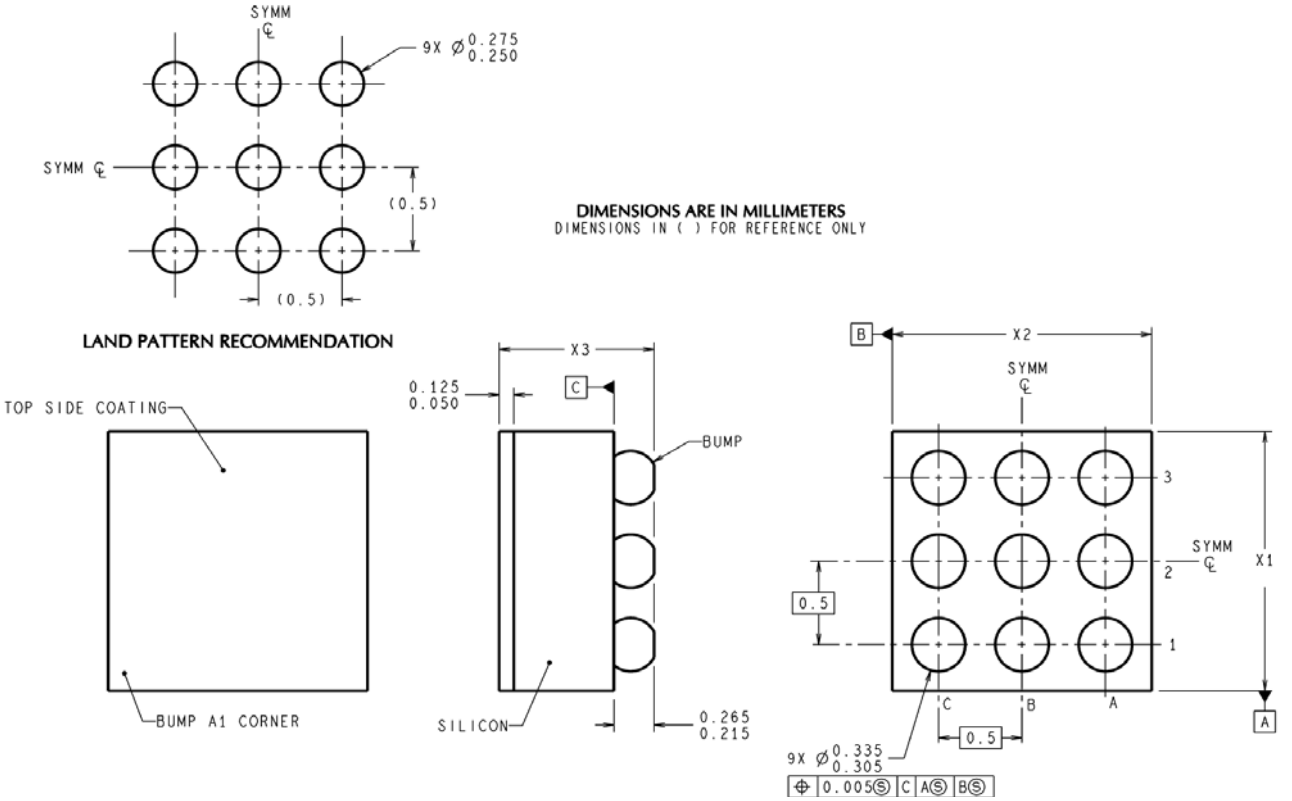


Figure 7. WCSP Package Physical Dimension

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