ft4266

1.3W Dual Audio Power Amplifier

Introductions

The ft4266 is a 1.3W bridge-connected dual audio amplifier. When supplied with 5V voltage, the ft4266 can deliver 1.3W to a 8Ω load with the THD+N rate lower than 1.0%.

The dual audio power amplifier design of ft4266 provides high quality dual-channel output while requiring few external components and consuming very little PCB space.

The ft4266's power-saving feature is another plus tailored for handheld device. When the power-saving mechanism is activated, only 0.04μA current is running on the ft4266. Other features such as thermal shutdown protection and "click and pops" reduction during power-up ensure the safety and reliability in real applications.

Features

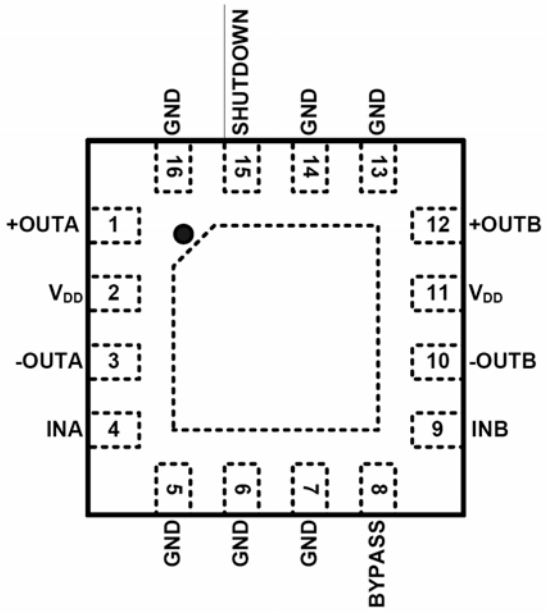
- Micro power shutdown mode
- Thermal shutdown protection
- Improved "click and pop" suppression circuitry
- Space-saving QFN package.
- Package: QFN-16 (3mm x 3mm)

Specifications

- P_O @ 1% THD+N, V_{DD} = 5V
  - R_L = 8Ω, P_O = 1.3W (TYP)
- Shutdown current: 0.04μA
- Supply voltage range: 2.7V to 5.5V
- PSRR @ 217Hz: 70dB (TYP)

Packaging Details

Figure 1. ft4266 Pinout Diagram



Pin	Pin	I/O	Description
+OUTA	1	O	Left channel +output
V_{DD}	2,11		Supply voltage
-OUTA	3	O	Left channel -output
INA	4	I	Left channel input
GND	5,6,7,13,14,16		GND
Bypass	8		Bypass capacitor which provides the common mode voltage
INB	9	I	Right channel input
-OUTB	10	O	Right channel –output
+OUTB	12	O	Right channel +output
SHUTDOWN	15	I	Shut down control, hold low for shutdown mode

Parametric Data

Absolute Maximum Ratings

Caution! The parameters provided in this table are the maximum values. Parameters exceeding these values may cause permanent damage to the device and the board.

Symbol	Parameters	Value
V_{DD}	Supply Voltage	6.0V
V_I	Input Voltage	−0.3V to V_{DD} +0.3V
	Power Dissipation	Internally Limited
T_J	Junction Temperature	150°C
T_{stg}	Storage Temperature	−65°C to +150°C
Soldering Information		
	Small Outline Package	
	Vapor Phase (60 sec.)	215°C
	Infrared (15 sec.)	220°C
Thermal Resistance		
θ_{JC} (TYP)		3°C/W
θ_{JA} (TYP`)		42°C/W

Operation Ratings

Parameters	Value
Temperature Range $T_{MIN} \le T_A \le T_{MAX}$	-40°C ≤ T_A ≤ 85°C
Supply Voltage	2.7V ≤ V_{DD} ≤ 5.5V

Electrical Characteristics

Typical, V_{DD} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
V_{DD}	Supply voltage			2.7	V(min)
				5.5	V(max)
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A	4.5	10	mA(max)
I_{SD}	Shutdown Current	GND applied to the SHUTDOWN pin	0.04	1.0	μA (max)
V_{IHSD}	Shutdown High Input Voltage		1.2	1.5	V(min)
V_{ILSD}	Shutdown Low Input Voltage		1	0.7	V(max)
T_{WU}	Turn On Time	1μF Bypass Cap (C4)	100		ms

Operation, V_{DD} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5		mV(max)
P_O	Output Power (Note 11)	THD + N = 1%, f = 1kHz, R_L = 8Ω	1.3	1.2	W(min)
		THD + N = 10%, f = 1kHz, R_L = 8Ω	1.6		W(min)
THD+N	Total Harmonic Distortion + Noise	f = 1kHz, A_{VD} = 2, R_L = 8Ω, P_O = 0.9W	0.06		%
PSRR	Power Supply Rejection Ratio	Input un-terminated, 217Hz, V_{ripple} = 200mV_{p-p}, C_4 = 1μF, R_L = 8Ω	70		dB
		Input un-terminated, 1kHz, V_{ripple} = 200mV_{p-p}, C_4 = 1μF, R_L = 8Ω	60.		dB
		Input grounded, 217Hz, V_{ripple} = 200mV_{p-p}, C_4 = 1μF, R_L = 8Ω	70		dB
		Input grounded, 1kHz, V_{ripple} = 200mV_{p-p}, C_4 = 1μF, R_L = 8Ω	65		dB
Xtalk	Channel separation	f=1KHz, C_4 = 1μF	80		dB

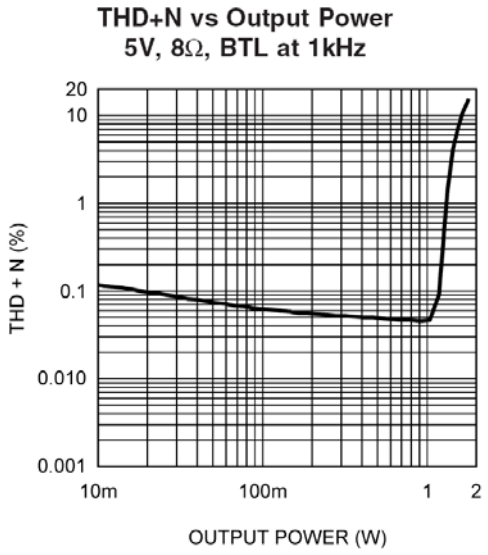
Typical, V_{DD} = 3V, T_A = 25°C

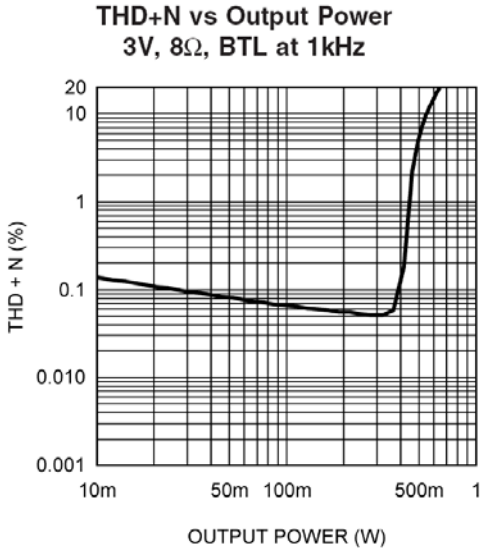
Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A	3	6	mA(max)
I_{SD}	Shutdown Current	GND applied to the SHUTDOWN pin	0.02	0.5	μA (max)
V_{IHSD}	Shutdown High Input Voltage		1.1	1.3	V(min)
V_{ILSD}	Shutdown Low Input Voltage		0.8	0.5	V(max)
T_{WU}	Turn On Time	1μF Bypass Cap (C4)	95		ms

Operation, V_{DD} = 3V, T_A = 25°C

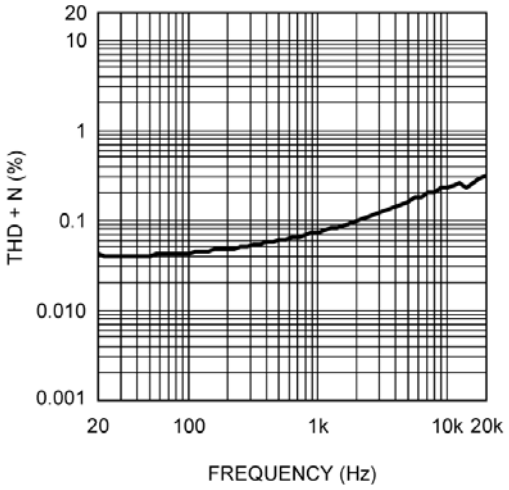
Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
V_{OS}	Output Offset Voltage	V_{IN} = 0V	2.5		mV(max)
P_O	Output Power (Note 11)	THD + N = 1%, f = 1kHz, R_L = 8Ω	0.45	0.40	W(min)
		THD + N = 10%, f = 1kHz, R_L = 8Ω	0.54		W
THD+N	Total Harmonic Distortion + Noise	f = 1kHz, A_{VD} = 2, R_L = 8Ω, P_O =0.35W	0.08		%
PSRR	Power Supply Rejection Ratio	Input un-terminated, 217Hz, V_{ripple} = 200mV_{p-p}, C_4 = 1μF, R_L = 8Ω	74		dB
		Input un-terminated, 1kHz, V_{ripple} = 200mV_{p-p}, C_4 = 1μF, R_L = 8Ω	64		dB
		Input grounded, 217Hz, V_{ripple} = 200mV_{p-p}, C_4 = 1μF, R_L = 8Ω	70		dB
		Input grounded, 1kHz, V_{ripple} = 200mV_{p-p}, C_4 = 1μF, R_L = 8Ω	65		dB
Xtalk	Channel separation	f=1kHz, C_4 = 1μF	80		dB

Typical Performance Characteristics

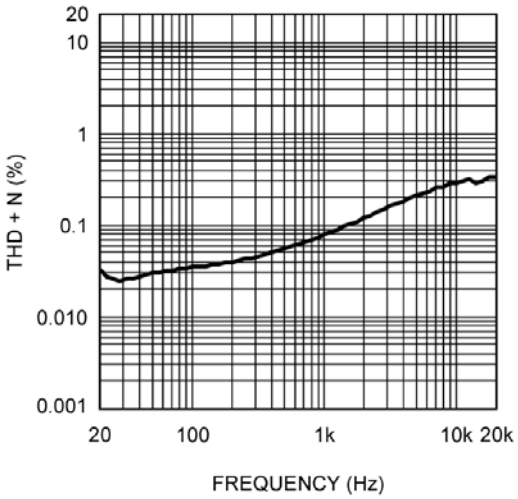




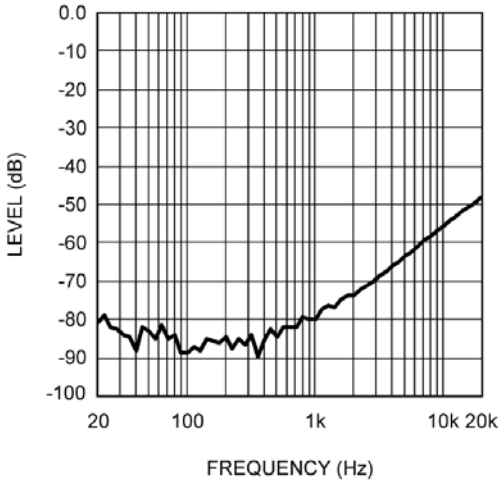
THD+N vs Frequency
5V, 8Ω, BTL at 400mW



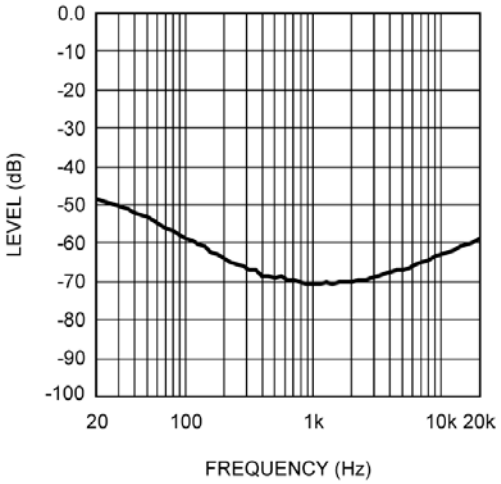
THD+N vs Frequency
3V, 8Ω, BTL at 150mW



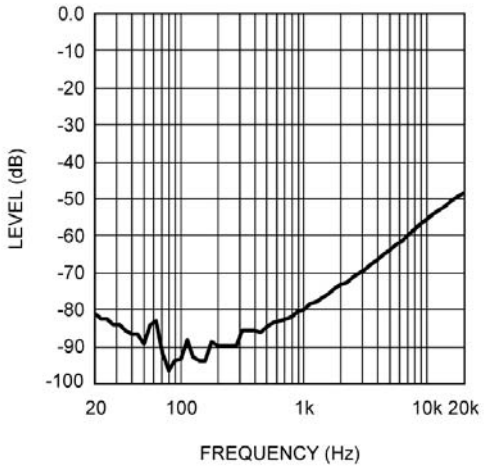
PSRR
5V, 8Ω, BTL, Input Unterminated



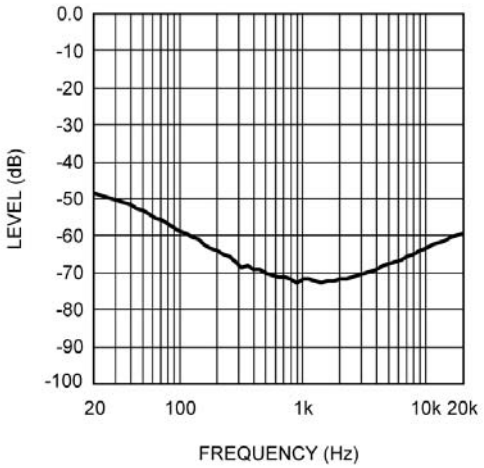
PSRR
5V, 8Ω, BTL, Input Terminated



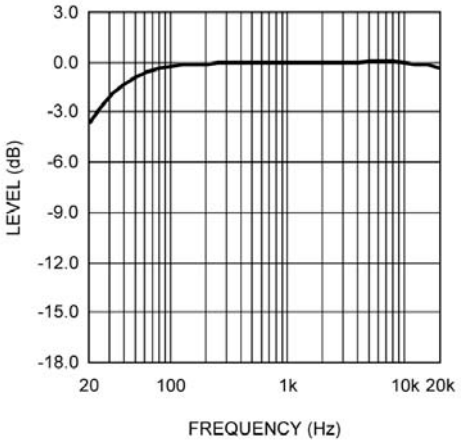
PSRR
3V, 8Ω, BTL, Input Unterminated



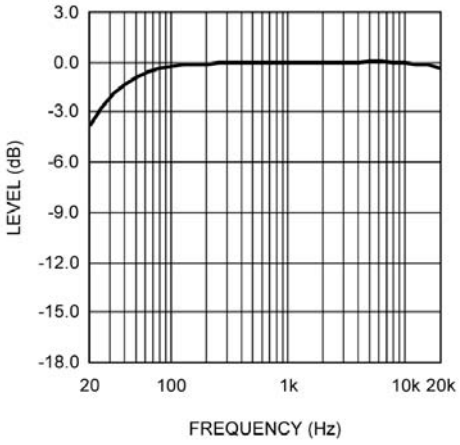
PSRR
3V, 8Ω, BTL, Input Terminated



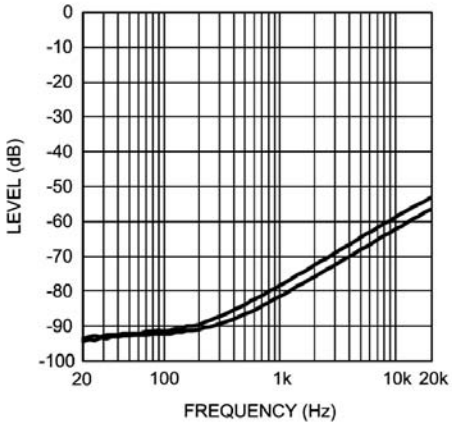
Frequency Response
5V, 8Ω, BTL



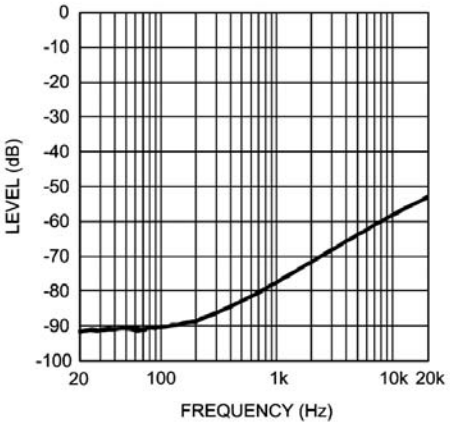
Frequency Response
3V, 8Ω, BTL



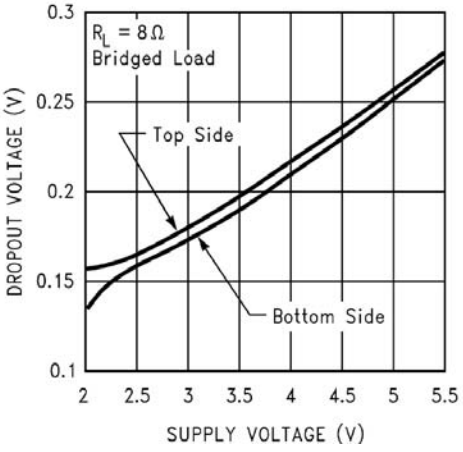
Crosstalk
5V, 8Ω, BTL



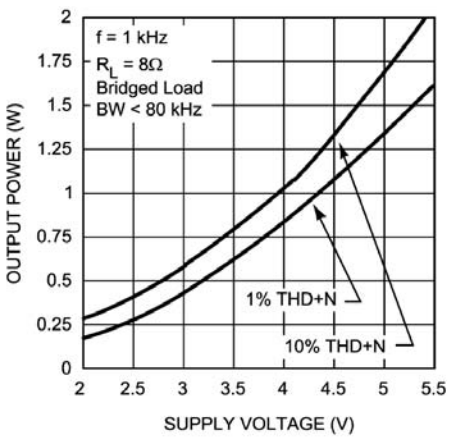
Crosstalk
3V, 8Ω, BTL

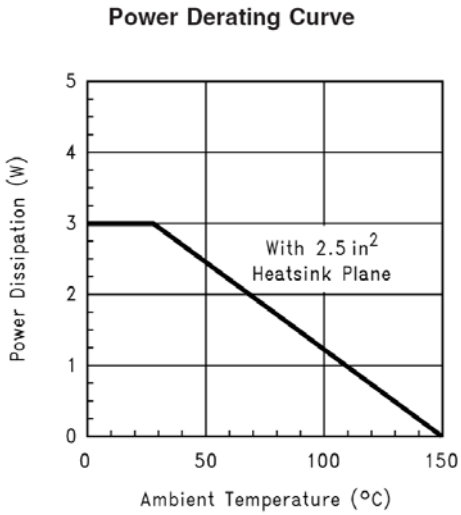


Dropout Voltage vs
Supply Voltage



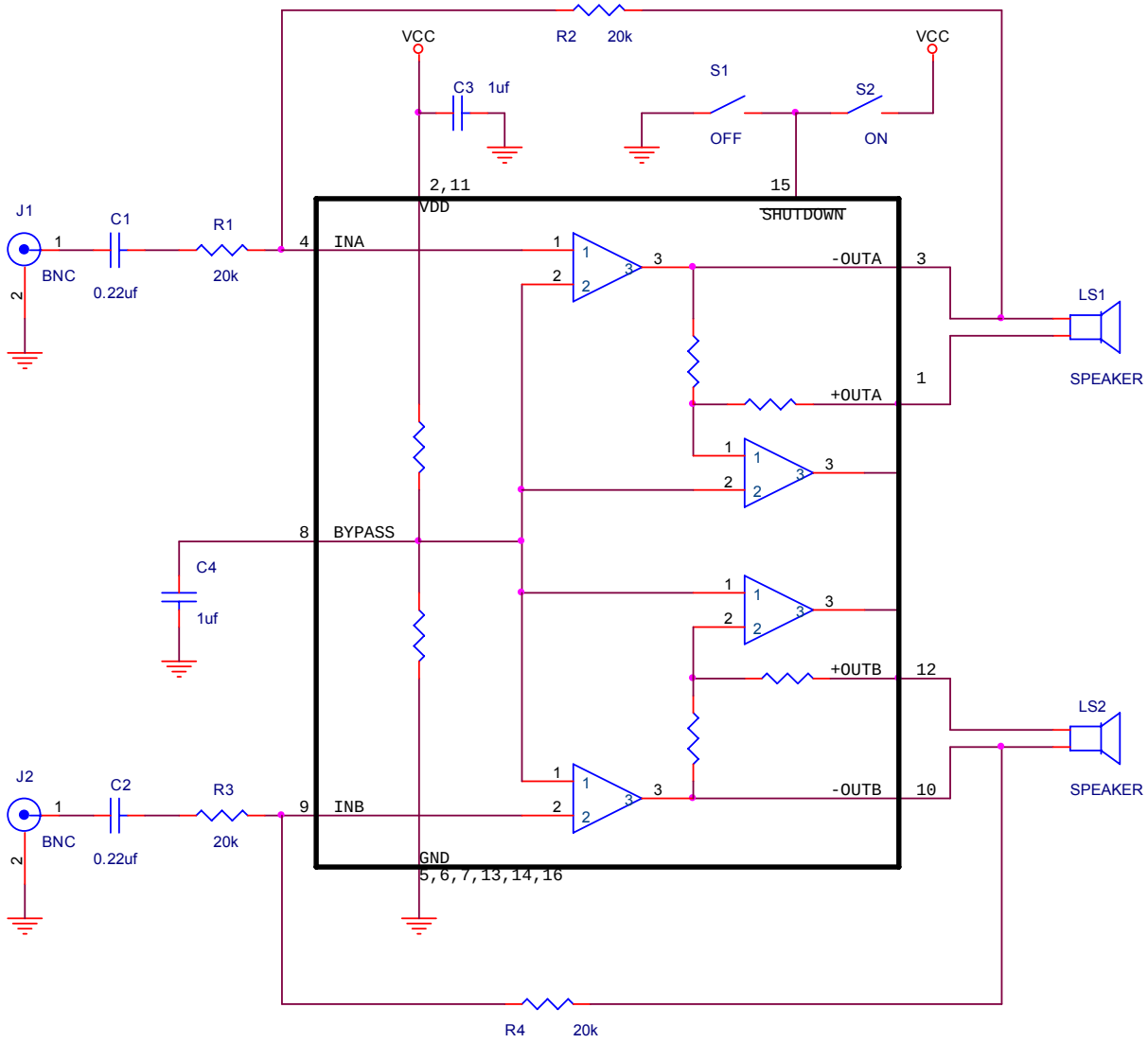
Output Power vs
Supply Voltage





Application Information

Figure 2. Typical Application Schematics



Bridged Amplifier

The ft4266 consists of two pairs of amplifiers which form a dual-channel stereo amplifier. External feedback resistors R2 and R4 and input resistors R1 and R3 set the closed-loop gain of Amplifier A (-OUT) and Amplifier B (-OUT), while two internal 20kΩ resistors set Amplifier A (+OUT) and Amplifier B (+OUT) gains to 1. The amplifiers' (-OUT) outputs also serve as (+OUT)'s inputs and produce (+OUT) outputs identical in magnitude but opposite in phase with the (-OUT) signal. Hence the load between the (+OUT) and (-OUT) is driven differentially, or in another word, in bridge mode.

The differential gain result:

$$A_{VD} = 2 * (R_F / R_I) \qquad (1)$$

Bridge mode amplifier provides four times the output power of that from single-ended amplifier under the same condition. However, the power increase calculation assumes that amplifier is not current limited or that the output signal is not clipped. Therefore, to ensure minimum output signal clipping, care must be taken when choosing an amplifier's closed-loop gain.

Power Dissipation

Power dissipation is critical for either single-ended or bridged amplifier board design. Equation (2) indicates the maximum power dissipation for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \quad \text{Single-ended} \qquad (2)$$

For ft4266 where two operational amplifiers per channel are adopted, the internal power dissipation per channel is four times that of a single-ended amplifier, as indicated in Equation (3). Given a 5V input power and a 8Ω output load, the maximum total power dissipation is 0.63W for single channel or 1.23W for stereo output.

$$P_{DMAX} = 4 * (V_{DD})^2 / (2\pi^2 R_L) \quad \text{Bridge mode} \qquad (3)$$

The ft4266 single channel power dissipation must not exceed the P_{DMAX}' value in equation (4). The ft4266's T_{JMAX} is 150°C; Θ_{JA} is 20°C/W given that the package is soldered to a DAP pad that expands to a copper area of 5 square inches on PCB. Equation (5) is a variation of Equation (4) for calculating the maximum ambient temperature at maximum stereo power dissipation when junction temperature limitation is not exceeded.

$$P_{DMAX}' = (T_{JMAX} - T_A) / \Theta_{JA} \qquad (4)$$

$$T_A = T_{JMAX} - 2*P_{DMAX}\Theta_{JA} \qquad (5)$$

The examples above assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases. If P_{DMAX} in Equation (2) or (3) exceeds P_{DMAX}' in Equation (4), measures should be taken by either decreasing the supply voltage, increasing load impedance, reducing the ambient temperature or adding external heat sink. When heat sink is applied to system design, the Θ_{JA} equals (Θ_{JC} + Θ_{CS} + Θ_{SA}). (Θ_{JC}: junction-to-case thermal impedance; Θ_{CS}: case-to-sink thermal impedance; Θ_{SA}: sink-to-ambient thermal impedance).

Power Supply Bypassing

Proper power supply bypassing is critical for low noise performance and high power supply rejection in a power amplifier. Applications employing 5V regulator typically use a 10μF in parallel with a 0.1μF filter capacitor to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a 1.0μF tantalum bypass capacitor connected between the ft4266's power supply pins and the ground. **DO NOT** substitute a ceramic capacitor for the tantalum, or it would cause oscillation. Optimizing the length of leads and traces between the ft4266 and ground also help to improve the power supply bypassing.

Micro-Power Shutdown

The ft4266's power saving scheme is realized through the SHUTDOWN pin and the voltage applied on it. The micro-power shutdown is performed to turn off the amplifier's bias circuitry as long as the SHUTDOWN pin is grounded. Typically, current as low as 0.04μA can be achieved by applying a voltage close to GND to the SHUTDOWN pin.

The Micro-Power shutdown can be initiated and controlled by either a single-pole, single-throw switch, or a microprocessor, or a microcontroller. A switch is employed in the reference design illustrated in Figure 1. Connect an external 100k resistor between the SHUTDOWN pin and the ground; connect the switch between the SHUTDOWN pin and V_{DD}. Closing the switch sets the amplifier in normal function, while opening the switch sets the SHUTDOWN pin to ground through the 100k resistor and consequently activates the shutdown. The switch and resistor design guarantees that the SHUTDOWN pin is not float to prevent unwanted state changes. In digital systems, where microprocessors or microcontrollers are deployed, digital output can be applied to control the SHUTDOWN input voltage.

Components

Proper external components are essential for building up an ft4266 system. Although the ft4266 can function well with various external component combinations, most optimized performance and cost are achieved only with careful selection.

The ft4266 is unity-gain stable which provides wide design feasibility for designers. The gain is set to meet individual application requirements but no higher in order to get minimum THD+N and maximum Signal-Noise Ratio (SNR). However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as CODECs have outputs of $1V_{RMS}$ ($2.83V_{P-P}$).

Input Capacitor

High value input coupling capacitors (C1, C2) are required to amplifying the low inputting audio signal as illustrated in Figure 1. However, high value capacitor can be expensive in cost and big in size which may become a fatal issue for handheld devices. Besides, the speakers in handheld and portable devices, either internal or external, seldom reproduce signals below 150Hz. Therefore, big input capacitor has very little influence in output signal quality in applications using limited frequency response speakers.

Besides the cost and size, C1 and C2 also influence the click and pop performance. When the supply voltage is fed in, a transient (pop) is generated as the charge on the input capacitor changes from 0 to a quiescent state. The magnitude of the pop is proportional to the input capacitance. The higher the capacitance is, the more time it requires to reach quiescent DC voltage (usually $0.5V_{DD}$) when charged

with a fixed current. The amplifier output charges the input capacitor through the feedback resistors (R2, R4). Therefore, pops can be minimized with input capacitance no higher than necessary to provide -3dB frequency.

R1 and R3 are input resistors. C1 and C2 produce -3dB high pass filter cutoff frequency as stated in Equation (7).

$$f_{-3dB} = 1 / (2\pi R_{IN} C_{IN}) = 1 / (2\pi R1C1) \qquad (7)$$

Bypass Capacitor

Bypass capacitor determines the time needed for setting ft4266 to quiescent operation and plays an important role in minimizing turn-on pops. The slower the output ramp to quiescent DC voltage ($0.5V_{DD}$ nominal), the smaller the turn-on pop is. The relationship between the capacitance and turn-on time is listed in the table below. In Figure 1, C4 is a 1.0μF bypass capacitor which, altogether with C1, minimizes the pops and clicks.

C4	T_{ON}
0.01μF	38ms
0.1μF	40ms
0.22μF	50ms
0.47μF	70ms
1.0μF	100ms

Besides the click and pop reduction function, the C4 connected between the BYPASS pin and the ground improves the internal bias voltage stability and amplifier PSRR.

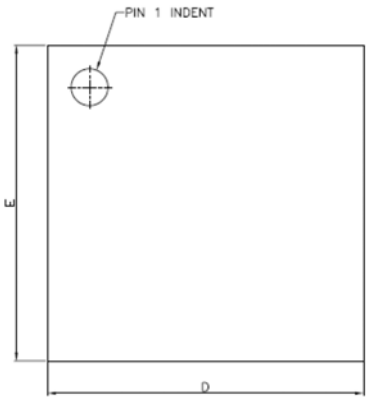
Optimizing click and POP reduction performance

The ft4266 contains circuitry that minimizes turn-on and shutdown transients or “clicks and pop”. For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. When the part is turned on, an internal current source changes the voltage of the BYPASS pin in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches 1/2 V_{DD}. As soon as the voltage on the bypass pin is stable, the device becomes fully operational. Although the BYPASS pin current cannot be modified, changing the size of C4 alters the device’s turn-on time and the magnitude of “clocks and pops”. Increasing the value of C4 reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of C4 increases, the turn-on time increases. There is a linear relationship between the size of C4 and the turn-on time.

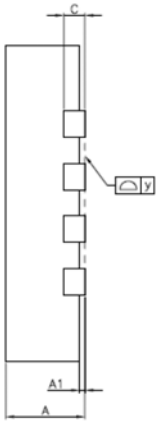
In order eliminate “clicks and pops”, all capacitors must be discharged before turn-on. Rapidly switching V_{DD} on and off may not allow the capacitors to fully discharge, which may cause “clicks and pops”.

Package Information

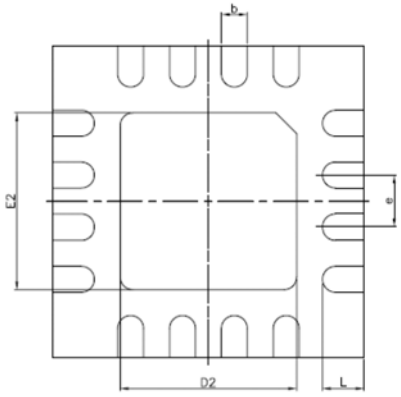
Top view



Side View



Bottom View



Symbol	Dimension (mm)		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
C	——	0.02 REF.	——
D	2.90	3.00	3.10
D2	1.65	1.70	1.75
E	2.90	3.00	3.10
E2	1.65	1.7	1.75
e	——	0.50	——
L	0.35	0.40	0.45
y	0.00	——	0.075

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