fangtek

ft4888

2.1W Dual Audio Amplifier with 3D Enhancement
Datasheet (Rev. 2.0)

Introductions

The ft4888 is a 2.1W bridge-connected dual audio amplifier. When supplied with 5V voltage, the ft4888 can deliver 2.1W to a 4Ω load or 2.4W to 3Ω load with the THD+N rate lower than 1.0%.

The dual audio power amplifier design of ft4888 provides high quality dual-channel output while requiring few external components and consuming very little PCB space. With two device selection inputs (HP_LOGIC and HP_SENSE) of different logic level thresholds respectively, the ft4888 can connect to a pair of dual-channel speakers or to a stereo headphone. The HP_SENSE logic connects to the headphone jack to detect if headphone is present. The other logic, HP_LOGIC, is determined by standard logic level standards.

The ft4888 also features an optional 3D enhancement design which can help widen the perceived soundstage from a stereo audio signal to improve stereo channel sounding effect.

The ft4888's power-saving feature is another plus tailored for handheld device. When the power-saving mechanism is activated, only 0.04μA current is running on the ft4888. Other features such as thermal shutdown protection and "click and pops" reduction during power-up ensure the safety and reliability in real applications.

Features

- Dual channel audio amplifier design
- User-configurable headphone select scheme
- 3D effect enhancement
- Micro power shutdown mode
- Thermal shutdown protection
- Improved "click and pop" suppression circuitry
- Space-saving LLP package.

Specifications

- P_O @ 1% THD+N, V_{DD} = 5V
  - R_L = 3Ω, P_O = 2.4W (TYP)
  - R_L = 4Ω, P_O = 2.1W (TYP)
  - R_L = 8Ω, P_O = 1.3W (TYP)
- Single-ended mode THD+N @ 0.01% under 75mW, 32Ω load impedance (5V, 1kHz)
- Shutdown current: 0.04μA
- Supply voltage range: 2.7V to 5.5V
- PSRR @ 217Hz: 85dB (TYP)

Packaging Details

Figure 1. ft4888 Pinout Diagram

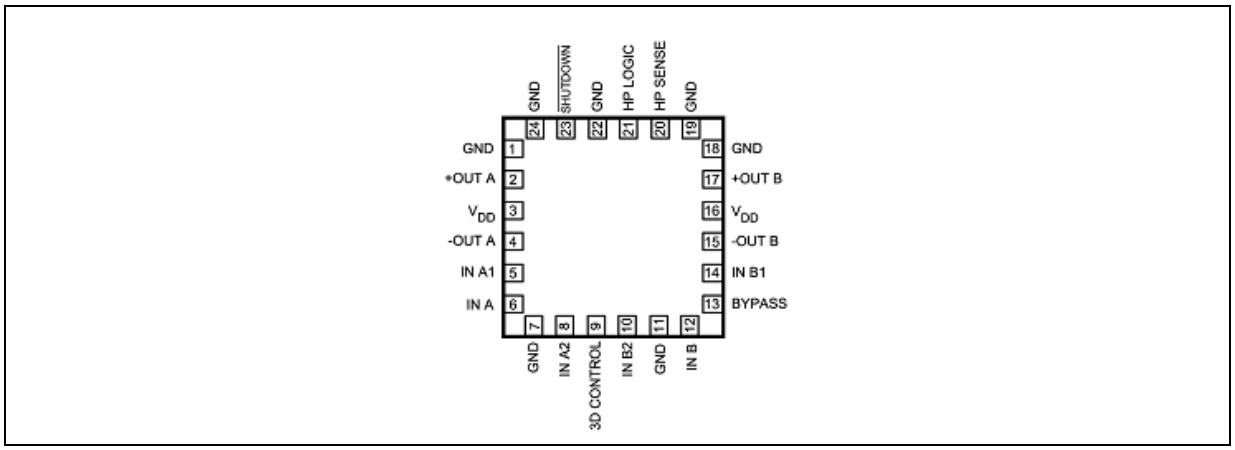
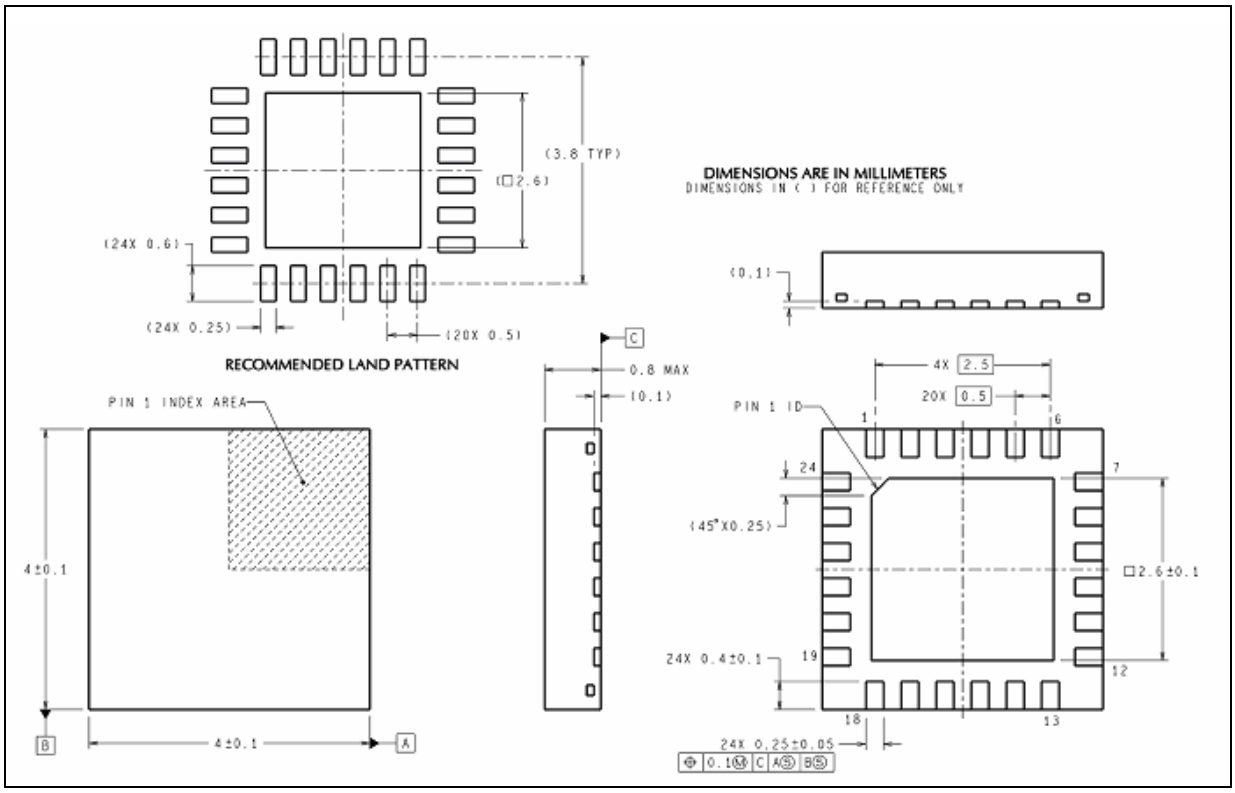
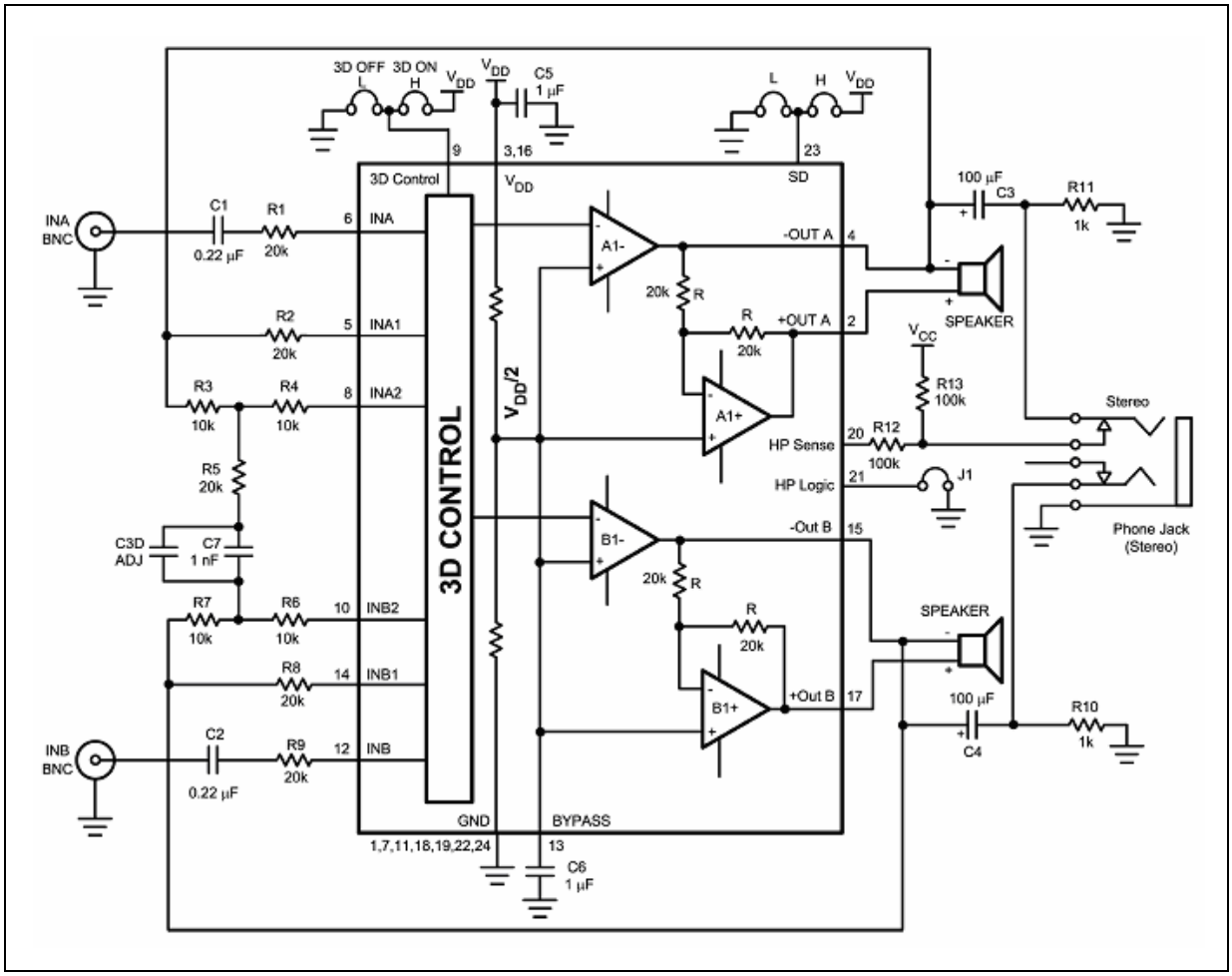


Figure 2. ft4888 Package Dimensions



Application Information

Figure 3. Typical Application Schematics



Bridged Amplifier

The ft4888 consists of two pairs of amplifiers (illustrated as A1 and B1 in Figure 1) which form a dual-channel stereo amplifier. External feedback resistors R2 (or R3, R4) and R8 (or R6, R7) and input resistors R1 and R9 set the closed-loop gain of Amplifier A (-OUT) and Amplifier B (-OUT), while two internal 20kΩ resistors set Amplifier A (+OUT) and Amplifier B (+OUT) gains to 1. The amplifiers' (-OUT) outputs also serve as (+OUT)'s inputs and produce (+OUT) outputs identical in magnitude but opposite in phase with the (-OUT) signal. Hence the load between the (+OUT) and (-OUT) is driven differentially, or in another word, in bridge mode.

The differential gain result:

$$A_{VD} = 2 * (R_F / R_I) \qquad (1)$$

Bridge mode amplifier provides four times the output power of that from single-ended amplifier under the same condition. However, the power increase calculation assumes that amplifier is not current limited or that the output signal is not clipped. Therefore, to ensure minimum output signal clipping, care must be taken when choosing an amplifier's closed-loop gain.

Power Dissipation

Power dissipation is critical for either single-ended or bridged amplifier board design. Equation (2) indicates the maximum power dissipation for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L)$ Single-ended *(2)*

For ft4888 where two operational amplifiers per channel are adopted, the internal power dissipation per channel is four times that of a single-ended amplifier, as indicated in Equation (3). Given a 5V input power and a 4Ω output load, the maximum total power dissipation is 1.27W for single channel or 2.54W for stereo output.

$P_{DMAX} = 4 * (V_{DD})^2 / (2\pi^2 R_L)$ Bridge mode *(3)*

The ft4888 single channel power dissipation must not exceed the P_{DMAX}' value in equation (4). The ft4888's T_{JMAX} is 150°C; Θ_{JA} is 20°C/W given that the package is soldered to a DAP pad that expands to a copper area of 5 square inches on PCB. Equation (5) is a variation of Equation (4) for calculating the maximum ambient temperature at maximum stereo power dissipation when junction temperature limitation is not exceeded.

$P_{DMAX}' = (T_{JMAX} - T_A) / \Theta_{JA}$ *(4)*

$T_A = T_{JMAX} – 2*P_{DMAX}\Theta_{JA}$ *(5)*

The examples above assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases. If P_{DMAX} in Equation (2) or (3) exceeds P_{DMAX}' in Equation (4), measures should be taken by either decreasing the supply voltage, increasing load impedance, reducing the ambient temperature or adding external heat sink. When heat sink is applied to system design, the Θ_{JA} equals ($\Theta_{JC} + \Theta_{CS} + \Theta_{SA}$). ($\Theta_{JC}$: junction-to-case thermal impedance; Θ_{CS}: case-to-sink thermal impedance; Θ_{SA}: sink-to-ambient thermal impedance).

Power Supply Bypassing

Proper power supply bypassing is critical for low noise performance and high power supply rejection in a power amplifier. Applications employing 5V regulator typically use a 10μF in parallel with a 0.1μF filter capacitor to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a 1.0μF tantalum bypass capacitor connected between the ft4888's power supply pins and the ground. **DO NOT** substitute a ceramic capacitor for the tantalum, or it would cause oscillation. Optimizing the length of leads and traces between the ft4888 and ground also help to improve the power supply bypassing.

Micro-Power Shutdown

The ft4888's power saving scheme is realized through the SHUTDOWN pin and the voltage applied on it. The micro-power shutdown is performed to turn off the amplifier's bias circuitry as long as the SHUTDOWN pin is grounded. Typically, current as low as 0.04μA can be achieved by applying a voltage close to GND to the SHUTDOWN pin.

The Micro-Power shutdown can be initiated and controlled by either a single-pole, single-throw switch, or a microprocessor, or a microcontroller. A switch is employed in the reference design illustrated in Figure 1. Connect an external 100k resistor between the SHUTDOWN pin and the ground; connect the switch between the SHUTDOWN pin and V_{DD}. Closing the switch sets the amplifier in normal function, while opening the switch sets the SHUTDOWN pin to ground through the 100k resistor and consequently activates the shutdown. The switch and resistor design guarantees that the

SHUTDOWN pin is not float to prevent unwanted state changes. In digital systems, where microprocessors or microcontrollers are deployed, digital output can be applied to control the SHUTDOWN input voltage.

Headphone and Speaker Selection

The headphone and speaker selection in ft4888 is achieved with the HP_SENSE and HP_LOGIC pins. When both HP_SENSE and HP_LOGIC pins are pulled low, the bridged mode is enabled. When either pin is pulled high, the (+OUT) outputs are cut off and the amplifier is set to single-ended mode.

Figure 4 illustrates the headphone and speaker selection scheme using HP_SENSE pin. When headphone is not present, the HP_SENSE pin receives a voltage as low as 50mV which pulled the pin low and set the amplifier in bridged mode. When headphone is inserted into the jack, the sense pin is disconnected and the HP_SENSE is pulled high. Therefore the amplifier is set to single-ended mode.

The HP_LOGIC pin can also be used to select headphone or speaker. When HP_LOGIC is pulled high, the ft4888 operates in single-ended mode; when pulled low, the ft 4888 operates in bridged mode subjected to that the HP_SENSE pin is also pulled low.

Figure 4. Headphone Circuit with HP_SENSE

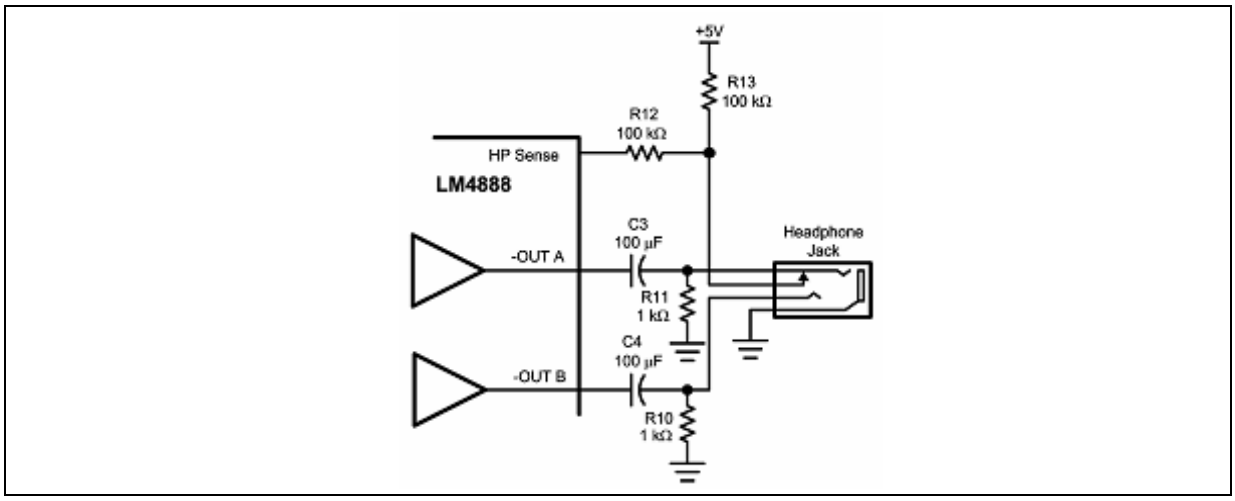


Table 1. Headphone and Speaker Selection Pin Signals

HP_LOGIC Pin	HP_SENSE Pin	Operational Output
High	Don't care	Single-ended mode
Low	Low (Headphone not present)	Bridged mode
Don't care	High (Headphone present)	Single-ended mode

3D Enhancement

The ft4888 provides a 3D enhancement feature which help to improve the stereo sound channel separation when the left and right speakers are too close to each other. This feature is achieved by widening the perceived soundstage from the analog audio signal.

In the reference design, an external RC network is added to enable or disable the 3D enhancement. The degree of 3D enhancement is decided by R5 and C7 or C3D_ADJ. Decreasing the R5 resistance can achieve 3D effect enhancement. Increasing the C7 or C3D capacitance will decrease the low cutoff frequency at which point the 3D enhancement starts to function. Refer to Equation below.

$$F_{3D(-3dB)} = 1/2\pi(R_{3D})(C_{3D}) \quad (6)$$

To activate the 3D enhancement, apply VDD to the 3D_CONTROL pin to increase the gain by a multiplication factor of (1 + 20kΩ/R5). When R5 is 20Ω, the multiplication factor is 2, and the gain increases by 6dB. Note that when 3D enhancement is enabled, R3, R4, R7, R8 take the place of R2 and R8.

Components

Proper external components are essential for building up an ft4888 system. Although the ft4888 can function well with various external component combinations, most optimized performance and cost are achieved only with careful selection.

The ft4888 is unity-gain stable which provides wide design feasibility for designers. The gain is set to meet individual application requirements but no higher in order to get minimum THD+N and maximum Signal-Noise Ratio (SNR). However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as CODECs have outputs of $1V_{RMS}$ ($2.83V_{P-P}$).

Input Capacitor

High value input coupling capacitors (C1, C2) are required to amplifying the low inputting audio signal as illustrated in Figure 1. However, high value capacitor can be expensive in cost and big in size which may become a fatal issue for handheld devices. Besides, the speakers in handheld and portable devices, either internal or external, seldom reproduce signals below 150Hz. Therefore, big input capacitor has very little influence in output signal quality in applications using limited frequency response speakers.

Besides the cost and size, C1 and C2 also influence the click and pop performance. When the supply voltage is fed in, a transient (pop) is generated as the charge on the input capacitor changes from 0 to a quiescent state. The magnitude of the pop is proportional to the input capacitance. The higher the capacitance is, the more time it requires to reach quiescent DC voltage (usually $0.5V_{DD}$) when charged with a fixed current. The amplifier output charges the input capacitor through the feedback resistors (R2, R8). Therefore, pops can be minimized with input capacitance no higher than necessary to provide -3dB frequency.

R1, R4, R5 and R6 are input resistors. C1 and C2 produce -3dB high pass filter cutoff frequency as stated in Equation (7).

$$f_{-3dB} = 1 / (2\pi R_{IN} C_{IN}) = 1 / (2\pi R1C1) \quad (7)$$

Bypass Capacitor

Bypass capacitor determines the time needed for setting ft4888 to quiescent operation and plays an important role in minimizing turn-on pops. The slower the output ramp to quiescent DC voltage ($0.5V_{DD}$ nominal), the smaller the turn-on pop is. The relationship between the capacitance and turn-on time is listed in the table below. In Figure 1, C6 is a 1.0μF bypass capacitor which, altogether with C1, minimizes the pops and clicks.

C6	T_{ON}
0.01μF	30ms
0.1μF	40ms
0.22μF	60ms
0.47μF	80ms
1.0μF	140ms

Besides the click and pop reduction function, the C6 connected between the BYPASS pin and the ground improves the internal bias voltage stability and amplifier PSRR.

Parametric Data

Absolute Maximum Ratings

Caution! The parameters provided in this table are the maximum values. Parameters exceeding these values may cause permanent damage to the device and the board.

Symbol	Parameters	Value
V_{DD}	Supply Voltage	6.0V
V_I	Input Voltage	−0.3V to V_{DD} +0.3V
	Power Dissipation	Internally Limited
	ESD Susceptibility	2000V
	ESD Susceptibility	200V
T_J	Junction Temperature	150°C
T_{stg}	Storage Temperature	−65°C to +150°C
Soldering Information		
	Small Outline Package	
	Vapor Phase (60 sec.)	215°C
	Infrared (15 sec.)	220°C
Thermal Resistance		
θ_{JC} (TYP)		3°C/W
θ_{JA} (TYP`)		42°C/W

Operation Ratings

Parameters	Value
Temperature Range $T_{MIN} \le T_A \le T_{MAX}$	-40°C ≤ T_A ≤ 85°C
Supply Voltage	2.7V ≤ V_{DD} ≤ 5.5V

Note: The following electrical characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. But note that specifications are not guaranteed for parameters where no limit is given. The typical value however, is a good indication of device performance. All voltages in the following tables are specified at 25°C which is generally taken as parametric norm. All measurements are taken from the application illustrated in Figure 3.

Electrical Characteristics (V_{DD} = 5V, T_A = 25°C)

Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
V_{DD}	Supply voltage			2.7	V(min)
				5.5	V(max)
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A (Note 10), BTL Load	6	10	mA(max)
		V_{IN} = 0V, I_O = 0A (Note 10), SE Load	3.0	6	mA(max)
I_{SD}	Shutdown Current	GND applied to the SHUTDOWN pin	0.04	2	μA (max)
V_{IH}	Headphone Sense High Input Voltage		3.7	4	V(min)
V_{IL}	Headphone Sense Low Input Voltage		2.6	0.8	V(max)
V_{IHSD}	Shutdown, Headphone micro, 3D control, High Input Voltage		1.2	1.4	V(min)
V_{ILSD}	Shutdown, Headphone micro, 3D control, Low Input Voltage		1	0.4	V(max)
T_{WU}	Turn On Time	1μF Bypass Cap (C6)	140		ms

Electrical Characteristics for Bridged-Mode Operation (V_{DD} = 5V, T_A = 25°C)

Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5	25	mV(max)
P_O	Output Power (Note 11)	THD + N = 1%, f = 1kHz (Note 12), R_L = 3Ω	2.4		W
		THD + N = 1%, f = 1kHz (Note 12), R_L = 4Ω	2.1		W
		THD + N = 1%, f = 1kHz (Note 12), R_L = 8Ω	1.3	1.0	W(min)
		THD + N = 10%, f = 1kHz (Note 12), R_L = 3Ω	3.0		W
		THD + N = 10%, f = 1kHz (Note 12), R_L = 4Ω	2.5		W
		THD + N = 10%, f = 1kHz (Note 12), R_L = 8Ω	1.7		W
THD+N	Total Harmonic Distortion + Noise	f = 1kHz, A_{VD} = 2, R_L = 4Ω, P_O = 1W	0.1		%
		f = 1kHz, A_{VD} = 2, R_L = 8Ω, P_O = 1W	0.06		%
PSRR	Power Supply Rejection Ratio	Input un-terminated, 217Hz, V_{ripple} = 200mV_{p-p}, C_6 = 1μF, R_L = 8Ω	85		dB
		Input un-terminated, 1kHz, V_{ripple} = 200mV_{p-p}, C_6 = 1μF, R_L = 8Ω	80		dB
		Input grounded, 217Hz, V_{ripple} = 200mV_{p-p}, C_6 = 1μF, R_L = 8Ω	65		dB
		Input grounded, 1kHz, V_{ripple} = 200mV_{p-p}, C_6 = 1μF, R_L = 8Ω	70		dB
X_{TALK}	Channel Separation	f = 1kHz, C_6 = 1μF, 3D Control = Low	82		dB
V_{NO}	Output Noise Voltage	1kHz, A-weighted	21		μV

Electrical Characteristics for Single-Ended Operation (V_{DD} = 5V, T_A = 25°C)

Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
P_O	Output Power	THD+N = 0.5%, f = 1kHz , R_L = 32Ω	90	75	mW(min)
THD+N	Total Harmonic Distortion + Noise	f = 1kHz, R_L = 32Ω, P_O = 20mW	0.015		%
PSRR	Power Supply Rejection Ratio	Input un-terminated, 217Hz, V_{ripple} = 200mV_{p-p}, C_6 = 1μF, R_L = 32Ω	70		dB
		Input un-terminated, 1kHz, V_{ripple} = 200mV_{p-p}, C_6 = 1μF, R_L = 32Ω	72		dB
		Input grounded, 217Hz, V_{ripple} = 200mV_{p-p}, C_6 = 1μF, R_L = 32Ω	65		dB
		Input grounded, 1kHz, V_{ripple} = 200mV_{p-p}, C_6 = 1μF, R_L = 32Ω	70		dB
X_{TALK}	Channel Separation	f = 1kHz, C_6 = 1μF, 3D Control = Low	80		dB
V_{NO}	Output Noise Voltage	1kHz, A-weighted	11		μV

Electrical Characteristics (V_{DD} = 3V, T_A = 25°C)

Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A (Note 10), BTL Load	4.5		mA
		V_{IN} = 0V, I_O = 0A (Note 10), SE Load	2.5		mA
I_{SD}	Shutdown Current	GND applied to the SHUTDOWN pin	0.01		μA (max)
V_{IH}	Headphone Sense High Input Voltage		2.2		V(min)
V_{IL}	Headphone Sense Low Input Voltage		1.5		V(max)
V_{IHSD}	Shutdown, Headphone micro, 3D control, High Input Voltage		1	1.4	V(min)
V_{ILSD}	Shutdown, Headphone micro, 3D control, Low Input Voltage		0.8	0.4	V(max)
T_{WU}	Turn On Time	1μF Bypass Cap (C6)	140		ms

Electrical Characteristics for Bridged-Mode Operation (V_{DD} = 3V, T_A = 25°C)

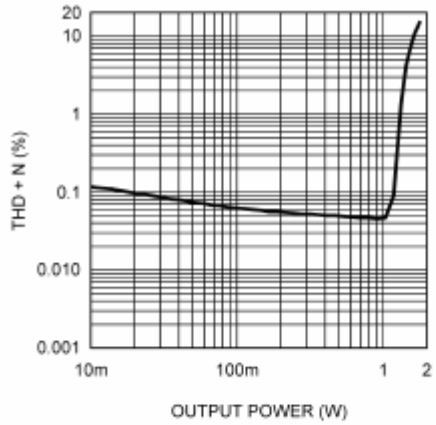
Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5		mV(max)
P_O	Output Power (Note 11)	THD + N = 1%, f = 1kHz (Note 12), R_L = 3Ω	0.82		W
		THD + N = 1%, f = 1kHz (Note 12), R_L = 4Ω	0.70		W
		THD + N = 1%, f = 1kHz (Note 12), R_L = 8Ω	0.43		W(min)
		THD + N = 10%, f = 1kHz (Note 12), R_L = 3Ω	1.0		W
		THD + N = 10%, f = 1kHz (Note 12), R_L = 4Ω	0.85		W
		THD + N = 10%, f = 1kHz (Note 12), R_L = 8Ω	0.53		W
THD+N	Total Harmonic Distortion + Noise	f = 1kHz, A_{VD} = 2, R_L = 4Ω, P_O = 1W	0.1		%
		f = 1kHz, A_{VD} = 2, R_L = 8Ω, P_O = 1W	0.05		%
PSRR	Power Supply Rejection Ratio	Input un-terminated, 217Hz, V_{ripple} = 200mV_{p-p}, C_6 = 1μF, R_L = 8Ω	90		dB
		Input un-terminated, 1kHz, V_{ripple} = 200mV_{p-p}, C_6 = 1μF, R_L = 8Ω	80		dB
		Input grounded, 217Hz, V_{ripple} = 200mV_{p-p}, C_6 = 1μF, R_L = 8Ω	65		dB
		Input grounded, 1kHz, V_{ripple} = 200mV_{p-p}, C_6 = 1μF, R_L = 8Ω	73		dB
X_{TALK}	Channel Separation	f = 1kHz, C_6 = 1μF, 3D Control = Low	85		dB
V_{NO}	Output Noise Voltage	1kHz, A-weighted	21		μV

Electrical Characteristics for Single-Ended Operation (V_{DD} = 3V, T_A = 25°C)

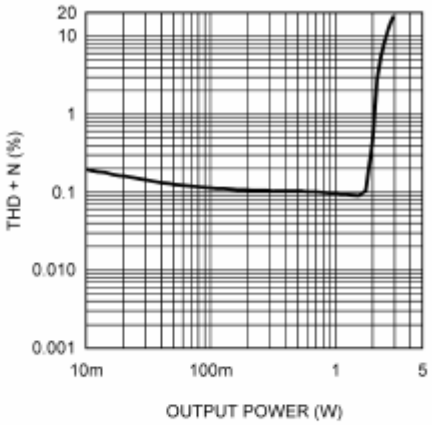
Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
P_O	Output Power	THD+N = 0.5%, f = 1kHz , R_L = 32Ω	35		mW(min)
THD+N	Total Harmonic Distortion + Noise	f = 1kHz, R_L = 32Ω, P_O = 25 mW	0.015		%
PSRR	Power Supply Rejection Ratio	Input un-terminated, 217Hz, V_{ripple} = 200mV_{p-p}, C_6 = 1μF, R_L = 32Ω	71		dB
		Input un-terminated, 1kHz, V_{ripple} = 200mV_{p-p}, C_6 = 1μF, R_L = 32Ω	79		dB
		Input grounded, 217Hz, V_{ripple} = 200mV_{p-p}, C_6 = 1μF, R_L = 32Ω	65		dB
		Input grounded, 1kHz, V_{ripple} = 200mV_{p-p}, C_6 = 1μF, R_L = 32Ω	72		dB
X_{TALK}	Channel Separation	f = 1kHz, C_6 = 1μF, 3D Control = Low	80		dB
V_{NO}	Output Noise Voltage	1kHz, A-weighted	11		μV

Typical Performance Characteristics

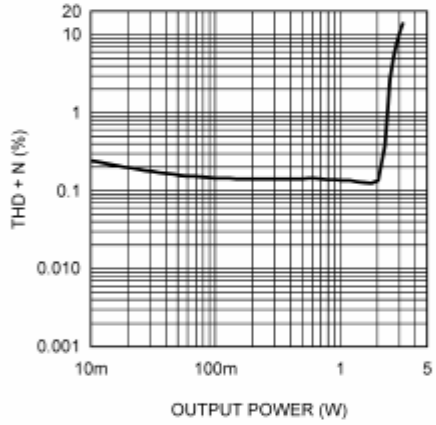
THD+N vs Output Power
5V, 8Ω, BTL at 1kHz



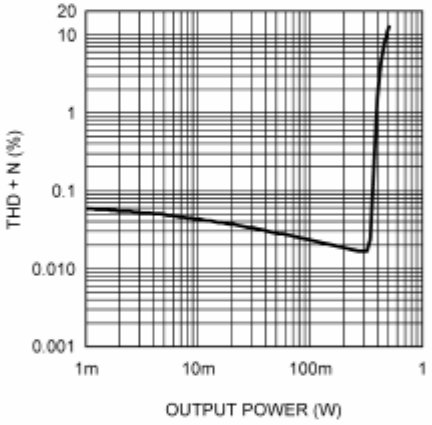
THD+N vs Output Power
5V, 4Ω, BTL at 1kHz



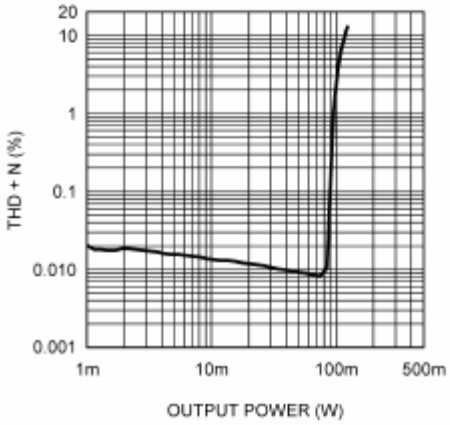
THD+N vs Output Power
5V, 3Ω, BTL at 1kHz



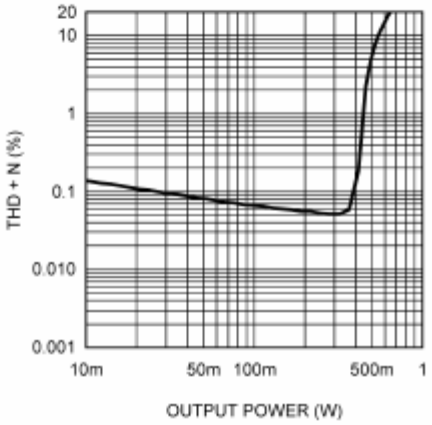
THD+N vs Output Power
5V, 32Ω, BTL at 1kHz



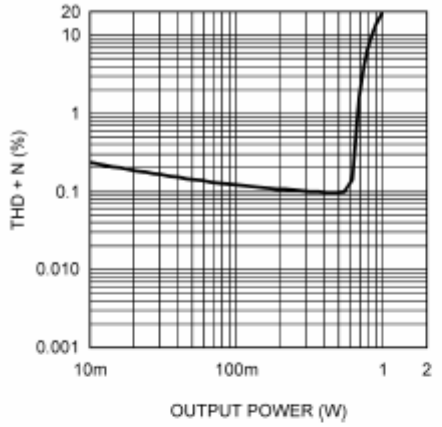
THD+N vs Output Power
5V, 32Ω, SE at 1kHz



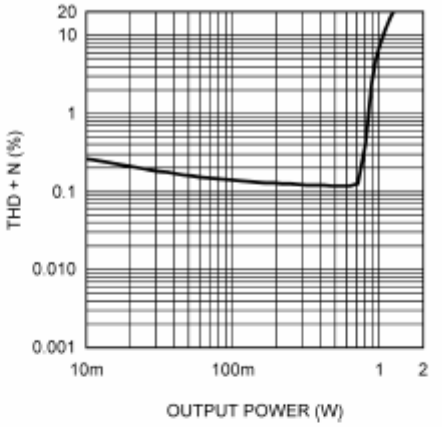
THD+N vs Output Power
3V, 8Ω, BTL at 1kHz



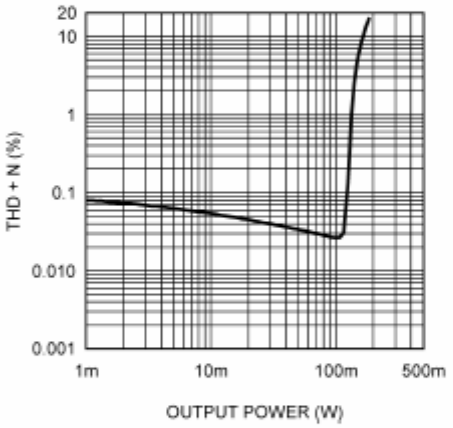
THD+N vs Output Power
3V, 4Ω, BTL at 1kHz



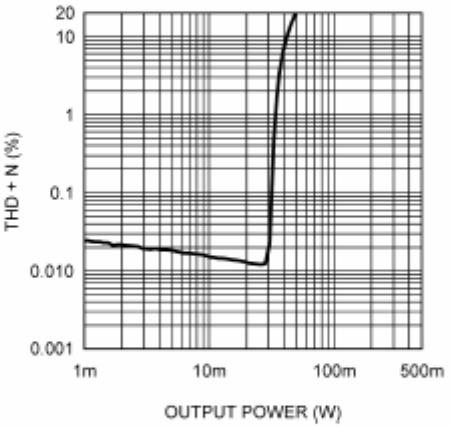
THD+N vs Output Power
3V, 3Ω, BTL at 1kHz



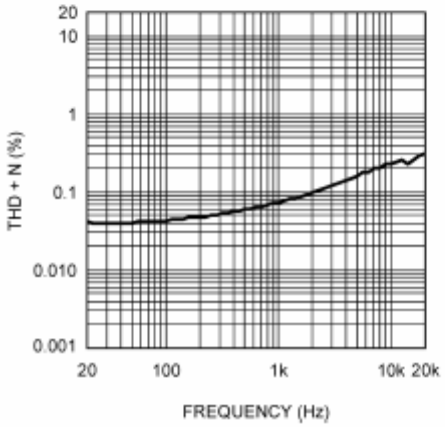
THD+N vs Output Power
3V, 32Ω, BTL at 1kHz



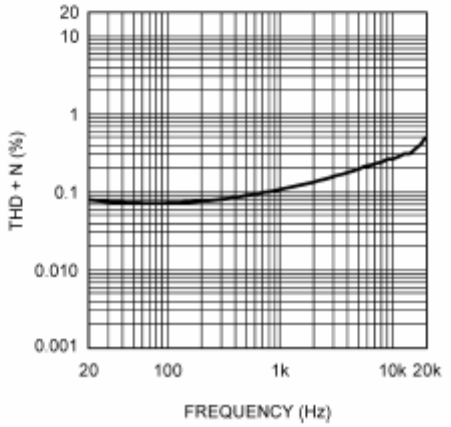
THD+N vs Output Power
3V, 32Ω, SE at 1kHz



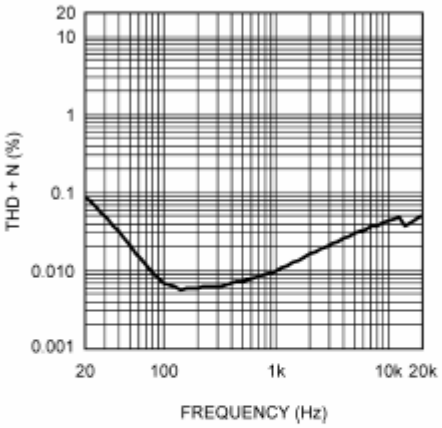
THD+N vs Frequency
5V, 8Ω, BTL at 400mW



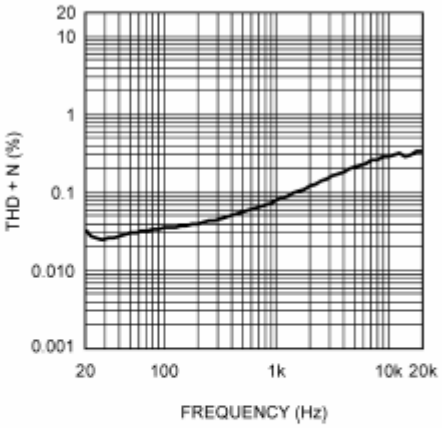
THD+N vs Frequency
5V, 4Ω, BTL at 1W



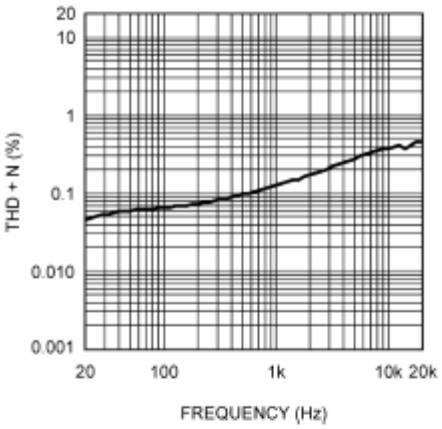
THD+N vs Frequency
5V, 32Ω, SE at 75mW



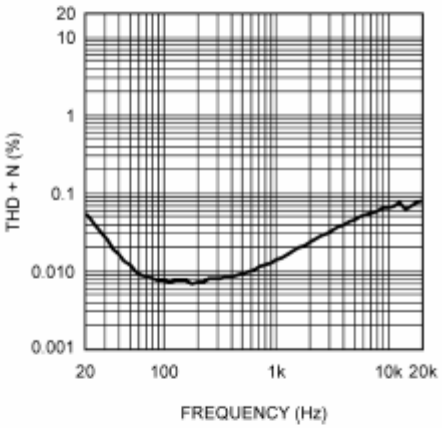
THD+N vs Frequency
3V, 8Ω, BTL at 150mW



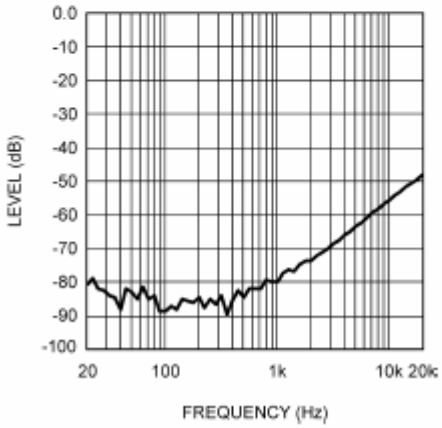
THD+N vs Frequency
3V, 4Ω, BTL at 250mW



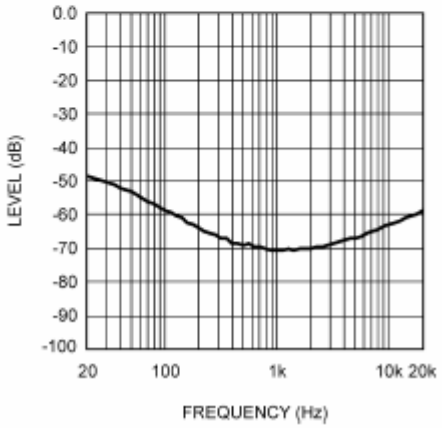
THD+N vs Frequency
3V, 32Ω, SE at 25mW



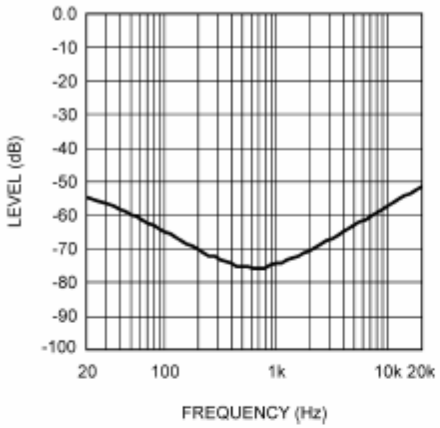
PSRR
5V, 8Ω, BTL, Input Unterminated



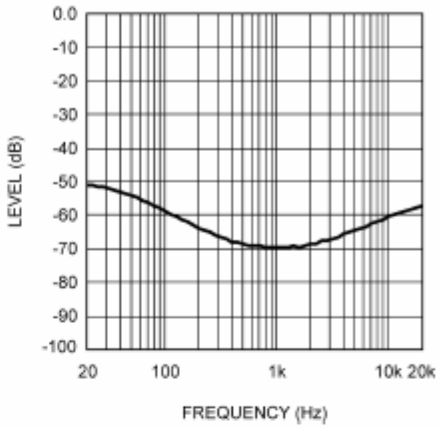
PSRR
5V, 8Ω, BTL, Input Terminated



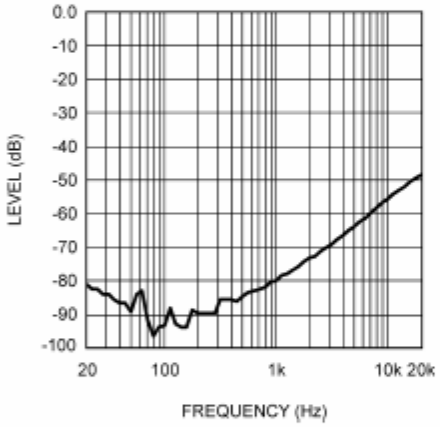
PSRR
5V, 32Ω, SE, Input Unterminated



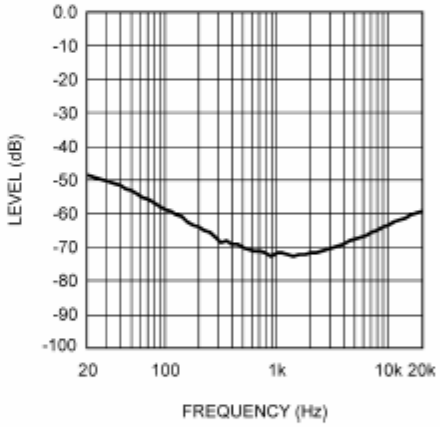
PSRR
5V, 32Ω, SE, Input Terminated



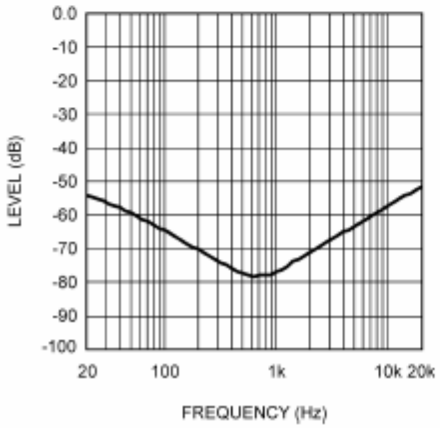
PSRR
3V, 8Ω, BTL, Input Unterminated



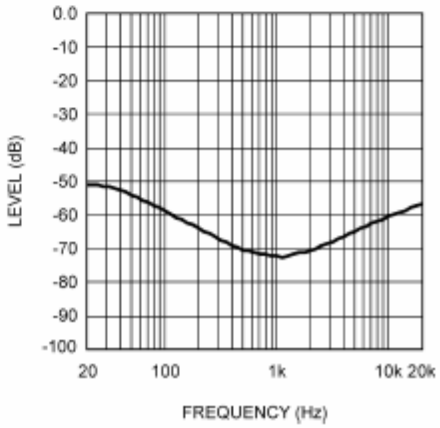
PSRR
3V, 8Ω, BTL, Input Terminated



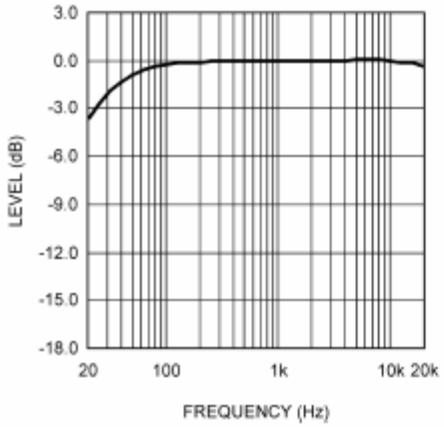
PSRR
3V, 32Ω, SE, Input Unterminated



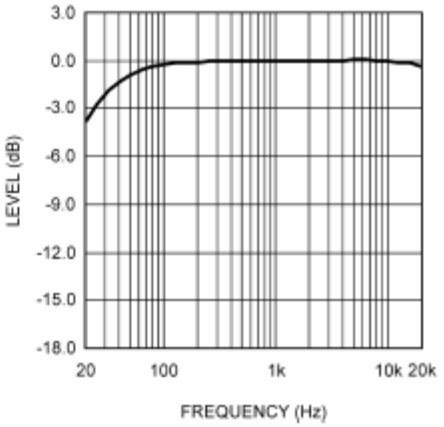
PSRR
3V, 32Ω, SE, Input Terminated



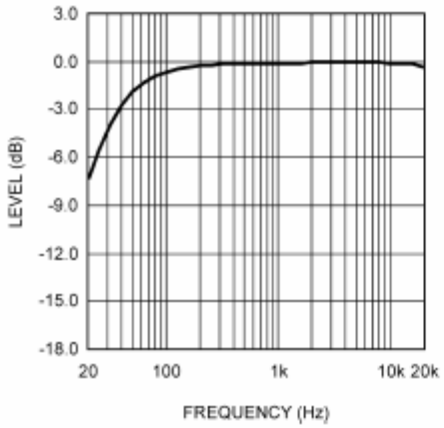
Frequency Response
5V, 8Ω, BTL



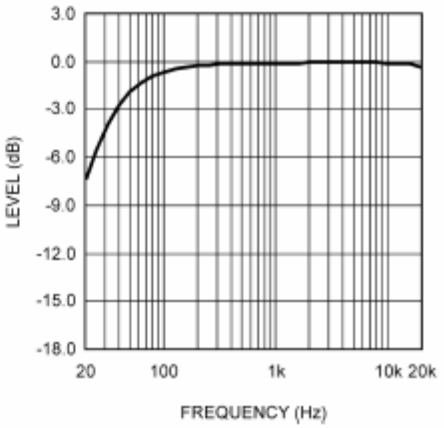
Frequency Response
3V, 8Ω, BTL



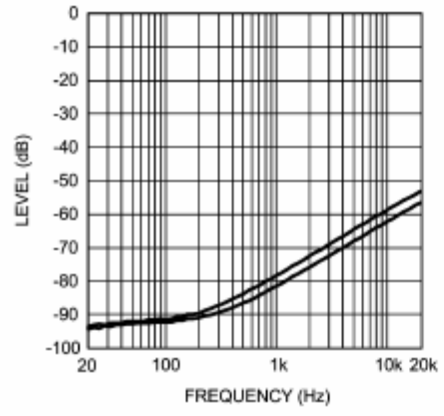
Frequency Response
5V, 32Ω, SE



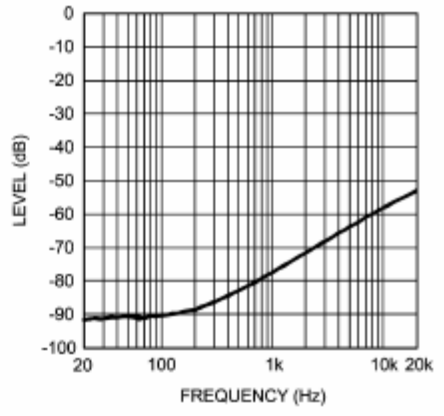
Frequency Response
3V, 32Ω, SE



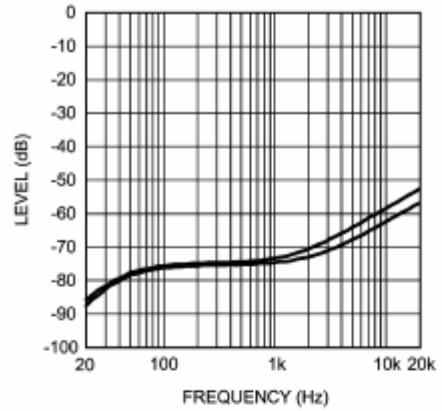
Crosstalk
5V, 8Ω, BTL



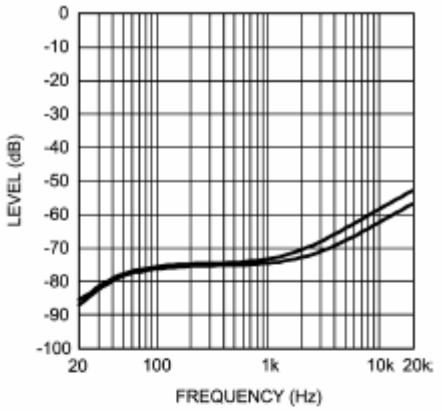
Crosstalk
3V, 8Ω, BTL



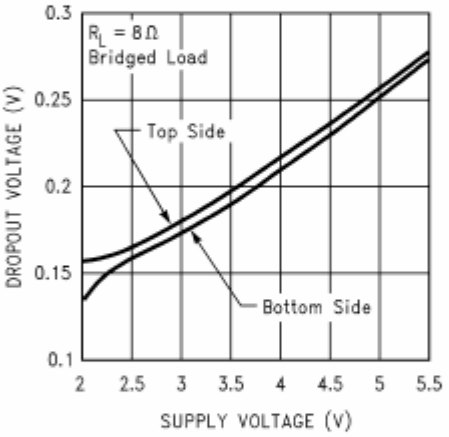
Crosstalk
3V, 32Ω, SE



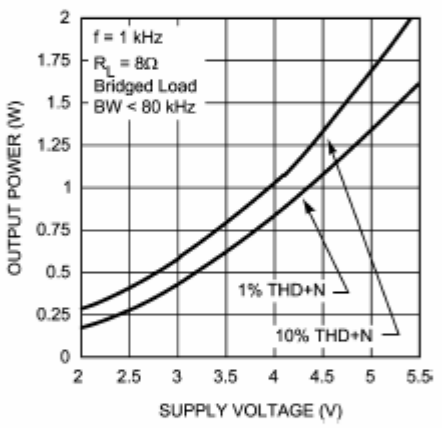
Crosstalk
5V, 32Ω, SE



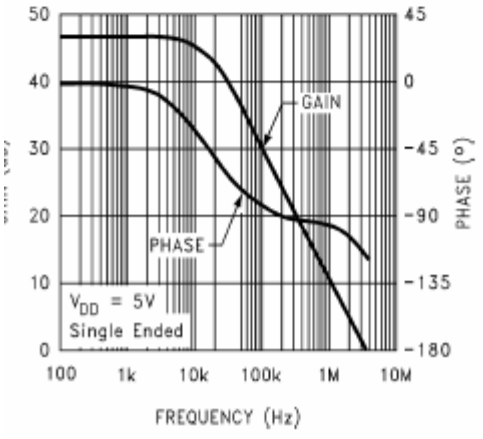
Dropout Voltage vs
Supply Voltage



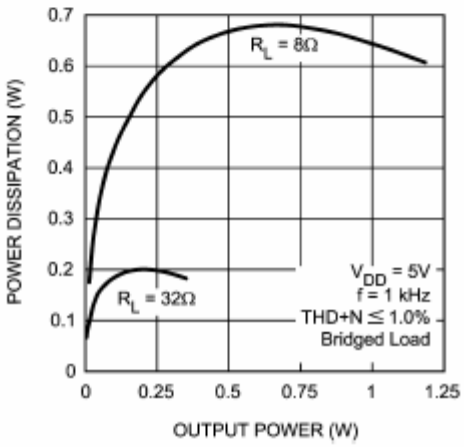
Output Power vs
Supply Voltage



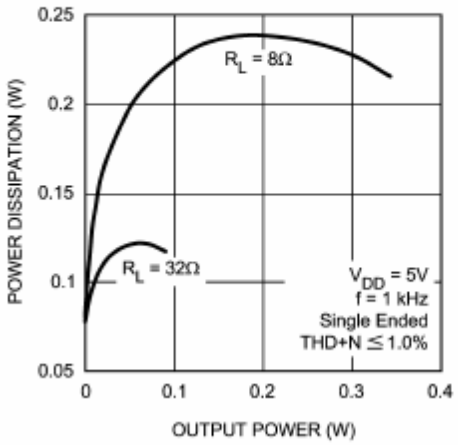
Open Loop
Frequency Response



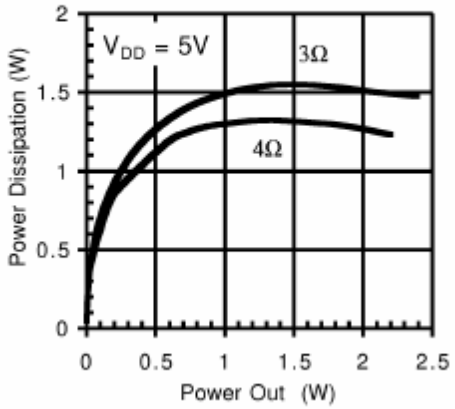
Power Dissipation vs
Output Power



Power Dissipation vs Output Power



Power Dissipation vs Output Power Single Channel, f = 1kHz, THD+N ≤ 1.0%, BW < 80kHz



Power Derating Curve