# BF6511AC2

**2.5W Mono Filter-Free Class-D Audio Power Amplifier**

**BYD Microelectronics Co., Ltd.**

## GENERAL DESCRIPTION

The BF6511AC2 is a 2.5W high efficiency, filter-free, mono, class-D audio power amplifier (class-D amp) in a 1.48 mm×1.48 mm wafer chip scale package (WCSP). A frequency jittering technology and optimized PWM architecture reduces EMI and eliminates the output filter, reducing external component count, board area consumption, system cost, and simplifying design.

Features like 88% efficiency, –78dB PSRR, improved RF-rectification immunity, and small total PCB area make the BF6511AC2 class-D amp ideal for cellular handsets. A fast start-up time of 1mS with minimal pop makes the BF6511AC2 ideal for PDA applications.

The BF6511AC2 features a low-power consumption shutdown mode. Shutdown may be enabled by driving the Shutdown pin to a logic low (GND).

The BF6511AC2 allows independent gain while summing input signals from separate sources. Output short circuit and thermal overload protection prevent the device from damage during fault conditions. Under voltage protection is available when the supply voltage is too low.

## FEATURES

- Frequency jittering technology reduces EMI
- ESD susceptibility is over 3.5kV in human body mode
- Efficiency with an $8\Omega$ speaker:
  88% at 3.6V, 400 mW
  80% at 3.6V, 100 mW
  88% at 5V, 1 W
- 2.9mA quiescent current at 3.6V power supply voltage and 0.2µA shutdown current
- Optimized PWM output stage eliminates LC output filter
- Improved PSRR (–78 dB) and wide supply voltage (2.5 V to 5.5 V) eliminates need for a voltage regulator
- Fully differential design eliminates bypass capacitor
- Improved CMRR eliminates two input coupling capacitors
- "Click and pop" suppression circuitry
- Fast start-up time of 1mS
- Wafer chip scale packaging (WCSP-9)

## APPLICATIONS

- Wireless or Cellular Handsets
- PDAs
- Portable electronic devices
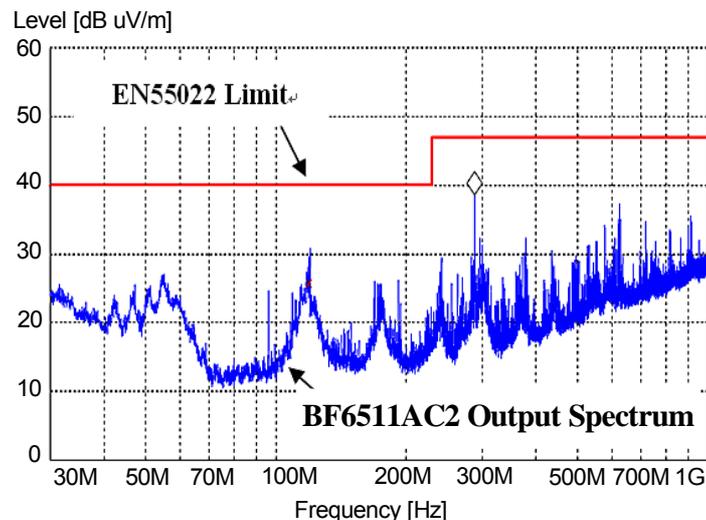


BF6511AC2 EMI Emissions

# TYPICAL APPLICATION
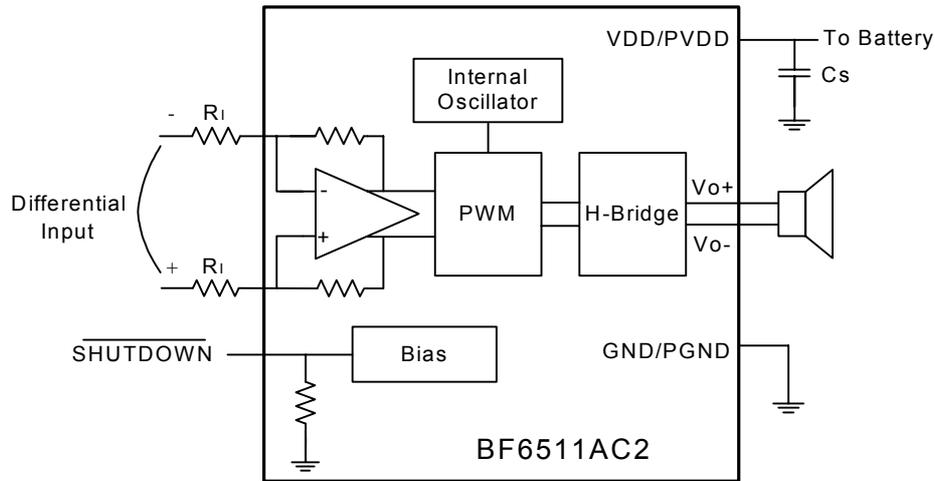


# PIN CONFIGURATION
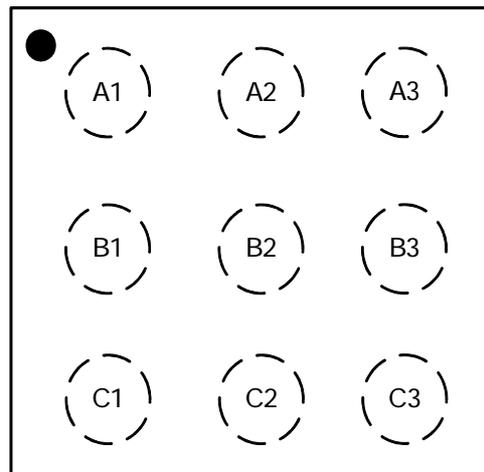


TOP VIEW

| PIN | NAME | I/O | DESCRIPTION |
|-----|------|-----|-------------|
| A1 | IN+ | I | Positive differential input |
| A2 | GND | I | High-current ground |
| A3 | VO- | O | Negative BTL output |
| B1 | VDD | I | Power supply |
| B2 | PVDD | I | Power supply |
| B3 | PGND | I | Power ground |
| C1 | IN- | I | Negative differential input |
| C2 | $\overline{\text{SHUTDOWN}}$ | I | Shutdown terminal (active low logic) |
| C3 | VO+ | O | Positive BTL output |

# FUNCTIONAL BLOCK DIAGRAM
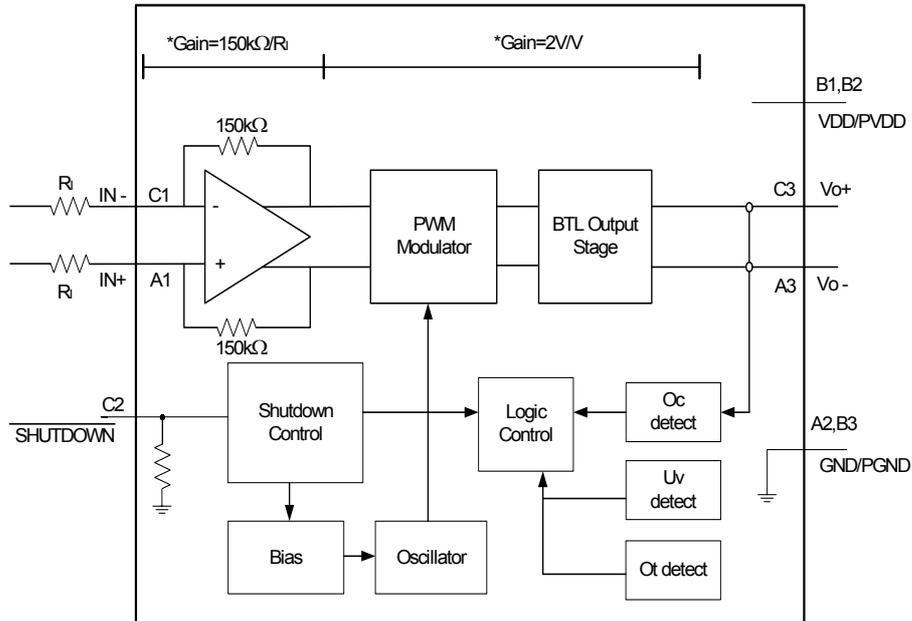


Notes: Total gain =2*150 k$\Omega$/R$_l$
Oc: Over Current
Uv: Under Voltage
Ot: Over Temperature

# ORDERING INFORMATION

| Orderable Device | Package Type | Package Qty | Marking[Note] | Operating Temperature range T$_A$ |
|---|---|---|---|---|
| BF6511AC2 | WCSP-9 Pb-Free (RoHS) | 3000 | AAB YWD | -40~85 |

Note:  Y  =Year
W  =Week
D  =Day

# ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

| PARAMETER | RANGE |
|---|---|
| VDD/PVDD        Supply Voltage | -0.3V to 6.0V |
| $V_I$               Input Voltage | -0.3V to VDD+0.3V |
| Power Dissipation(Note1) | Internally Limited |
| ESD Susceptibility, all other pins(Note2) | 3.5kV |
| $T_J$               Operating Junction Temperature | -40℃ to 125℃ |
| $T_{stg}$            Storage Temperature | -65℃ to 150℃ |
| Lead temperature 1,6 mm(1/16 inch) from case for 10 seconds | 245℃ |
| $\Theta_{JA}$              Thermal Resistance(Note 3) | 90℃/W |

Note1: The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{JMAX}$, $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX}–T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the BF6511AC2, $T_{JMAX}$ = 150°C.The typical $\theta_{JA}$ is 90°C/W for the WCSP package.

Note2: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note3: For the 9-Pin WCSP package, the $\theta_{JA}$ is highly dependent of the PCB Heatsink area. For example, $\theta_{JA}$ can equal 195°C/W with 50 mm$^2$ total area and also 135°C/W with 500 mm$^2$. When using ground and power planes, the value is around 90°C/W.

# OPERATING RATINGS

| PARAMETER | RANGE |
|---|---|
| VDD/PVDD        Supply Voltage | 2.5V to 5.5V |
| $T_A$               Operating Free-air Temperature | -40    to 85 |

# RECOMMENDED OPERATING CONDITIONS

| | PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage, the chip woks | VDD=2.5V~5.5V | 1.4 | | VDD | V |
| $V_{IL}$ | Low-level input voltage, the chip is shut-down | VDD=2.5V~5.5V | 0 | | 0.4 | V |
| $R_I$ | Input resistor | Gain $\leq$ 20 V/V (26 dB) | 15 | 150 | | k$\Omega$ |
| $V_{IC}$ | Common mode input voltage range | VDD = 2.5 V~ 5.5 V, CMRR $\leq$ –49 dB | 1.5 | | VDD-0.8 | V |

# ELECTRICAL CHARACTERISTICS

($T_A$ = 25°C,unless otherwise noted)

| | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $|V_{OS}|$ | Output offset voltage (measured differentially) | $V_I$ = 0 V, $A_V$ = 2 V/V, VDD = 2.5 V ~ 5.5 V | | 2 | 25 | mV |
| PSRR | Power supply rejection ratio | VDD = 2.5 V~ 5.5 V | | -78 | -55 | dB |
| CMRR | Common mode rejection ratio | VDD =2.5V ~5.5V, $V_{IC}$= VDD/2 ~ 0.5 V, $V_{IC}$= VDD/2 ~ VDD-8 | | -68 | -49 | dB |
| $|I_{IH}|$ | High-level input current | VDD = 5.5 V, $V_I$ = 5.8 V | | | 100 | μA |
| $|I_{IL}|$ | Low-level input current | VDD = 5.5 V, $V_I$ = –0.3 V | | | 5 | μA |
| $I_{(Q)}$ | Quiescent current | VDD = 5.5 V, no load | | 3.8 | 5 | mA |
| | | VDD = 3.6 V, no load | | 2.9 | 4 | |
| | | VDD = 2.5 V, no load | | 2.4 | 3.2 | |
| $I_{(SD)}$ | Shutdown current | $V_{(SHUTDOWN)}$ = 0.35 V, VDD = 2.5 V~5.5 V | | 0.2 | 2 | μA |
| $r_{DS(on)}$ | Static drain-source on-state resistance | VDD = 2.5 V | | 500 | | m$\Omega$ |
| | | VDD =3.6 V | | 400 | | |
| | | VDD =5.5 V | | 300 | | |
| | Output impedance in SHUTDOWN | $V_{(SHUTDOWN)}$= 0.4 V | | >1 | | k$\Omega$ |
| $f_{(sw)}$ | Switching frequency | VDD = 2.5 V~5.5 V | 180 | | 330 | kHz |
| GAIN | | VDD = 2.5 V~5.5 V | 215k$\Omega$ /$R_I$ | 300k$\Omega$ /$R_I$ | 315k$\Omega$ /$R_I$ | V/V |
| | Resistance from shutdown to GND | | | 300 | | k$\Omega$ |

# OPERATING CHARACTERISTICS

($T_A$ = 25°C, Gain=2V/V,RL=8$\Omega$,unless otherwise noted)

| PARAMETER | | TEST CONDITION | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| PO | Output power | THD + N = 10%, f = 1 kHz, RL = 4 $\Omega$ | VDD = 5 V | | 2.96 | | W |
| | | | VDD = 3.6 V | | 1.5 | | |
| | | | VDD = 2.5 V | | 0.68 | | |
| | | THD + N = 1%, f = 1 kHz, RL = 4 $\Omega$ | VDD = 5 V | | 2.4 | | |
| | | | VDD = 3.6 V | | 1.23 | | |
| | | | VDD = 2.5 V | | 0.56 | | |
| | | THD + N = 10%, f = 1 kHz, RL = 8$\Omega$ | VDD = 5 V | | 1.7 | | |
| | | | VDD = 3.6 V | | 0.88 | | |
| | | | VDD = 2.5 V | | 0.4 | | |
| | | THD + N = 1%, f = 1 kHz, RL = 8$\Omega$ | VDD = 5 V | | 1.4 | | |
| | | | VDD = 3.6 V | | 0.71 | | |
| | | | VDD = 2.5 V | | 0.33 | | |
| THD+N | Total harmonic distortion plus noise | VDD = 5 V, PO = 1 W, RL = 8 $\Omega$, f = 1 kHz | | | 0.25 | | % |
| | | VDD = 3.6 V, PO = 0.5 W, RL = 8 $\Omega$, f = 1 kHz | | | 0.23 | | |
| | | VDD = 2.5 V, PO = 200 mW, RL = 8 $\Omega$, f = 1 kHz | | | 0.15 | | |
| $k_{SVR}$ | Supply ripple rejection ratio | VDD=3.6V, Inputs ac -grounded with $C_I$=2µF f=217 Hz, $V_{(RIPPLE)}$=200mVpp | | | -64 | | dB |
| SNR | Signal-to-noise ratio | VDD = 5 V, PO = 1 W, RL = 8 $\Omega$ | | | 90 | | dB |
| Vn | Output voltage noise | VDD=3.6V,f=20Hz to 20kHz,Inputs ac-grounded with $C_I$=2µF | No weighting | | 160 | | uV$_{RMS}$ |
| | | | A weighting | | 100 | | |
| CMRR | Common mode rejection ratio | VDD = 3.6 V, VIC = 1 Vpp   f = 217 Hz | | | -68 | | dB |
| $Z_I$ | Input impedance | | | 125 | 150 | 175 | k$\Omega$ |
| Start-up time from shutdown | | VDD = 3.6 V | | | 1 | | mS |

# TYPICAL PERFORMANCE CHARACTERISTICS

($T_A$ = 25°C, unless otherwise noted)

**Efficiency vs Output Power**

VDD=3.6V RL=8Ohm,33uH

VDD=2.5V RL=8Ohm,33uH

VDD=5V RL=8Ohm,33uH

**Efficiency vs Output Power**

VDD=3.6V RL=4Ohm,33uH

VDD=2.5V RL=4Ohm,33uH

VDD=5V RL=4Ohm,33uH

**Power Disspation vs Output Power**

VDD=5V RL=4Ohm,33uH

VDD=5V RL=8Ohm,33uH

**Power Disspation vs Output Power**

VDD=3.6V RL=4Ohm,33uH

VDD=3.6V RL=8Ohm,33uH

**Supply Current vs Output Power**

RL=4Ohm,33uH

VDD=2.5V

VDD=3.6V

VDD=5V

**Supply Current vs Output Power**

RL=8Ohm,33uH

VDD=2.5V

VDD=3.6V

VDD=5V

**Supply Current vs Supply Voltage**
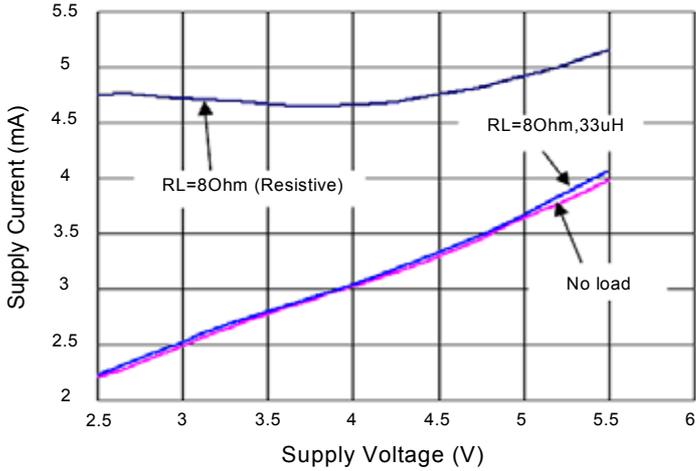
**Supply Current vs Output Power**
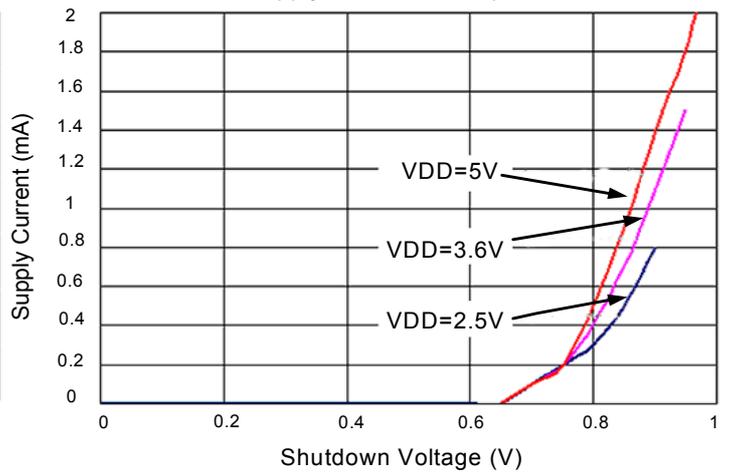
**Output Power vs Load Resistance**
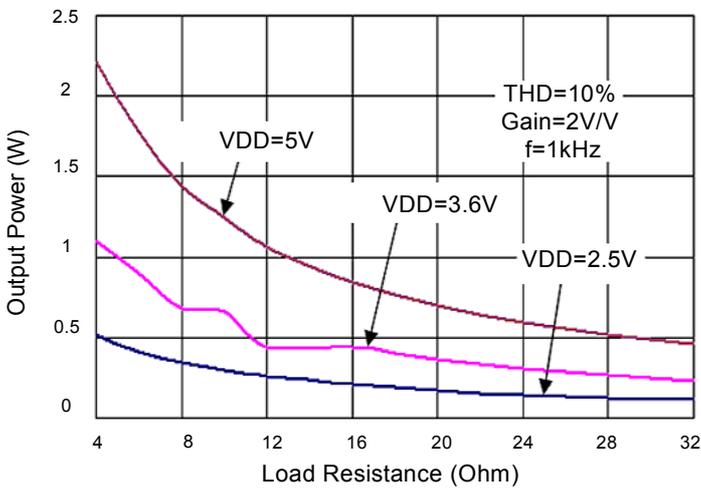
**Output Power vs Load Resistance**
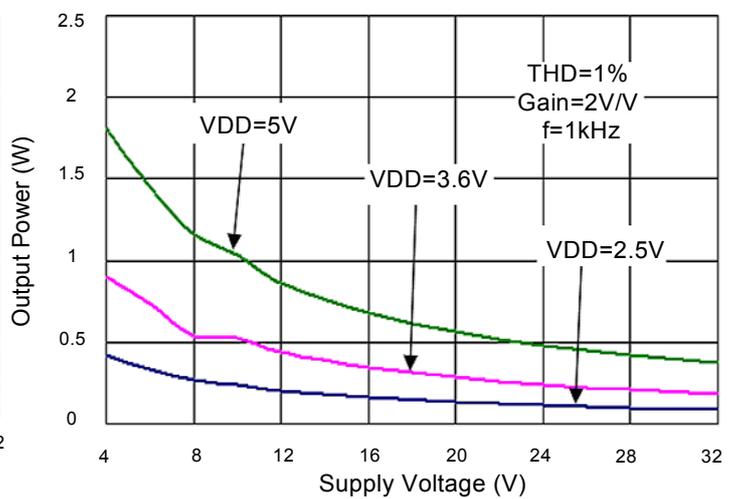
**Output Power vs Supply Voltage**
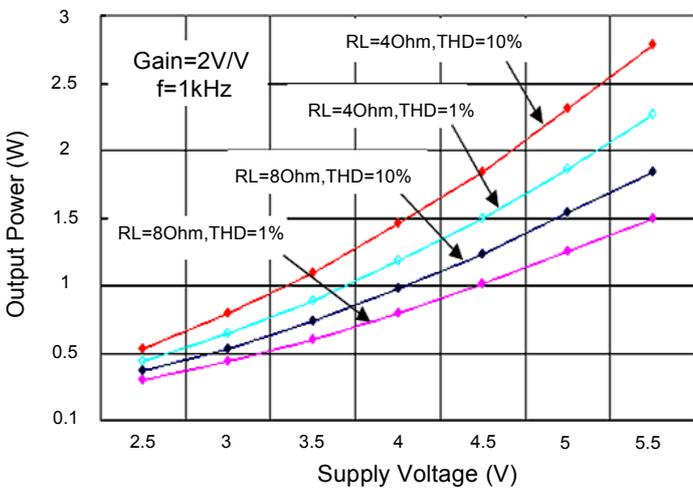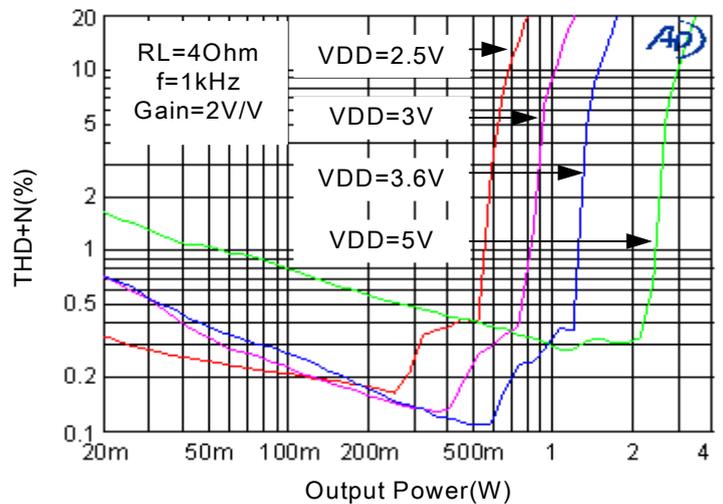
**THD+N vs Output Power**

## THD+N vs Output Power
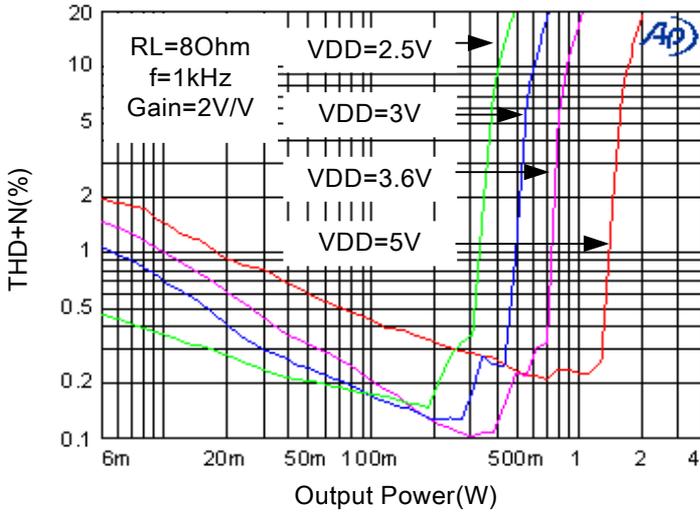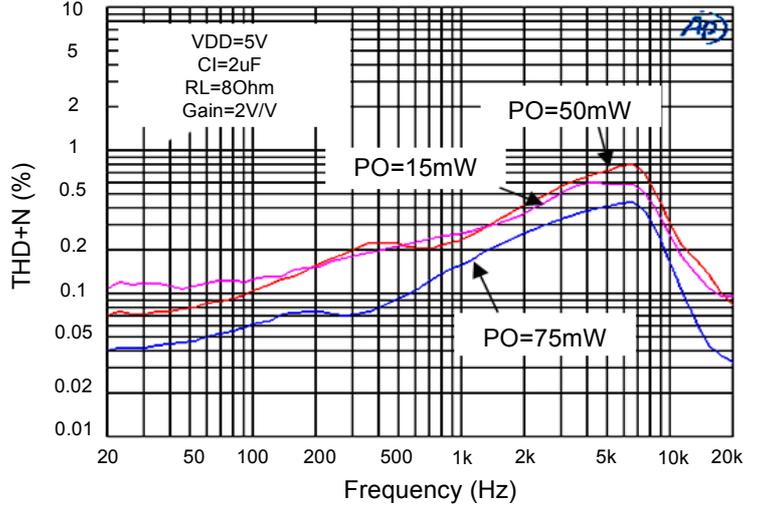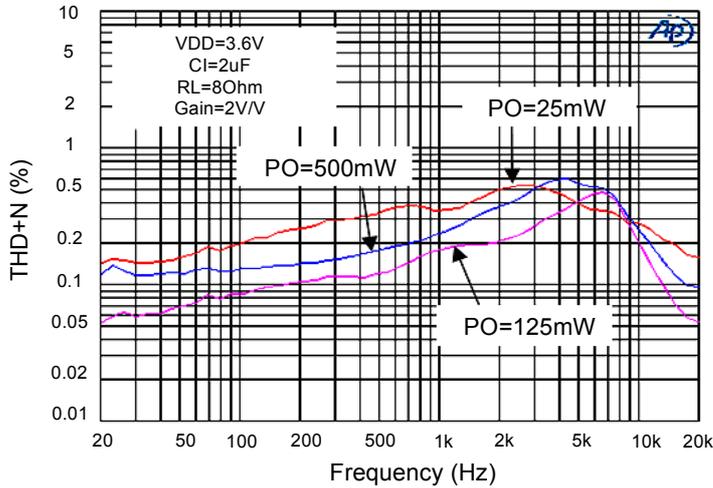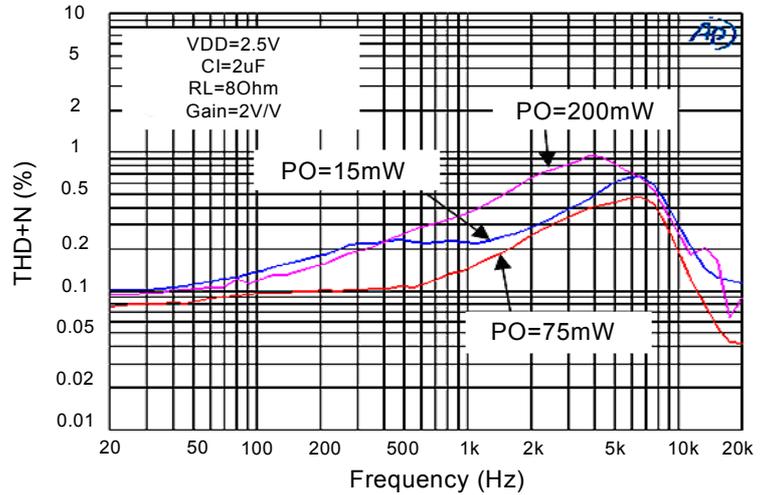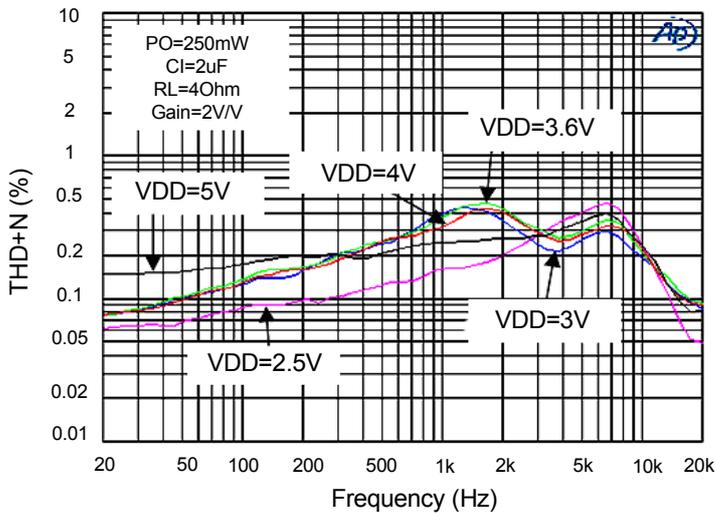
RL=8Ohm
f=1kHz
Gain=2V/V

VDD=2.5V
VDD=3V
VDD=3.6V
VDD=5V

## THD+N vs Frequency

VDD=5V
CI=2uF
RL=8Ohm
Gain=2V/V

PO=50mW
PO=15mW
PO=75mW

## THD+N vs Frequency

VDD=3.6V
CI=2uF
RL=8Ohm
Gain=2V/V

PO=25mW
PO=500mW
PO=125mW

## THD+N vs Frequency

VDD=2.5V
CI=2uF
RL=8Ohm
Gain=2V/V

PO=200mW
PO=15mW
PO=75mW

## THD+N vs Frequency

PO=250mW
CI=2uF
RL=4Ohm
Gain=2V/V

VDD=3.6V
VDD=4V
VDD=5V
VDD=3V
VDD=2.5V

## Supply Ripple Rejection Ratio vs Frequency

Input AC-grounded
CI=2uF
RL=8Ohm
Gain=2V/V

VDD=2.5V
VDD=3.6V
VDD=5V

### Supply Ripple Rejection Ratio vs Frequency

Input AC-grounded
CI=2uF
RL=4Ohm
Gain=2V/V

VDD=2.5V

VDD=3.6V

VDD=5V

### Supply Ripple Rejection Ratio vs Frequency

Input floating
RL=8Ohm

VDD=2.5V

VDD=3.6V

VDD=5V

### CMRR vs Frequency

VDD=3.6V
VIC=200mV
RL=8Ohm
Gain=2V/V
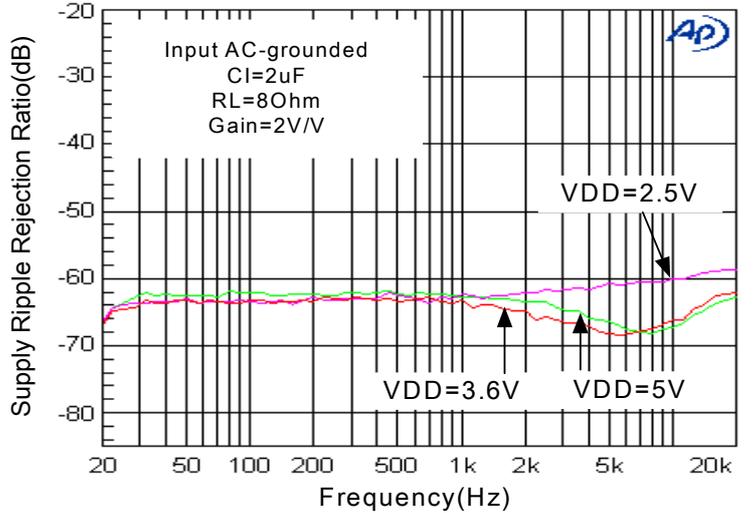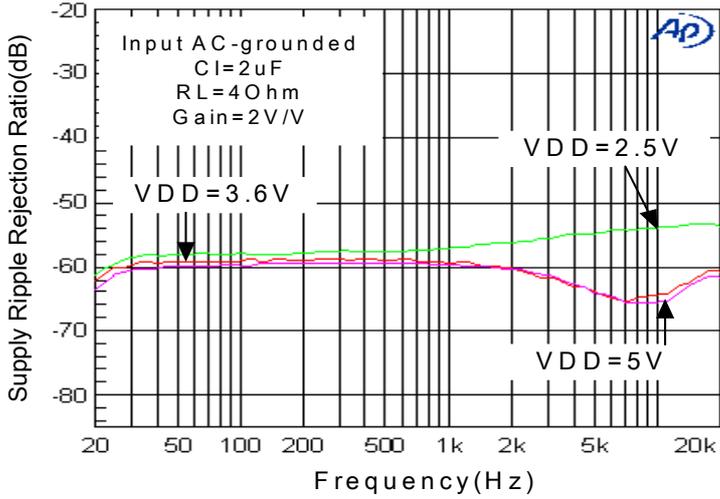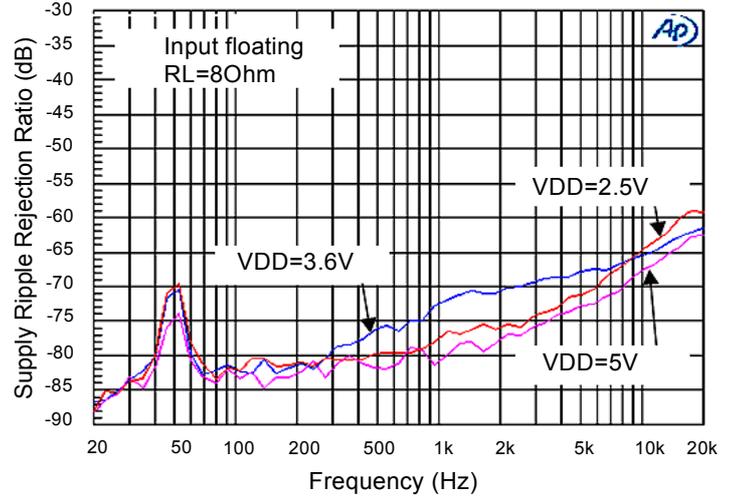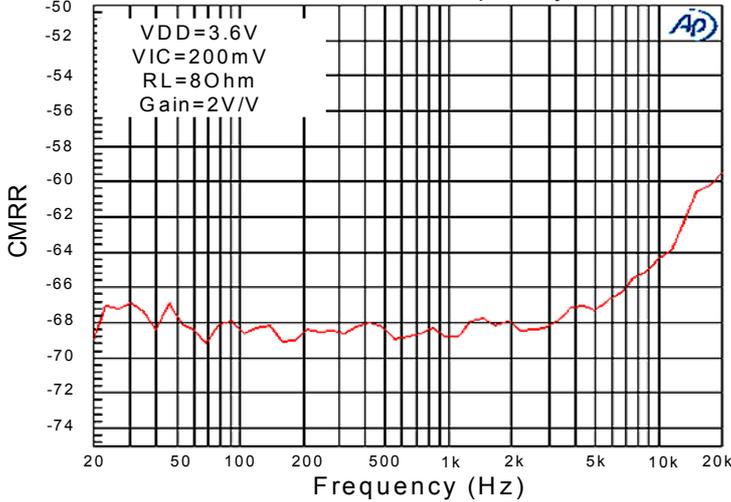
### CMRR vs Common Mode Input Voltage

VDD=2.5V

VDD=3.6V

VDD=5V
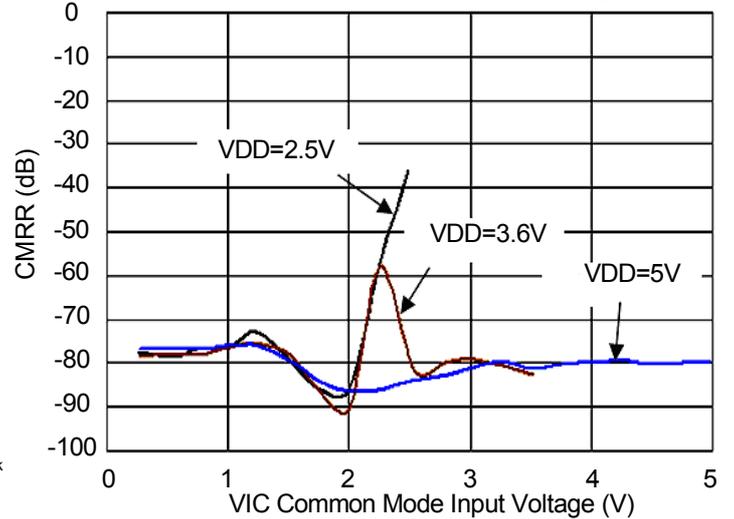
### Supply Ripple Rejection Ratio vs DC Common Mode Voltage

VDD=2.5V

VDD=3.6V

VDD=5V

GSM Power Supply Rejection vs Frequency



VDD
200mV/div

High - 3.6V
Amp - 512mV
Duty - 88%

VOUT
2mV/div

t (2ms/div)

GSM Power Supply Rejection vs Frequency



VDD in the left figure
CI=2uF
Gain=2V/V
Inputs AC-grounded

Frequency (Hz)
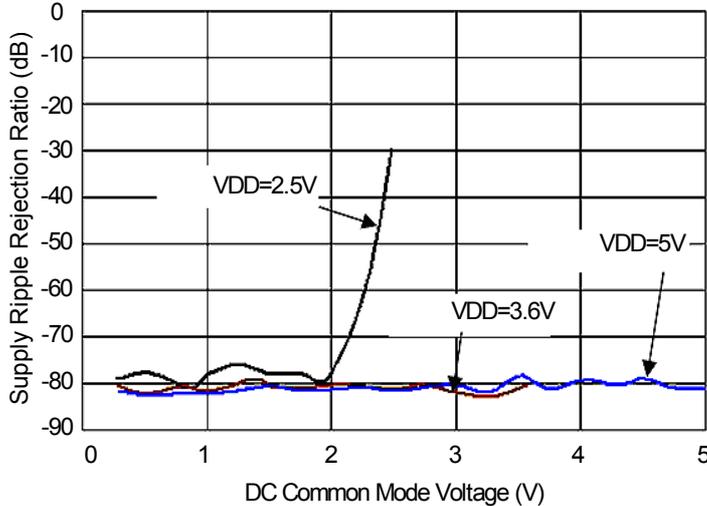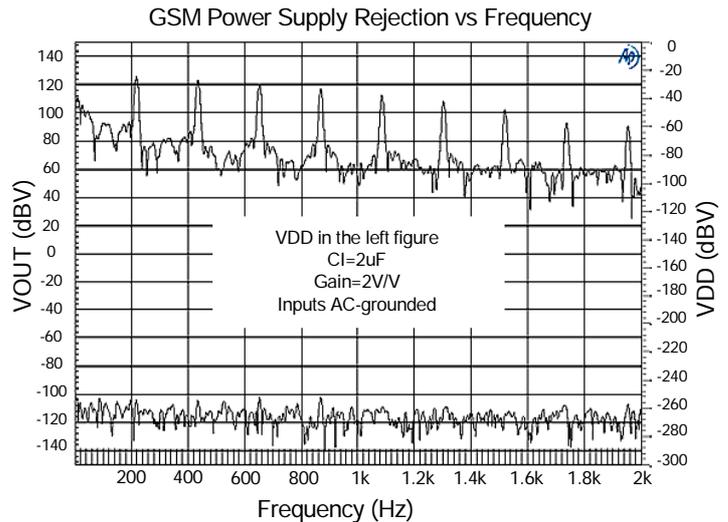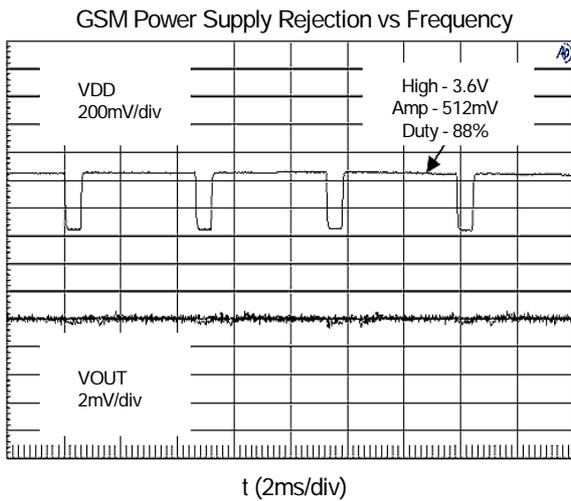
# APPLICATION INFORMATION

### FULLY DIFFERENTIAL AMPLIFIER

The BF6511AC2 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around VDD/2 regardless of the common-mode voltage at the input. The fully differential BF6511AC2 can still be used with a single-ended input; however, the BF6511AC2 should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

### ADVANTAGES OF FULLY DIFFERENTIAL AMPLIFIERS

Input-coupling capacitors not required: a fully differential amplifier allows the inputs to be biased at voltage other than mid-supply. For example, if a codec has a midsupply lower than the midsupply of the BF6511AC2, the common-mode feedback circuit will adjust, and the BF6511AC2 outputs will still be biased at midsupply of the BF6511AC2. The inputs of the BF6511AC2 can be biased from 0.5 V to VDD–0.8 V. If the inputs are biased outside of that range, input-coupling capacitors are required.

Midsupply bypass capacitor, $C_{(BYPASS)}$, not required: The fully differential amplifier does not require a bypass capacitor. This is because any shift in the midsupply affects both positive and negative channels equally and cancels at the differential output.

Better RF-immunity: GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217 Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier.

### FREQUENCY JITTERING MODULATION

The BF6511AC2 features a fitlerless frequency jittering modulation scheme that eliminates the need for output filters, ferrite beads or chokes. The switching frequency varies from 180 kHz to 330 kHz, reducing the wideband spectral contend, improving EMI emissions radiated by the speaker and associated cables

and traces. Where a fixed frequency class D exhibits large amounts of spectral energy at multiples of the switching frequency, the frequency jittering architecture of the BF6511AC2 spreads that energy over a larger bandwidth. The cycle-to-cycle variation of the switching period does not affect the audio reproduction of efficiency. The EMI emissions of BF6511AC2 is tested in the measurement conditions of European Standard EN 55022, with output cable area of 1100mm*5.04mm.

## COMPONENT SELECTION

Figure 1 shows the BF6511AC2 typical schematic with differential inputs and Figure 2 shows the BF6511AC2 with differential inputs and input capacitors, and Figure 3 shows the BF6511AC2 with single-ended inputs. Differential inputs should be used whenever possible because the single-ended inputs are much more susceptible to noise.
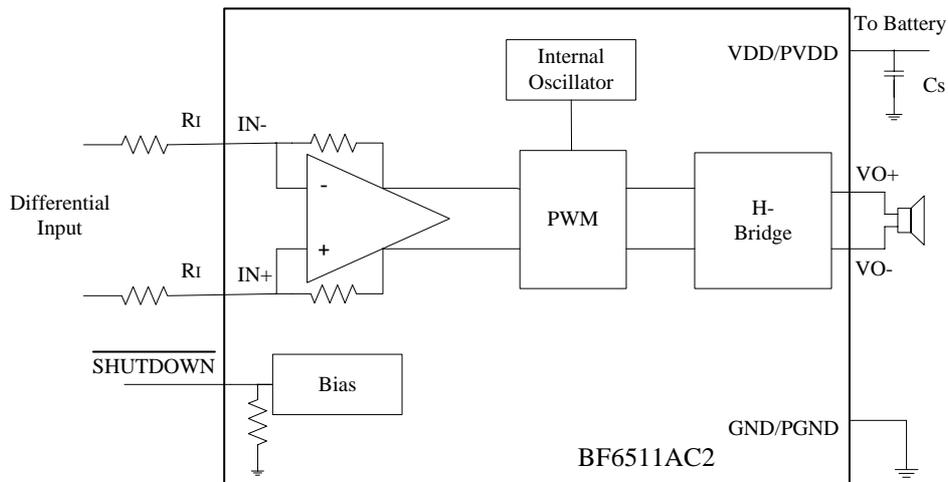


Figure 1. Typical BF6511AC2 Application Schematic with Differential Input for a Wireless Phone
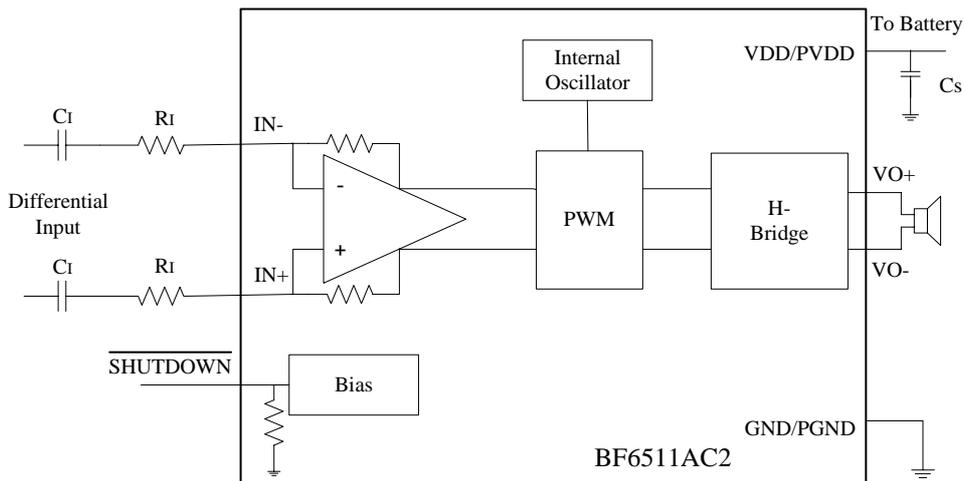


Figure 2. BF6511AC2 Application Schematic with Differential Input and Input Capacitors
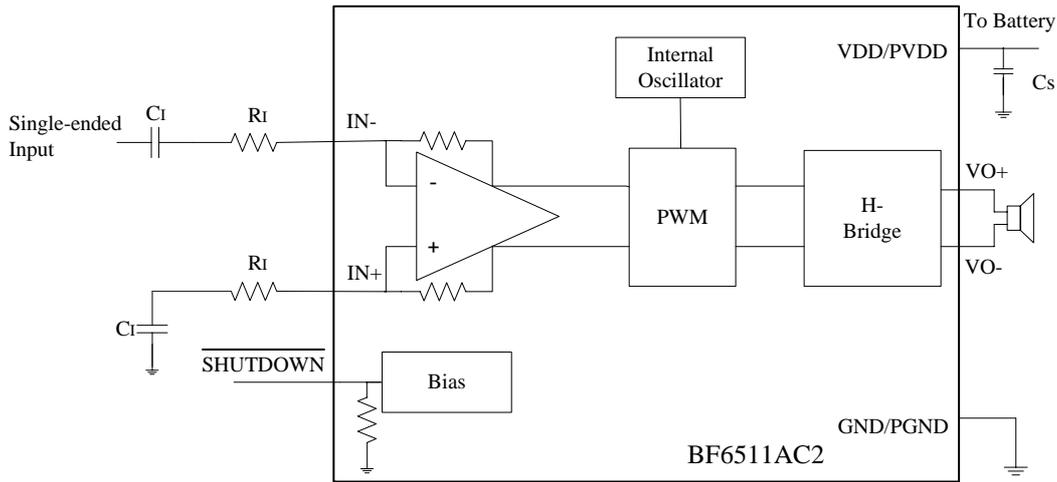
Figure 3. BF6511AC2 Application Schematic with Single-Ended Input

## TYPICAL COMPONENT VALUES

| COMPONENT | DESCRIPTION | VALUE |
|-----------|-------------|-------|
| $R_I$ | Input Resistors | 150 k$\Omega$ ($\pm$0.5%) |
| $C_S$ | Decoupling Capacitor | 1 μF (+22%, -80%) |
| $C_I$ | Input Capacitor | 3.3 nF ($\pm$10%) |

Note: $C_I$ is only needed for single-ended input or if $V_{ICM}$ is not between 0.5 V and VDD– 0.8 V. $C_I$ = 3.3 nF (with $R_I$ = 150 k$\Omega$ ) gives a high-pass corner frequency of 321 Hz.

## INPUT RESISTORS $R_I$

The input resistors ($R_I$) set the gain of the amplifier according to Equation 1.

Gain=2 x 150 k$\Omega$/$R_I$      (V/V) …………………………………………… (1)

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%. Place the input resistors very close to the BF6511AC2 to limit noise injection on the high-impedance nodes.

For optimal performance the gain should be set to 2 V/V or lower. Lower gain allows the BF6511AC2 to operate at its best, and keeps a high voltage at the input making the inputs less susceptible to noise.

## DECOUPLING CAPACITOR $C_S$

The BF6511AC2 is a high-performance class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF, placed as close as possible to the device VDD lead works best. Placing this decoupling capacitor close to the BF6511AC2 is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 10 μF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

**INPUT CAPACITOR C$_I$**

The BF6511AC2 does not require input coupling capacitors if the design uses a differential source that is biased from 0.5 V to VDD– 0.8 V (shown in Figure 1). If the input signal is not biased within the recommended common-mode input range, if needing to use the input as a high pass filter (shown in Figure 2), or if using a single-ended source (shown in Figure 3), input coupling capacitors are required. The input capacitors and input resistors form a high-pass filter with the corner frequency, fc, determined in Equation 2.

$$f_c = \frac{1}{2\pi R_I C_I} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(2)}$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application. Equation 3 is reconfigured to solve for the input coupling capacitance.

$$C_I = \frac{1}{2\pi R_I f_C} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(3)}$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

For a flat low-frequency response, use large input coupling capacitors (1 µF). However, in a GSM phone the ground signal is fluctuating at 217 Hz, but the signal from the codec does not have the same 217 Hz fluctuation. The difference between the two signals is amplified, sent to the speaker, and heard as a 217 Hz hum.

**SUMMING INPUT SIGNALS WITH THE BF6511AC2**

Most wireless phones or PDAs need to sum signals at the audio power amplifier or just have two signal sources that need separate gain. The BF6511AC2 makes it easy to sum signals or use separate signal sources with different gains. Many phones now use the same speaker for the earpiece and ringer, where the wireless phone would require a much lower gain for the phone earpiece than for the ringer. PDAs and phones that have stereo headphones require summing of the right and left channels to output the stereo signal to the mono speaker.

**SUMMING TWO DIFFERENTIAL SIGNALS**

Two extra resistors are needed for summing differential signals (a total of 5 components). The gain for each input source can be set independently (see Equation 4 and Equation 5, and Figure 4).

$$Gain1 = \frac{V_O}{V_{I1}} = 2 \times \frac{150k\Omega}{R_{I1}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(4)}$$

$$Gain2 = \frac{V_O}{V_{I2}} = 2 \times \frac{150k\Omega}{R_{I2}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(5)}$$

If summing left and right inputs with a gain of 1 V/V, use R$_{I1}$ = R$_{I2}$ = 300 k .
If summing a ring tone and a phone signal, set the ring-tone gain to Gain 2 = 2 V/V, and the phone gain to gain1 = 0.1 V/V. The resistor values would be: R$_{I1}$=3M, and R$_{I2}$=150 k.
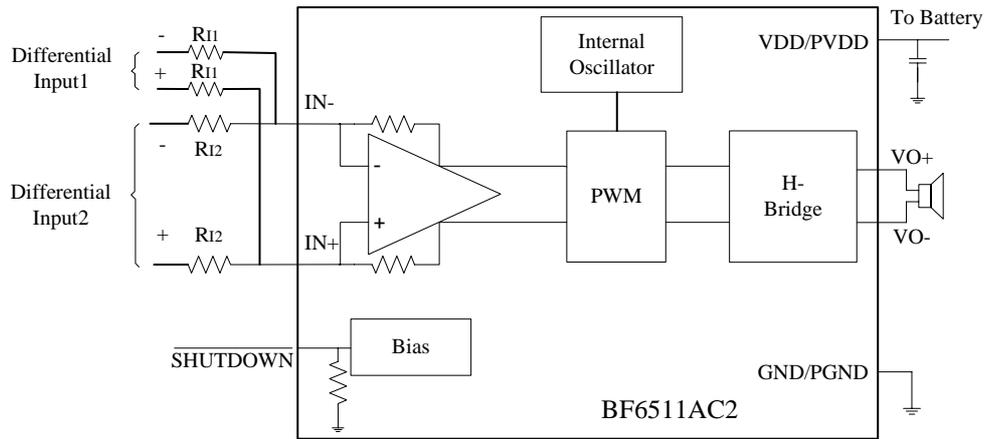
Figure 4. Application Schematic with BF6511AC2 Summing Two Differential Inputs

## SUMMING A DIFFERENTIAL INPUT SIGNAL AND A SINGLE-ENDED INPUT SIGNAL

Figure 5 shows how to sum a differential input signal and a single-ended input signal. Ground noise can couple in through IN+ with this method. It is better to use differential inputs. The corner frequency of the single-ended input is set by $C_{I2}$, shown in Equation 8. To assure that each input is balanced, the single-ended input must be driven by a low-impedance source even if the input is not in use

$$Gain1 = \frac{V_O}{V_{I1}} = 2 \times \frac{150k\Omega}{R_{I1}} \text{(V/V)}..............................(6)$$

$$Gain2 = \frac{V_O}{V_{I2}} = 2 \times \frac{150k\Omega}{R_{I2}} \text{(V/V)}.............................(7)$$

$$C_{I2} = \frac{1}{2\pi R_{I2} f_{C2}}...............................................(8)$$

If summing a ring tone and a phone signal, the phone signal should use a differential input signal while the ring tone might be limited to a single-ended signal. Phone gain is set at gain 1 = 0.1 V/V, and the ring-tone gain is set to gain 2 = 2 V/V, the resistor values would be

$R_{I1}$ = 3M$\Omega$ , and $R_{I2}$ = 150 k$\Omega$.
The high pass corner frequency of the single-ended input is set by $C_{I2}$. If the desired corner frequency is less than 20 Hz.

$$C_{I2} > \frac{1}{2\pi \times 150k\Omega \times 20Hz} = 53pF \qquad ....................(9)$$
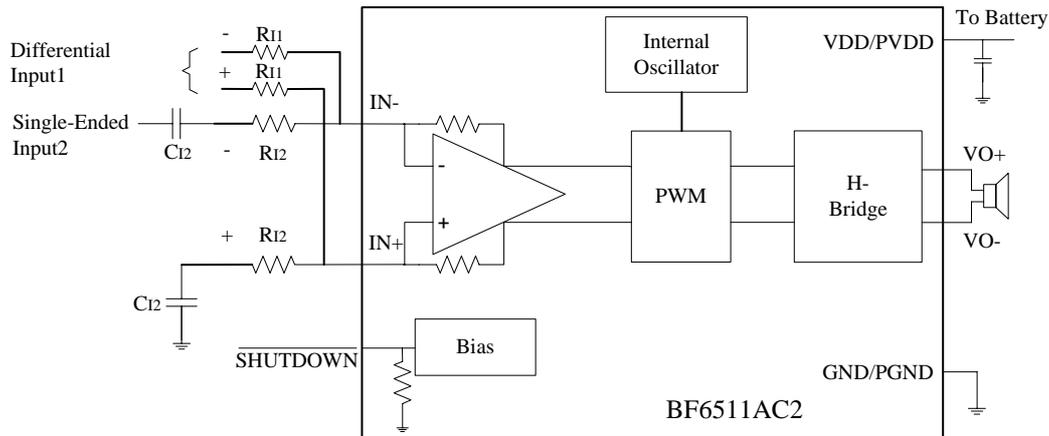
Figure 5. Application Schematic with BF6511AC2 Summing Differential Input and Single-Ended Input Signals

## SUMMING TWO SINGLE-ENDED INPUT SIGNALS

Four resistors and three capacitors are needed for summing single-ended input signals. The gain and corner frequencies (fc1 and fc2) for each input source can be set independently (see Equation 11 through Equation 14, and Figure 6). Resistor, $R_P$, and capacitor, $C_P$, are needed on the IN+ terminal to match the impedance on the IN- terminal. The single-ended inputs must be driven by low impedance sources even if one of the inputs is not outputting an ac signal.

$$Gain1 = \frac{V_O}{V_{I1}} = 2 \times \frac{150k\Omega}{R_{I1}} (V/V) ................................(11)$$

$$Gain2 = \frac{V_O}{V_{I2}} = 2 \times \frac{150k\Omega}{R_{I2}} (V/V) .............................(12)$$
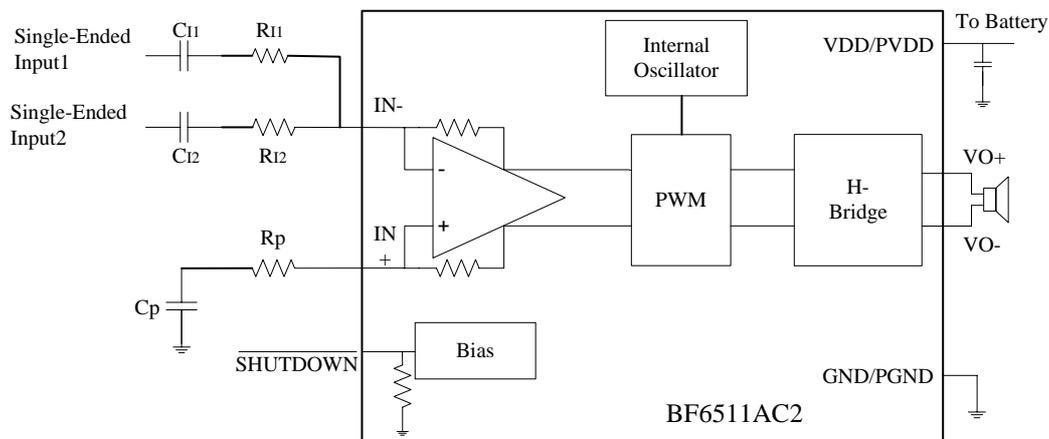


Figure 6. Application Schematic with BF6511AC2 Summing Two Single-Ended Inputs

## ELIMINATING THE OUTPUT FILTER WITH THE BF6511AC2

This section focuses on why the user can eliminate the output filter with the BF6511AC2.

### EFFECT ON AUDIO

The class-D amplifier outputs a pulse-width modulated (PWM) square wave, which is the sum of the switching waveform and the amplified input audio signal. The human ear acts as a band-pass filter such that only the frequencies between approximately 20 Hz and 20 kHz are passed. The switching frequency components are much greater than 20 kHz, so the only signal heard is the amplified input audio signal.

### BF6511AC2 MODULATION SCHEME

The BF6511AC2 uses a modulation scheme that still has each output switching from 0 to the supply voltage. However, OUT+ and OUT- are now in phase with each other with no input. The duty cycle of OUT+ is greater than 50% and OUT- is less than 50% for positive voltages. The duty cycle of OUT+ is less than 50% and OUT- is greater than 50% for negative voltages. The voltage across the load sits at 0 volts throughout most of the switching period greatly reducing the switching current, which reduces any $I^2R$ losses in the load.

### WHEN TO USE AN OUTPUT FILTER

Design the BF6511AC2 without an output filter if the traces from amplifier to speaker are short. The BF6511AC2 passed FCC and CE radiated emissions with no shielding with speaker trace wires 100 mm long or less. Wireless handsets and PDAs are great applications for class-D without a filter.

A ferrite bead filter can often be used if the design is failing radiated emissions without an LC filter, and the frequency sensitive circuit is greater than 1 MHz. This is good for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30 MHz. If choosing a ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies. Use an LC output filter if there are low frequency (< 1 MHz) EMI sensitive circuits and/or there are long leads from amplifier to speaker.

Figure 7 and Figure 8 show typical ferrite bead and LC output filters.
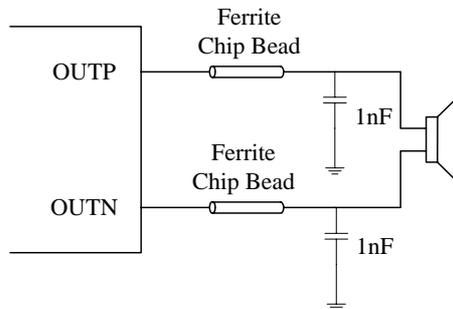


Figure 7. Typical Ferrite Chip Bead Filter (Chip bead example: NEC/Tokin: N2012ZPS121)
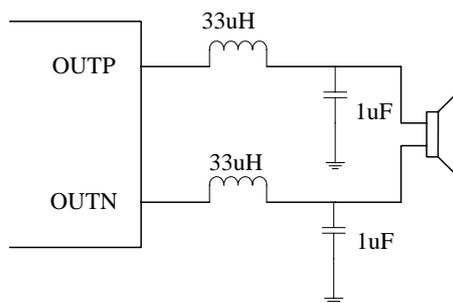


Figure 8. Typical LC Output Filter, Cutoff Frequency of 27 kHz

## PACKAGING INFORMATION

| Orderable Device | Package Type | Pins | Package Qty | Eco Plan[Note1] | Peak Temp[Note2] |
|---|---|---|---|---|---|
| BF6511AC2 | WCSP | 9 | 3000 | Pb-Free (RoHS) | 245C-UNLIM |

**Note1:** Eco Plan -

**Pb-Free (RoHS):** BYD's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, BYD Pb-Free products are suitable for use in specified lead-free processes.

**Note2:** Peak Temp. -- Peak solder temperature.

## TAPE AND REEL INFORMATION



Sprocket holes

Pocket quadrants
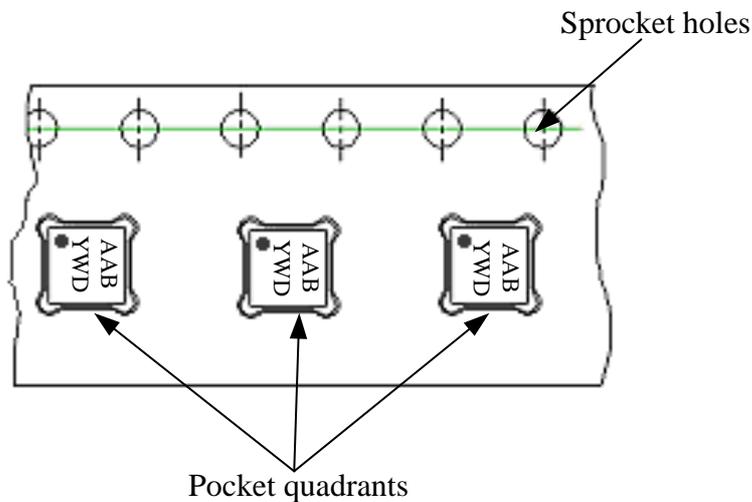
| Material | Description |
|---|---|
| Carrier Tape | Tape width: 8 mm; Length: 506 M |
| | Pocket Pitch: 4 mm |
| | Thickness: 0.23 mm |
| Cover Tape | Tape width: 5.3 mm; Length: 500 M |
| Reel | PS (Blue) reel 7", 9mm |
| Antistatic Adhesive Tapes | Width: 6mm |

# PACKAGE DESCRIPTION UNIT MILLIMETRE

TOP VIEW

BOTTOM VIEW

SIDE VIEW
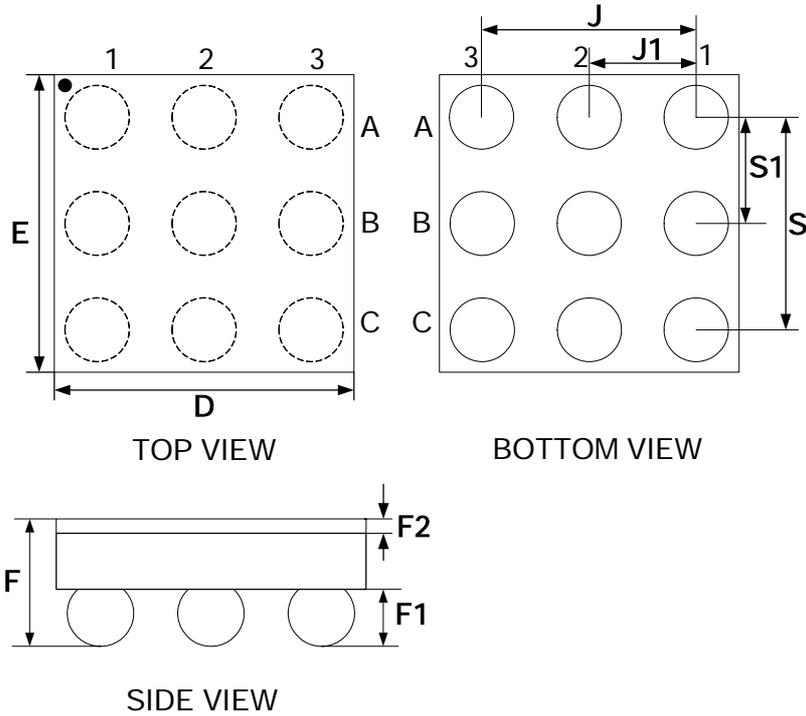
| SYMBOL | DIMENSION | | |
|---|---|---|---|
| | MIN | TYP | MAX |
| D | 1.43 | | 1.53 |
| E | 1.43 | | 1.53 |
| F | 0.575 | | 0.625 |
| F1 | 0.22 | | 0.27 |
| F2 | 0.02 | | 0.03 |
| J | | 1.0 | |
| J1 | | 0.5 | |
| S | | 1.0 | |
| S1 | | 0.5 | |

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