

# SN75172 QUADRUPLE DIFFERENTIAL LINE DRIVER

SLLS038B – OCTOBER 1980 – REVISED MAY 1995

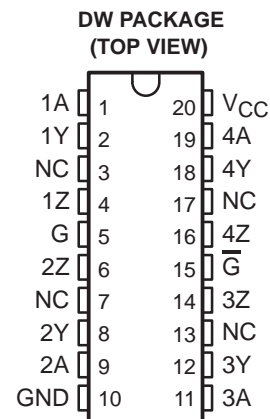
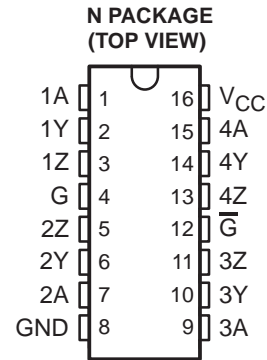
- Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Output Voltage Range of  $-7\text{ V}$  to  $12\text{ V}$
- Active-High and Active-Low Enables
- Thermal Shutdown Protection
- Positive- and Negative-Current Limiting
- Operates From Single 5-V Supply
- Logically Interchangeable With AM26LS31

## description

The SN75172 is a monolithic quadruple differential line driver with 3-state outputs. It is designed to meet the requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11. The device is optimized for balanced multipoint bus transmission at rates of up to 4 megabaud. Each driver features wide positive and negative common-mode output voltage ranges, making it suitable for party-line applications in noisy environments.

The SN75172 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately  $150^{\circ}\text{C}$ . This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

The SN75172 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .



NC – No internal connection

**FUNCTION TABLE**  
(each driver)

INPUT A	ENABLES		OUTPUTS	
	G	$\bar{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level, X = irrelevant,  
Z = high impedance (off)



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 **TEXAS  
INSTRUMENTS**

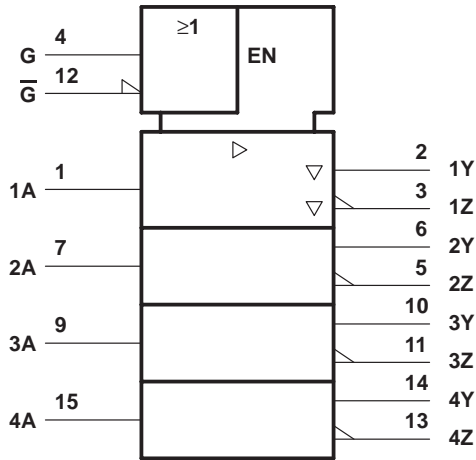
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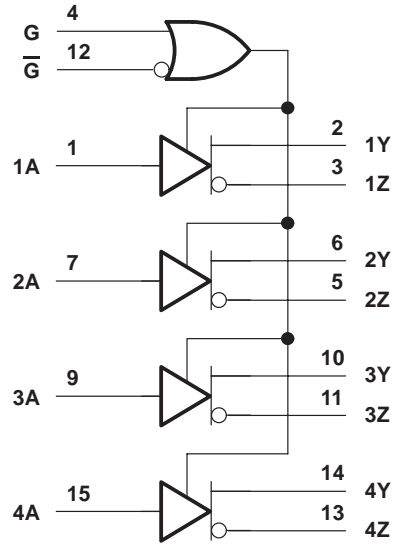
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Terminal numbers shown are for the N package.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature (unless otherwise noted)‡

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Voltage range at any bus terminal	-10 V to 15 V
Input voltage, $V_I$	5.5 V
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

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## recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$	4.75	5	5.25	V
High-level input voltage, $V_{IH}$	2			V
Low-level input voltage, $V_{IL}$			0.8	V
Common-mode output voltage, $V_{OC}$			-7 to 12	V
High-level output current, $I_{OH}$			-60	mA
Low-level output current, $I_{OL}$			60	mA
Operating free-air temperature, $T_A$	0		70	°C

## electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
$V_{IK}$ Input clamp voltage	$I_I = -18$ mA			-1.5	V	
$V_O$ Output voltage	$I_O = 0$	0		6	V	
$V_{OH}$ High-level output voltage	$V_{IH} = 2$ V, $V_{IL} = 0.8$ V, $I_{OH} = -33$ mA		3.7		V	
$V_{OL}$ Low-level output voltage	$V_{IH} = 2$ V, $V_{IL} = 0.8$ V, $I_{OH} = 33$ mA		1.1		V	
$ V_{OD1} $ Differential output voltage	$I_O = 0$	1.5		6	V	
$ V_{OD2} $ Differential output voltage	$R_L = 100$ $\Omega$ , See Figure 1	$1/2 V_{OD1}$ or $2^\ddagger$			V	
	$R_L = 54$ $\Omega$ , See Figure 1	1.5	2.5	5	V	
$V_{OD3}$ Differential output voltage	See Note 2	1.5		5	V	
$\Delta V_{OD} $ Change in magnitude of differential output voltage§	$R_L = 54$ $\Omega$ or $100$ $\Omega$ , See Figure 1			$\pm 0.2$	V	
$V_{OC}$ Common-mode output voltage¶				+3 -1	V	
$\Delta V_{OC} $ Change in magnitude of common-mode output voltage§				$\pm 0.2$	V	
$I_O$ Output current with power off	$V_{CC} = 0$ , $V_O = -7$ V to $12$ V			$\pm 100$	$\mu$ A	
$I_{OZ}$ High-impedance-state output current	$V_O = -7$ V to $12$ V			$\pm 100$	$\mu$ A	
$I_{IH}$ High-level input current	$V_I = 2.7$ V			20	$\mu$ A	
$I_{IL}$ Low-level input current	$V_I = 0.5$ V			-360	$\mu$ A	
$I_{OS}$ Short-circuit output current	$V_O = -7$ V			-180	mA	
	$V_O = V_{CC}$			180		
	$V_O = 12$ V			500		
$I_{CC}$ Supply current (all drivers)	No load	Outputs enabled		38	60	mA
		Outputs disabled		18	40	

† All typical values are at  $V_{CC} = 5$  V and  $T_A = 25^\circ$ C.

‡ The minimum  $V_{OD2}$  with a 100- $\Omega$  load is either  $1/2 V_{OD1}$  or 2 V, whichever is greater.

§  $\Delta|V_{OD}|$  and  $\Delta|V_{OC}|$  are the changes in magnitude of  $V_{OD}$  and  $V_{OC}$ , respectively, that occur when the input is changed from a high level to a low level.

¶ In ANSI Standard EIA/TIA-422-B,  $V_{OC}$ , which is the average of the two output voltages with respect to ground, is called output offset voltage,  $V_{OS}$ .

NOTE 2: See Figure 3-5 of EIA Standard RS-485.



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## SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	EIA/TIA-422-B	RS-485
$V_O$	$V_{oa}, V_{ob}$	$V_{oa}, V_{ob}$
$ V_{OD1} $	$V_o$	$V_o$
$ V_{OD2} $	$V_t (R_L = 100 \Omega)$	$V_t (R_L = 54 \Omega)$
$ V_{OD2} $		$V_t$ (Test Termination Measurement 2)
$\Delta V_{OD} $	$  V_t  -  \bar{V}_t  $	$  V_t  -  \bar{V}_t  $
$V_{OC}$	$ V_{os} $	$ V_{os} $
$\Delta V_{OC} $	$ V_{os} - \bar{V}_{os} $	$ V_{os} - \bar{V}_{os} $
$I_{OS}$	$ I_{sa} ,  I_{sb} $	
$I_O$	$ I_{xa} ,  I_{xb} $	$I_{ia}, I_{ib}$

switching characteristics,  $V_{CC} = 5 V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_d(OD)$ Differential-output delay time	$R_L = 54 \Omega, \text{ See Figure 2}$		45	65	ns
$t_t(OD)$ Differential-output transition time			80	120	ns
$t_{pZH}$ Output enable time to high level	$R_L = 110 \Omega, \text{ See Figure 3}$		80	120	ns
$t_{pZL}$ Output enable time to low level	$R_L = 110 \Omega, \text{ See Figure 4}$		45	80	ns
$t_{PHZ}$ Output disable time from high level	$R_L = 110 \Omega, \text{ See Figure 3}$		78	115	ns
$t_{PLZ}$ Output disable time from low level	$R_L = 110 \Omega, \text{ See Figure 4}$		18	30	ns

## PARAMETER MEASUREMENT INFORMATION

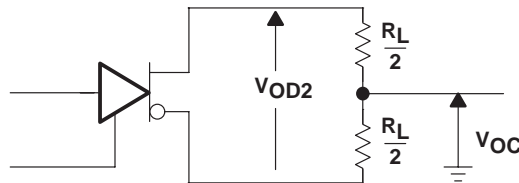
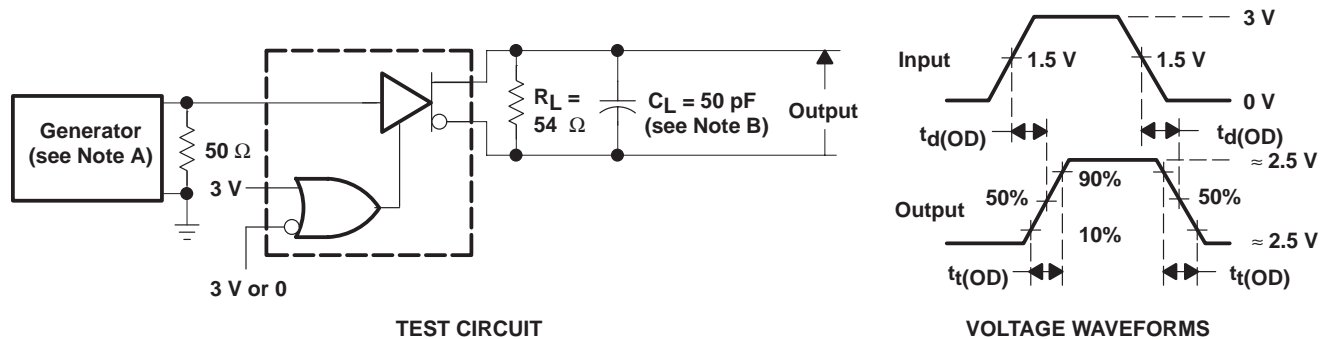


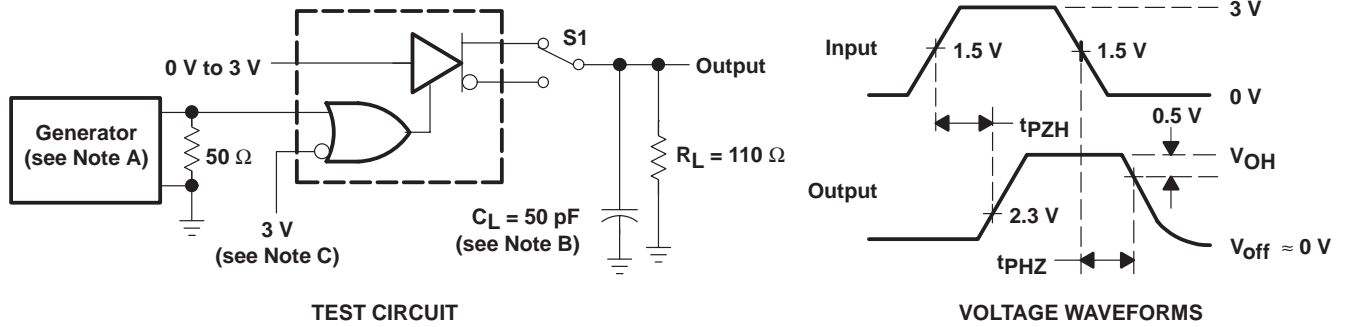
Figure 1. Differential and Common-Mode Output Voltages



- NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $t_r \leq 5 \text{ ns}, t_f \leq 5 \text{ ns}, \text{PRR} \leq 1 \text{ MHz}, \text{duty cycle} = 50\%, Z_0 = 50 \Omega$ .  
B.  $C_L$  includes probe and stray capacitance.

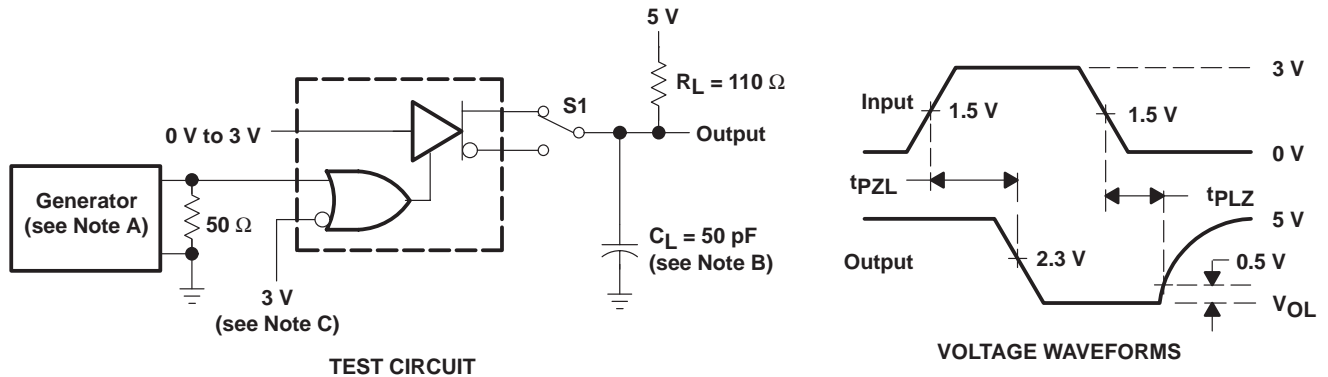
Figure 2. Differential-Output Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES. A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, duty cycle = 50%,  $t_r \leq 5$  ns,  $t_f \leq 5$  ns,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and stray capacitance.  
 C. To test the active-low enable  $\overline{G}$ , ground G and apply an inverted waveform to  $\overline{G}$ .

Figure 3. Test Circuit and Voltage Waveforms



- NOTES. A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, duty cycle = 50%,  $t_r \leq 5$  ns,  $t_f \leq 5$  ns,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and stray capacitance.  
 C. To test the active-low enable  $\overline{G}$ , ground G and apply an inverted waveform to  $\overline{G}$ .

Figure 4. Test Circuit and Voltage Waveforms

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## TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE  
vs  
HIGH-LEVEL OUTPUT CURRENT

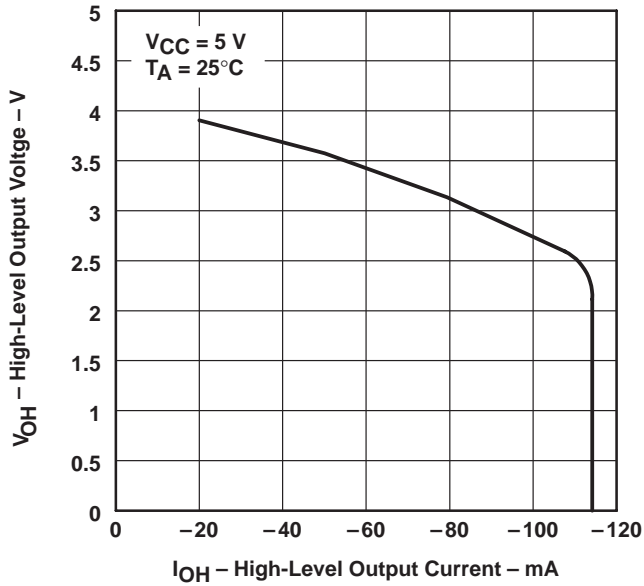


Figure 5

LOW-LEVEL OUTPUT VOLTAGE  
vs  
LOW-LEVEL OUTPUT CURRENT

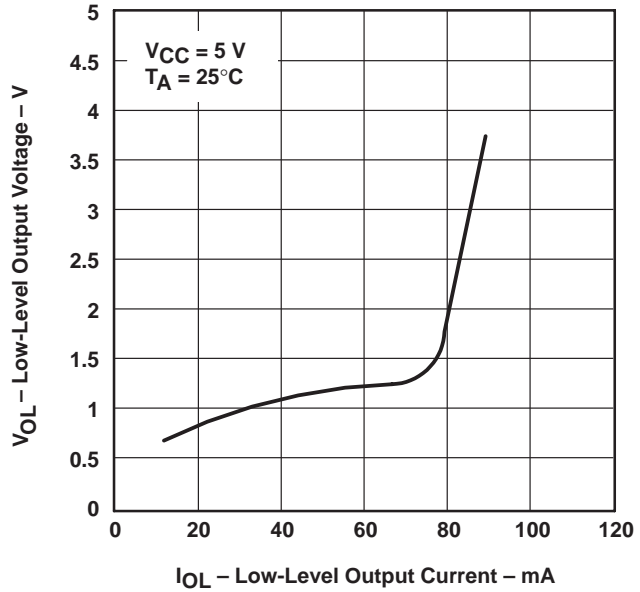


Figure 6

DIFFERENTIAL OUTPUT VOLTAGE  
vs  
OUTPUT CURRENT

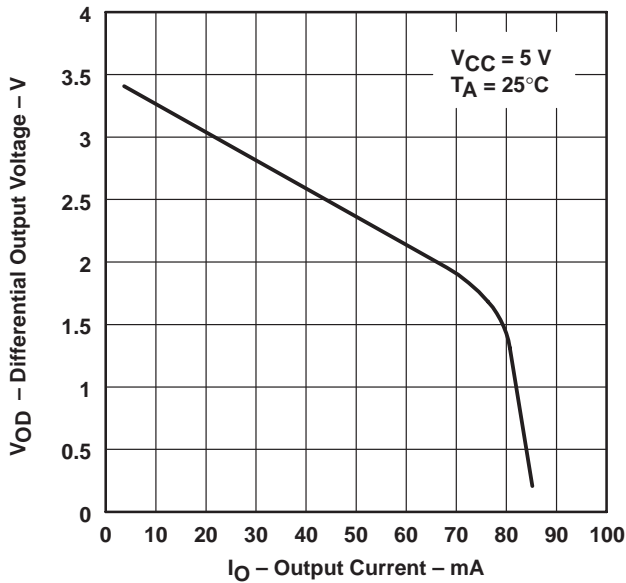


Figure 7

OUTPUT CURRENT  
vs  
OUTPUT VOLTAGE

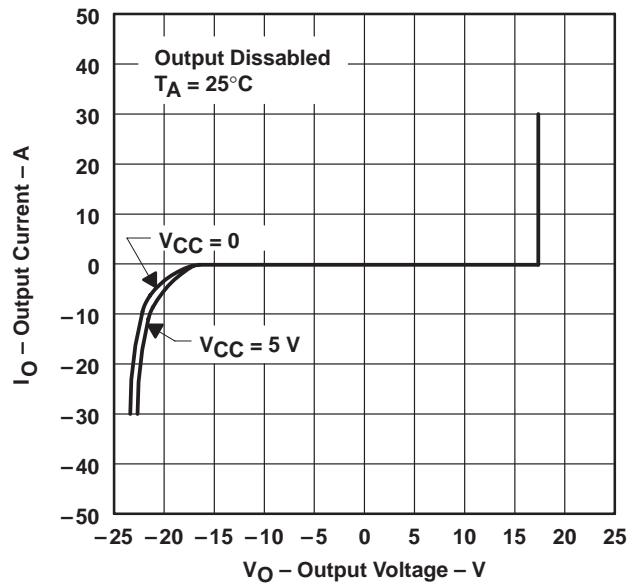


Figure 8

TYPICAL CHARACTERISTICS

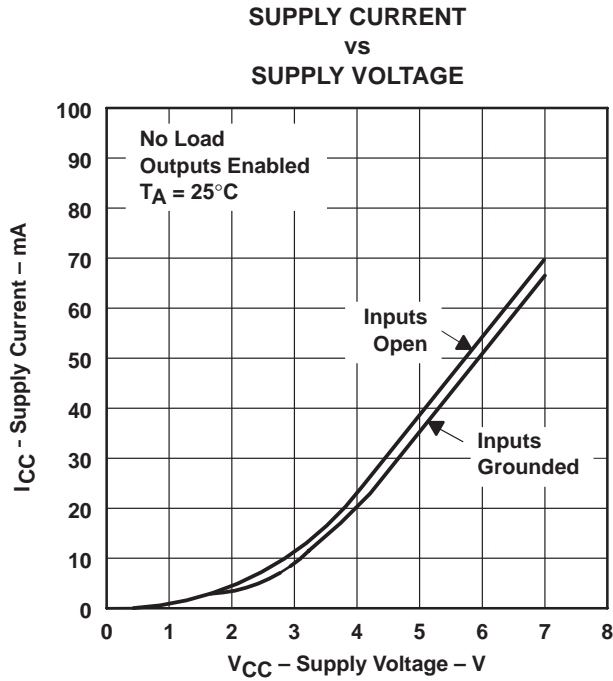


Figure 9

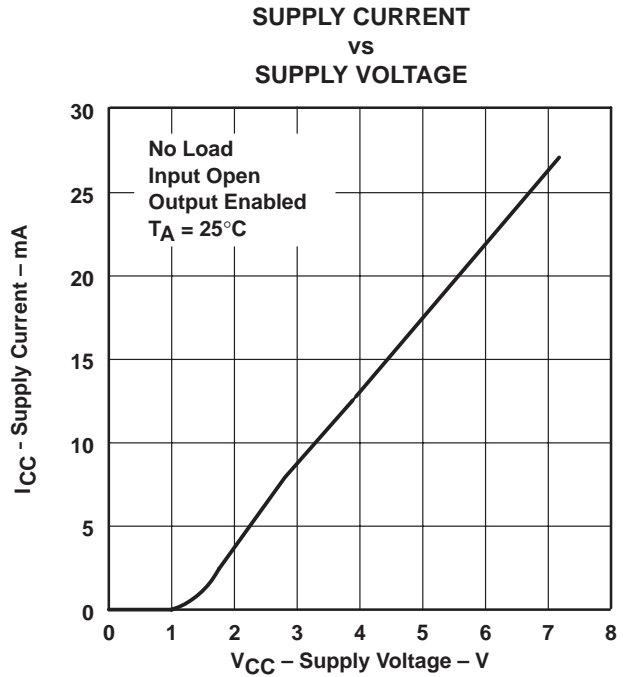
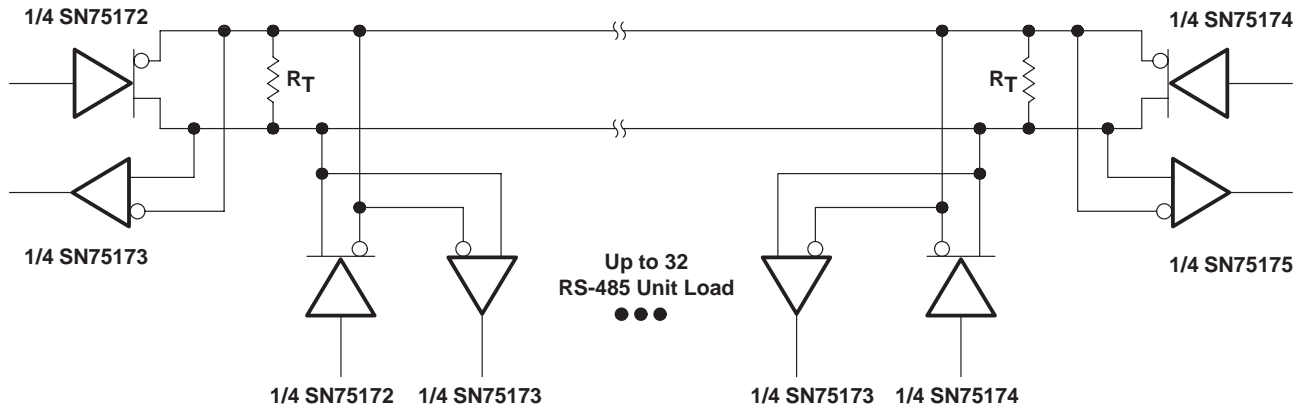


Figure 10

APPLICATION INFORMATION



NOTE A: The line length should be terminated at both ends in its characteristic impedance ( $R_T = Z_0$ ). Stub lengths off the main line should be kept as short as possible.

Figure 11

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN75172DW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN75172DWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN75172N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



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