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TOSHIBA MULTI-CHIP INTEGRATED CIRCUIT SILICON GATE CMOS

Low Power SDRAM and Nand E^{2}PROM Mixed Multi-Chip Package

Lead-Free

DESCRIPTION

The TY9000AC10AOGG is a mixed multi-chip package containing a 536,870,912-bit (268,435,456-bit × 2devices) Low Power Synchronous DRAM and a 1,107,296,256-bit (553,648,128-bit × 2devices) Nand E^{2}PROM.
The TY9000AC10AOGG is available in a 225-pin BGA package making it suitable for a variety of applications.

MCP Features

- Power supply voltage
  Low power SDRAM : 1.65 to 1.95 V
  Nand E^{2}PROM : 2.5 to 3.0 V
- Operating temperature of –30° to 85°C
- Package
  P-TFBGA225-1114-0.65BZ (Weight: g)
- Lead-Free

Low Power SDRAM Features

- Organization : 2pcs of 4M × 16 bits × 4 banks
  (32 bits I/O)
- Power dissipation
  Operating : 80 mA maximum
  Refresh : 110 mA maximum
  Self refresh : 800 μA maximum
- Programmable driver strength
- Programmable temperature compensated self refresh (Option)
- Deep power down mode
- Fully Synchronous DRAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Quad internal banks controlled by BA0 and BA1
- Byte control by DQM0, DQM1, DQM2 and DQM3
- Wrap sequence = Sequential/ Interleave
- /CAS latency (CL) = 2, 3
- Automatic precharge and controlled precharge
- Auto refresh and self refresh
- 8,192 refresh cycles/64ms
- Burst termination by Burst stop command and Precharge command

Nand E^{2}PROM Features

- Organization
  Memory cell array : 528 × 256K × 8 bits
  Register : 528 × 8 bits
  Page size : 528 bytes
  Block size : (16K + 512) bytes
- Power dissipation
  Read operating : 30 mA maximum
  Program / Erase operating : 30 mA maximum
  Standby : 100 μA maximum
- Access time :
  Cell array register : 25 μs @CL=100pF
  Serial read cycle : 50 ns @CL=100pF
- Modes :
  Read , Reset , Auto page program
  Auto block erase , Status read
  Multi block program , Multi block erase
- Mode control
  Serial input / output , Command control
- Program/Erase cycles
  1E5 cycle (with ECC)

PIN ASSIGNMENT (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	NC	NC	NC							NC	NC	NC	NC
B	NC	NC	NC	NC							NC	NC	NC	NC
C	NC	NC	A0	BA0	NC	V_{SS}	V_{CCd}	CLK	A12	A9	A7	A5	NC	NC
D	NC	V_{CCd}	A1	BA1	$\overline{RAS}$	$\overline{WEd}$	$\overline{CS1}$	CKE	A11	A8	A6	A4	V_{CCd}	NC
E	NC	A3	A2	A10	$\overline{CS0}$	$\overline{CAS}$	NC	NC	NC	NC	NC	NC	NC	
F		NC	NC	NC	NC	NC	V_{SS}	NC	NC	NC	NC	NC	NC	
G		V_{SS}	NC	NC	NC	NC	NC	NC	NC	NC	NC	I/O8	V_{SS}	
H		NC	NC	NC	NC	NC			NC	I/O7	NC	I/O6	NC	
J		NC	NC	NC	NC	NC			I/O5	NC	NC	V_{CCn}	NC	
K	NC	NC	NC	NC	NC	$\overline{WEn}$			NC	NC	NC	V_{CCn}	NC	NC
L	NC	NC	NC	NC	NC	$\overline{WPn}$			NC	I/O3	NC	I/O4	V_{SS}	NC
M		R/$\overline{Bn}$	ALE	CLE	NC	NC			$\overline{CEn}$	$\overline{REn}$	I/O1	NC	I/O2	
N		NC	NC	NC	NC	NC			NC	NC	NC	NC	NC	
P		V_{SS}	DQ16	DQ18	DQ20	DQ22	NC	NC	DQ24	DQ25	DQ27	DQ29	V_{SS}	
R		NC	DQ17	DQ19	DQ21	DQ23	NC	V_{SS}	NC	DQ26	DQ28	DQ30	DQ31	
T		NC	NC	DQ1	DQ2	DQ5	NC	DQM1	DQ8	DQ9	DQ11	DQ14	NC	
U	NC	V_{SS}	NC	DQ0	DQ4	V_{SS}	DQ7	DQM0	DQM3	V_{SS}	DQ12	DQ15	V_{SS}	NC
V	NC	NC	V_{CCd}	V_{CCQd}	DQ3	DQ6	DQM2	V_{CCd}	V_{CCQd}	DQ10	DQ13	V_{CCd}	NC	NC
Y	NC	NC	NC	NC							NC	NC	NC	NC
AA	NC	NC	NC	NC							NC	NC	NC	NC

PIN NAMES

A0 to A12	Address inputs for Low Power SDRAM
BA0,BA1	Bank Select for Low Power SDRAM
DQ0 to DQ31	Data inputs / outputs for Low Power SDRAM
CLK	Clock input for Low Power SDRAM
CKE	Clock enable for Low Power SDRAM
$\overline{CS0}$, $\overline{CS1}$	Chip select for Low Power SDRAM
$\overline{RAS}$	Row address strobe for Low Power SDRAM
$\overline{CAS}$	Column address strobe for Low Power SDRAM
$\overline{WEd}$	Write enable for Low Power SDRAM
DQM0, DQM1 DQM2, DQM3	Data mask enable for Low Power SDRAM
I/O1 to I/O8	I/O port Nand E^2PROM
$\overline{CEn}$	Chip enable for Nand E^2PROM
$\overline{REn}$	Read enable for Nand E^2PROM
$\overline{WEn}$	Write enable for Nand E^2PROM
CLE	Command latch enable for Nand E^2PROM
ALE	Address latch enable for Nand E^2PROM
$\overline{WPn}$	Write protect for Nand E^2PROM
R/$\overline{Bn}$	Ready/Busy for Nand E^2PROM
V_{CCd}	Main power supply for Low Power SDRAM
V_{CCQd}	DQ power supply for Low Power SDRAM
V_{CCn}	Main power supply for Nand E^2PROM
V_{SS}	Ground
NC	Not connected

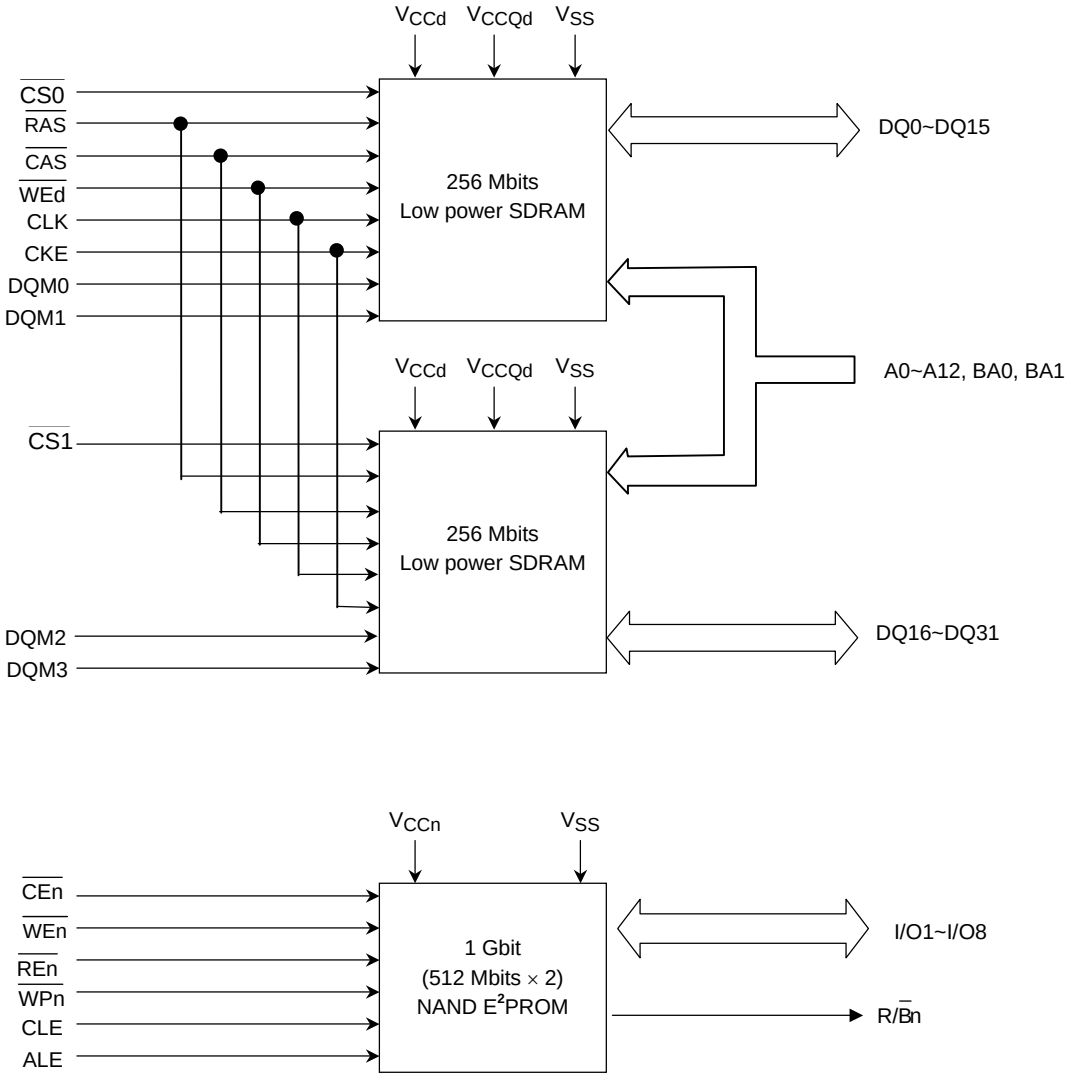
PIN NAME CONVERSION TABLE

MCP Pin		256M LPSD (1)	256M LPSD (2)	1G Nand
Loc	Name			
A1-4	NC	–	–	–
A11-14	NC	–	–	–
B1-4	NC	–	–	–
B11-14	NC	–	–	–
C1-2	NC	–	–	–
C3	A0	A0	A0	–
C4	BA0	BA0	BA0	–
C5	NC	–	–	–
C6	V_{SS}	V_{SS}	V_{SS}	V_{SS}
C7	V_{CCd}	V_{DD}	V_{DD}	–
C8	CLK	CLK	CLK	–
C9	A12	A12	A12	–
C10	A9	A9	A9	–
C11	A7	A7	A7	–
C12	A5	A5	A5	–
C13-14	NC	–	–	–
D1	NC	–	–	–
D2	V_{CCd}	V_{DD}	V_{DD}	–
D3	A1	A1	A1	–
D4	BA1	BA1	BA1	–
D5	$\overline{RAS}$	$\overline{RAS}$	$\overline{RAS}$	–
D6	$\overline{WEd}$	$\overline{WE}$	$\overline{WE}$	–
D7	$\overline{CS1}$	–	$\overline{CS}$	–
D8	CKE	CKE	CKE	–
D9	A11	A11	A11	–
D10	A8	A8	A8	–
D11	A6	A6	A6	–
D12	A4	A4	A4	–
D13	V_{CCd}	V_{DD}	V_{DD}	–
D14	NC	–	–	–
E1	NC	–	–	–
E2	A3	A3	A3	–
E3	A2	A2	A2	–
E4	A10	A10	A10	–
E5	$\overline{CS0}$	$\overline{CS}$	–	–
E6	$\overline{CAS}$	$\overline{CAS}$	$\overline{CAS}$	–
E7-13	NC	–	–	–
F2-6	NC	–	–	–
F7	V_{SS}	V_{SS}	V_{SS}	V_{SS}
F8-13	NC	–	–	–
G2	V_{SS}	V_{SS}	V_{SS}	V_{SS}
G3-G11	NC	–	–	–
G12	I/O8	–	–	I/O8
G13	V_{SS}	V_{SS}	V_{SS}	V_{SS}
H2-6	NC	–	–	–
H9	NC	–	–	–
H10	I/O7	–	–	I/O7
H11	NC	–	–	–
H12	I/O6	–	–	I/O6
H13	NC	–	–	–
J2-6	NC	–	–	–
J9	I/O5	–	–	I/O5
J10-11	NC	–	–	–
J12	V_{CCn}	–	–	V_{CC}
J13	NC	–	–	–

MCP Pin		256M LPSD (1)	256M LPSD (2)	1G Nand
Loc	Name			
K1-5	NC	–	–	–
K6	$\overline{WEn}$	–	–	$\overline{WE}$
K9-11	NC	–	–	–
K12	V_{CCn}	–	–	V_{CC}
K13-14	NC	–	–	–
L1-5	NC	–	–	–
L6	$\overline{WPn}$	–	–	$\overline{WP}$
L9	NC	–	–	–
L10	I/O3	–	–	I/O3
L11	NC	–	–	–
L12	I/O4	–	–	I/O4
L13	V_{SS}	V_{SS}	V_{SS}	V_{SS}
L14	NC	–	–	–
M2	R/$\overline{Bn}$	–	–	RY/$\overline{BY}$
M3	ALE	–	–	ALE
M4	CLE	–	–	CLE
M5-6	NC	–	–	–
M9	$\overline{CEn}$	–	–	$\overline{CE}$
M10	$\overline{REn}$	–	–	$\overline{RE}$
M11	I/O1	–	–	I/O1
M12	NC	–	–	–
M13	I/O2	–	–	I/O2
N2-6	NC	–	–	–
N9-13	NC	–	–	–
P2	V_{SS}	V_{SS}	V_{SS}	V_{SS}
P3	DQ16	–	DQ0	–
P4	DQ18	–	DQ2	–
P5	DQ20	–	DQ4	–
P6	DQ22	–	DQ6	–
P7-8	NC	–	–	–
P9	DQ24	–	DQ8	–
P10	DQ25	–	DQ9	–
P11	DQ27	–	DQ11	–
P12	DQ29	–	DQ13	–
P13	V_{SS}	V_{SS}	V_{SS}	V_{SS}
R2	NC	–	–	–
R3	DQ17	–	DQ1	–
R4	DQ19	–	DQ3	–
R5	DQ21	–	DQ5	–
R6	DQ23	–	DQ7	–
R7	NC	–	–	–
R8	V_{SS}	V_{SS}	V_{SS}	V_{SS}
R9	NC	–	–	–
R10	DQ26	–	DQ10	–
R11	DQ28	–	DQ12	–
R12	DQ30	–	DQ14	–
R13	DQ31	–	DQ15	–

MCP Pin		256M LPSD (1)	256M LPSD (2)	1G Nand
Loc	Name			
T2-3	NC	–	–	–
T4	DQ1	DQ1	–	–
T5	DQ2	DQ2	–	–
T6	DQ5	DQ5	–	–
T7	NC	–	–	–
T8	DQM1	UDQM	–	–
T9	DQ8	DQ8	–	–
T10	DQ9	DQ9	–	–
T11	DQ11	DQ11	–	–
T12	DQ14	DQ14	–	–
T13	NC	–	–	–
U1	NC	–	–	–
U2	V_{SS}	V_{SS}	V_{SS}	V_{SS}
U3	NC	–	–	–
U4	DQ0	DQ0	–	–
U5	DQ4	DQ4	–	–
U6	V_{SS}	V_{SS}	V_{SS}	V_{SS}
U7	DQ7	DQ7	–	–
U8	DQM0	LDQM	–	–
U9	DQM3	–	UDQM	–
U10	V_{SS}	V_{SS}	V_{SS}	V_{SS}
U11	DQ12	DQ12	–	–
U12	DQ15	DQ15	–	–
U13	V_{SS}	V_{SS}	V_{SS}	V_{SS}
U14	NC	–	–	–
V1-2	NC	–	–	–
V3	V_{CCd}	V_{DD}	V_{DD}	–
V4	V_{CCQd}	V_{DDQ}	V_{DDQ}	–
V5	DQ3	DQ3	–	–
V6	DQ6	DQ6	–	–
V7	DQM2	–	LDQM	–
V8	V_{CCd}	V_{DD}	V_{DD}	–
V9	V_{CCQd}	V_{DDQ}	V_{DDQ}	–
V10	DQ10	DQ10	–	–
V11	DQ13	DQ13	–	–
V12	V_{CCd}	V_{DD}	V_{DD}	–
V13-14	NC	–	–	–
Y1-4	NC	–	–	–
Y11-14	NC	–	–	–
AA1-4	NC	–	–	–
AA11-14	NC	–	–	–

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RANGE	UNIT
V_{CCd}	V_{CCd} Supply Voltage		−0.5~2.6	V
V_{CCQd}	V_{CCQd} Supply Voltage (DQ)		−0.5~2.6	V
V_{CCn}	V_{CCn} Supply Voltage		−0.5~4.6	V
V_{IN}	Input Voltage	LPSDRAM	−0.5~2.6	V
		Nand E^2PROM	−0.5~4.6	V
V_{DQ}	Input/Output Voltage	LPSDRAM	−0.5~V_{CCQd} + 0.5 (≤ 2.6)	V
		Nand E^2PROM	−0.5~V_{CCn} + 0.3 (≤ 4.6)	V
T_{opr}	Operating Temperature		−30~85	°C
P_D	Power Dissipation		0.6	W
T_{solder}	Soldering Temperature		260	°C
I_{OSHORT}	Output Short Circuit Current(1)		50	mA
T_{stg}	Storage Temperature		−55~125	°C

Note : (1) Output shorted for no more than one second. No more than one output shorted at a time

RECOMMENDED DC OPERATING CONDITIONS (Ta = −30°~85°C)

SYMBOL	PARAMETER		MIN	TYP.	MAX	UNIT
V_{CCd}	V_{CCd} Supply Voltage		1.65	1.8	1.95	V
V_{CCQd}	V_{CCQd} Supply Voltage (DQ)		1.65	1.8	1.95	
V_{CCn}	V_{CCn} Supply Voltage		2.5	2.8	3.0	
V_{IH}	Input High-Level Voltage	LPSDRAM	0.8 × V_{CCQd}	—	V_{CCQd} + 0.3(1)	
		Nand E^2PROM	2.0	—	V_{CCn} + 0.3	
V_{IL}	Input Low-Level Voltage	LPSDRAM	−0.3(2)	—	0.3	
		Nand E^2PROM	−0.3(3)	—	0.5	

Note: (1) V_{CCQd} + 1.5 V for pulse width ≤ 5 ns

(2) −1.5 V for pulse width ≤ 5 ns

(3) −2.0 V for pulse width ≤ 20 ns

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	—	—	TBD	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	—	—	TBD	pF

Note: These parameters are sampled periodically and are not tested for every device.

DC CHARACTERISTICS - 1

(Ta = –30°~85°C, V_{CCd}/V_{CCQd} = 1.65V~1.95V, V_{CCn} = 2.5V~3.0V)

SYMBOL	PARAMETER	CONDITION		MIN	MAX	UNIT
I_{CC1sd}	LPSDRAM Operating current(1)	Burst length=1 , tRC min I_{OUT} = 0 mA One bank active	$\overline{CAS}$ latency=2	—	80	mA
			$\overline{CAS}$ latency=3	—	80	mA
I_{CC2Psd}	LPSDRAM Standby current in power down	CKE = V_{IL} , tCK = 15 ns		—	1.2	mA
$I_{CC2PSsd}$	LPSDRAM Standby current in power down (Input signal stable)	CKE = V_{IL} , tCK = ∞		—	1.0	mA
I_{CC2Nsd}	LPSDRAM Standby current in non power down	CKE = V_{IH} , tCK = 15 ns , $\overline{CS0}$ = V_{IH}, $\overline{CS1}$ = V_{IH} Input signals are changed one time during 30 ns		—	6	mA
$I_{CC2NSsd}$	LPSDRAM Standby current in non power down (Input signal stable)	CKE = V_{IH} , tCK = ∞ , Input signals are stable		—	4	mA
I_{CC3Psd}	LPSDRAM Active standby Current in power down	CKE = V_{IL} , tCK = 15 ns , $\overline{CS0}$ = V_{IH}, $\overline{CS1}$ = V_{IH} Input signals are changed one time during 30 ns		—	2	mA
$I_{CC3PSsd}$	LPSDRAM Active standby Current in power down (Input signal stable)	CKE = V_{IL} , tCK = ∞		—	1.6	mA
I_{CC3Nsd}	LPSDRAM Active standby Current in non power down	CKE = V_{IH} , tCK = 15 ns , $\overline{CS0}$ = V_{IH}, $\overline{CS1}$ = V_{IH} Input signals are changed one time during 30 ns		—	30	mA
$I_{CC3NSsd}$	LPSDRAM Active standby Current in non power down (Input signal stable)	CKE = V_{IH} , tCK = ∞ , Input signals are stable		—	10	mA
I_{CC4sd}	LPSDRAM Burst operating current (2)	Burst length=1 , tCK min I_{OUT} = 0 mA , All banks active	$\overline{CAS}$ latency=2	—	90	mA
			$\overline{CAS}$ latency=3	—	120	mA
I_{CC5sd}	LPSDRAM Refresh current (3)	tCK min	$\overline{CAS}$ latency=2	—	110	mA
			$\overline{CAS}$ latency=3	—	110	mA
I_{CC6sd}	LPSDRAM Self refresh current (4)	Ta ≤ 85°C +0°C / -15°C, CKE ≤ 0.2V	PASR="000" (Full)	—	800	μA
			PASR="001" (2BK)	—	600	μA
			PASR="010" (1BK)	—	500	μA
		Ta ≤ 45°C CKE ≤ 0.2V	PASR="000" (Full)	360(5)	—	μA
			PASR="001" (2BK)	300(5)	—	μA
			PASR="010" (1BK)	260(5)	—	μA
I_{CC7sd}	LPSDRAM Standby current in deep power down mode	CKE ≤ 0.2V		—	20	μA

DC CHARACTERISTICS - 2

(Ta = −30°~85°C, V_{CCd}/V_{CCQd} = 1.65V~1.95V, V_{CCn} = 2.5V~3.0V)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
I_{CCO1n}	Nand Operating current (Serial Read)	$\overline{CEn}$ = V_{IL}, I_{OUT} = 0 mA , t_{cycle} = 50 ns	—	30	mA
I_{CCO3n}	Nand Operating current (Command input)	I_{OUT} = 0 mA, t_{cycle} = 50 ns	—	30	mA
I_{CCO4n}	Nand Operating current (Data input)	t_{cycle} = 50 ns	—	30	mA
I_{CCO5n}	Nand Operating current (Address input)	t_{cycle} = 50 ns	—	30	mA
I_{CCO7n}	Nand E^2PROM Programming current	—	—	30	mA
I_{CCO8n}	Nand E^2PROM Erasing current	—	—	30	mA
I_{CCS1n}	Nand Standby current	$\overline{CEn}$ = V_{IH}, $\overline{WPn}$ = 0 V or V_{CCn}	—	1	mA
I_{CCS2n}	Nand Standby current	$\overline{CEn}$ = V_{CCn} − 0.2 V, $\overline{WPn}$ = 0 V or V_{CCn}	—	100	μA
I_{IL}	Input leakage current	V_{IN} = 0 V~V_{CCQd} (V_{CCn})	—	±10	μA
I_{OHsd}	LPSDRAM Output high current	V_{OH} = V_{CCQd} − 0.2 V	−0.1	—	mA
I_{OLsd}	LPSDRAM Output low current	V_{OL} = 0.2 V	0.1	—	mA
I_{OHn}	Nand E^2PROM Output high current	V_{OH} = 2.4 V	−0.4	—	mA
I_{OLn}	Nand E^2PROM Output low current	V_{OL} = 0.4 V	2.1	—	mA
I_{LO}	Output leakage current	V_{OUT} = 0 V~V_{CCQd} (V_{CCn}), DQ(I/O) disable	—	±10	μA

Note :

(1) I_{CC1sd} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1sd} is measured on condition that addresses are changed only one time during tCK (min.).

(2) I_{CC4sd} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CCO4sd} is measured condition that addresses are changed only one time during tCK (min.)

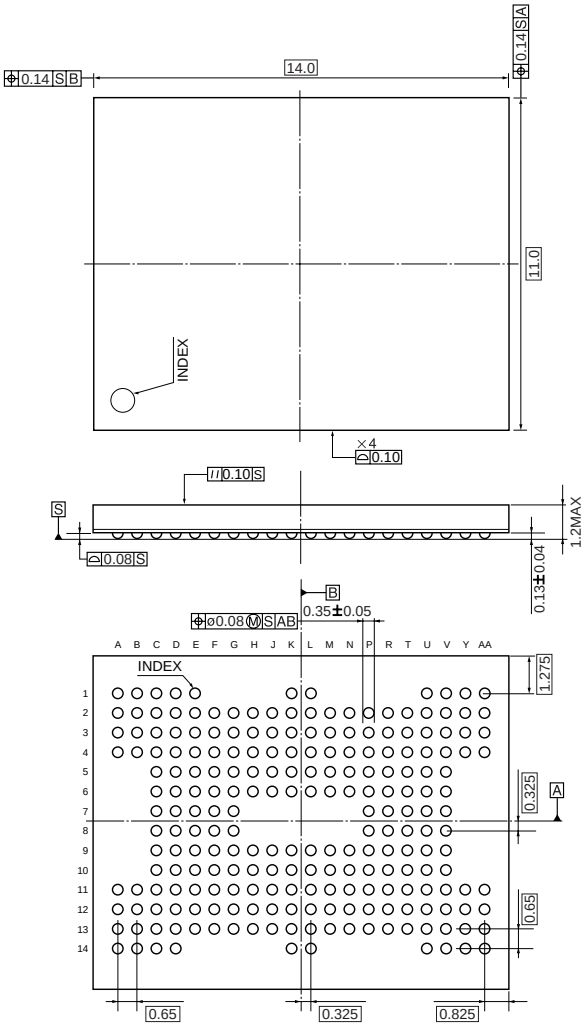
(3) I_{CC5sd} is measured on condition that addresses are changed only one time during tCK (min.).

(4) I_{CC6sd} is specified when self refresh state is maintained long enough under the specified TA condition, after a busy sequence of read and write operations. Ts is surface temperature.

(5) Typical

PACKAGE DIMENSION

P-TFBGA225-1114-0.65BZ Unit: mm



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030519EBA

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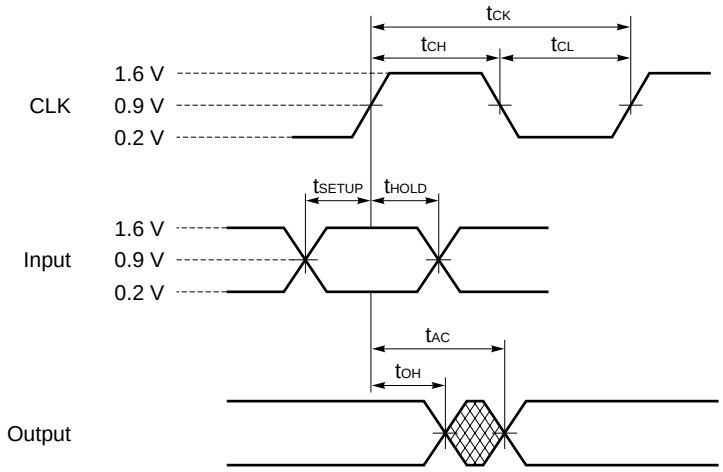
256 Mbits Low Power Synchronous Dynamic RAM

Organization : 4M words × 16 bits × 4 banks

AC Characteristics (TA = –30 to +85°C, VDD, VDDQ = 1.8V ± 0.15V, VSS, VSSQ = 0V)

Test Conditions

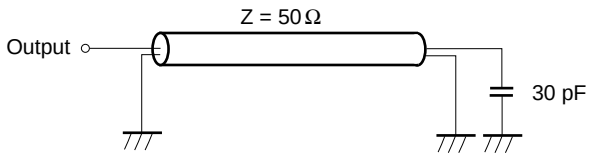
- AC high level input voltage / low level input voltage: 1.6 / 0.2V
- Input timing measurement reference level: 0.9V
- Transition time (Input rise and fall time): 1ns
- Output timing measurement reference level: 0.9V



Synchronous Characteristics

Parameter	Symbol	min.	max.	Unit	Note
Clock cycle time (CL= 2)	tCK2	15	—	ns	
(CL= 3)	tCK3	10	—	ns	
Access time from CLK (CL= 2)	tAC2	—	9	ns	1
(CL= 3)	tAC3	—	7	ns	1
CLK high level width	tCH	3	—	ns	
CLK low level width	tCL	3	—	ns	
Data-out hold time	tOH	3	—	ns	1
Data-out low-impedance time	tLZ	0	—	ns	
Data-out high-impedance time (CL= 2)	tHZ2	3	9	ns	
(CL= 3)	tHZ3	3	7	ns	
Data-in setup time	tDS	2	—	ns	
Data-in hold time	tDH	1	—	ns	
Address setup time	tAS	2	—	ns	
Address hold time	tAH	1	—	ns	
CKE setup time	tCKS	2	—	ns	
CKE hold time	tCKH	1	—	ns	
CKE setup time (Power down exit)	tCKSP	2	—	ns	
Command (/CS, /RAS, /CAS, /WE, UDQM, LDQM) setup time	tCMS	2	—	ns	
Command (/CS, /RAS, /CAS, /WE, UDQM, LDQM) hold time	tCMH	1	—	ns	

Note: 1. Output load.



Output load

Asynchronous Characteristics

Parameter	Symbol	min.	max.	Unit	Notes
ACT to REF/ACT command period (operation)	tRC	90	—	ns	
ACT to REF/ACT command period (refresh)	tRC1	110	—	ns	
Self refresh exit to REF/ACT command period	tRC2	120	—	ns	
ACT to PRE command period	tRAS	60	120000	ns	
PRE to ACT command period	tRP	30	—	ns	
Delay time ACT to READ/WRITE command	tRCD	30	—	ns	
ACT (one) to ACT (another) command period	tRRD	2	—	CLK	
Data-in to PRE command period	tDPL	2	—	CLK	
Data-in to ACT (REF) command period (Auto precharge) (CL = 2)	tDAL2	2CLK + 30	—	ns	
(CL = 3)	tDAL3	2CLK + 30	—	ns	
Mode register set cycle time	tRSC	2	—	CLK	
Transition time	tT	1	30	ns	
Refresh time (8,192 refresh cycles)	tREF	—	64	ms	

Pin Function

CLK (input pin)
CLK is the master clock input. Other inputs signals are referenced to the CLK rising edge.

CKE (input pins)
CKE determine validity of the next CLK (clock). If CKE is high, the next CLK rising edge is valid; otherwise it is invalid. If the CLK rising edge is invalid, the internal clock is not issued and the Mobile RAM suspends operation. When the Mobile RAM is not in burst mode and CKE is negated, the device enters power down mode. During power down mode, CKE must remain low.

/CS (input pins)
/CS low starts the command input cycle. When /CS is high, commands are ignored but operations continue.

/RAS, /CAS, and /WE (input pins)
/RAS, /CAS and /WE have the same symbols on conventional DRAM but different functions. For details, refer to the command table.

A0 to A12 (input pins)
Row Address is determined by A0 to A12 at the CLK (clock) rising edge in the active command cycle. It does not depend on the bit organization.
Column Address is determined by A0 to 8 at the CLK rising edge in the read or write command cycle.
A10 defines the precharge mode. When A10 is high in the precharge command cycle, all banks are precharged; when A10 is low, only the bank selected by BA0 and BA1 is precharged.
When A10 is high in read or write command cycle, the precharge starts automatically after the burst access.

BA0 and BA1 (input pin)
BA0 and BA1 are bank select signal. (See Bank Select Signal Table)

[Bank Select Signal Table]

	BA0	BA1
Bank A	L	L
Bank B	H	L
Bank C	L	H
Bank D	H	H

Remark: H: VIH. L: VIL. ×: VIH or VIL

UDQM and LDQM (input pins)
UDQM and LDQM control upper byte and lower byte I/O buffers, respectively. In read mode, DQM controls the output buffers like a conventional /OE pin. DQM high and DQM low turn the output buffers off and on, respectively. The DQM latency for the read is two clocks. In write mode, DQM controls the word mask. Input data is written to the memory cell if DQM is low but not if DQM is high. The DQM latency for the write is zero.

DQ0 to DQ15 (input/output pins)
DQ pins have the same function as I/O pins on a conventional DRAM.

VDD, VSS, VDDQ, VSSQ (Power supply)
VDD and VSS are power supply pins for internal circuits. VDDQ and VSSQ are power supply pins for the output buffers.

Command Operation

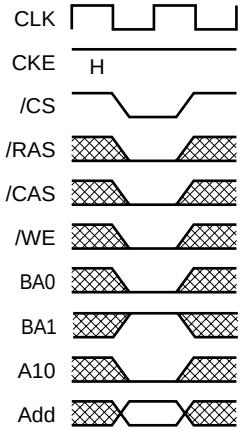
Extended Mode register set command (/CS, /RAS, /CAS, /WE, BA0 = Low, BA1 = High)

The Mobile RAM has an extended mode register that defines low power functions. In this command, A0 through A12 are the data input pins.

After power on, the extended mode register set command must be executed to fix low power functions.

The extended mode register can be set only when all banks are in idle state.

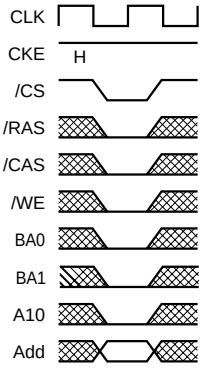
During tRSC following this command, the Mobile RAM can not accept any other commands.



Extended Mode register set command

Mode register set command (/CS, /RAS, /CAS, /WE, BA0, BA1 = Low)

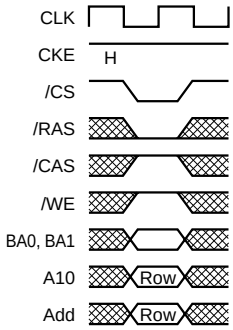
The Mobile RAM has a mode register that defines how the device operates. In this command, A0 through A12 are the data input pins. After power on, the mode register set command must be executed to initialize the device. The mode register can be set only when all banks are in idle state. During tRSC following this command, the Mobile RAM cannot accept any other commands.



Mode register set command

Activate command (/CS, /RAS = Low, /CAS, /WE = High)

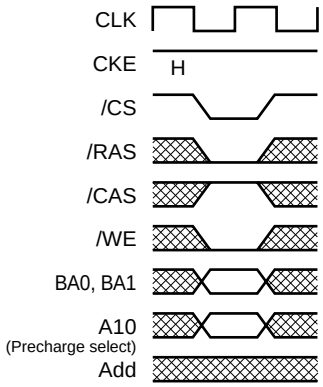
The Mobile RAM has four banks, each with 8,192 rows. This command activates the bank selected by BA0 and BA1 and a row address selected by A0 through A12. This command corresponds to a conventional DRAM's /RAS falling.



Activate command

Precharge command (/CS, /RAS, /WE = Low, /CAS = High)

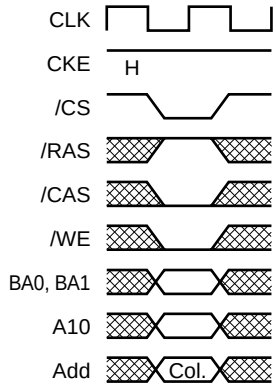
This command begins precharge operation of the bank selected by BA0 and BA1. When A10 is High, all banks are precharged, regardless of BA0 and BA1. When A10 is Low, only the bank selected by BA0 and BA1 is precharged. After this command, the Mobile RAM can't accept the activate command to the precharging bank during tRP (precharge to activate command period). This command corresponds to a conventional DRAM's /RAS rising.



Precharge command

Write command (/CS, /CAS, /WE = Low, /RAS = High)

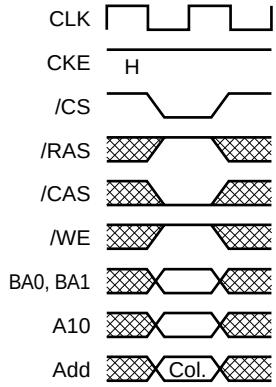
This command sets the burst start address given by the column address to begin the burst write operation. The first write data in burst mode can input with this command with subsequent data on following clocks.



Write command

Read command (/CS, /CAS = Low, /RAS, /WE = High)

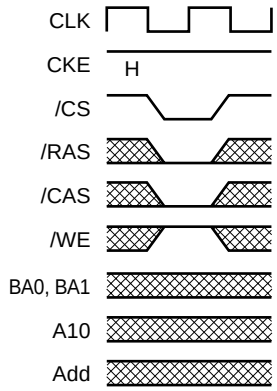
Read data is available after /CAS latency requirements have been met. This command sets the burst start address given by the column address.



Read command

Auto refresh command (/CS, /RAS, /CAS = Low, /WE, CKE = High)

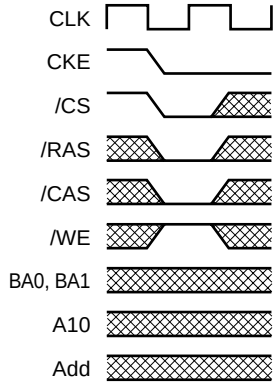
This command is a request to begin the Auto refresh operation. The refresh address is generated internally.
Before executing Auto refresh, all banks must be precharged. After this cycle, all banks will be in the idle (precharged) state and ready for a row activate command. During tRC1 period (from refresh command to refresh or activate command), the Mobile RAM cannot accept any other command.



Auto refresh command

Self refresh entry command (/CS, /RAS, /CAS, CKE = Low, /WE = High)

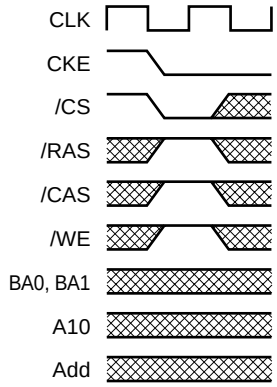
After the command execution, self refresh operation continues while CKE remains low. When CKE goes high, the Mobile RAM exits the self refresh mode. During self refresh mode, refresh interval and refresh operation are performed internally, so there is no need for external control. Before executing self refresh, all banks must be precharged.



Self refresh entry command

Power down entry command (/CS, CKE = Low, /RAS, /CAS, /WE = High)

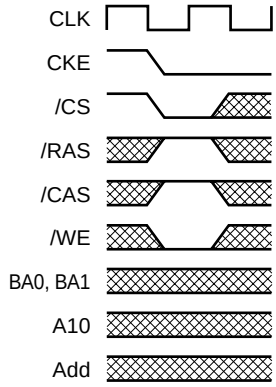
After the command execution, power down mode continues while CKE remains low. When CKE goes high, the Mobile RAM exits the power down mode. Before executing power down, all banks must be precharged.



Power down entry command

Deep power down entry command(/CS, CKE, /WE = Low, /RAS, /CAS = High)

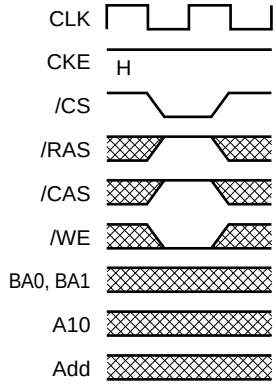
After the command execution, deep power down mode continues while CKE remains low. When CKE goes high, the Mobile RAM exits the deep power down mode. Before executing deep power down, all banks must be precharged.



Deep power down entry command

Burst stop command (/CS = /WE = Low, /RAS, /CAS = High)

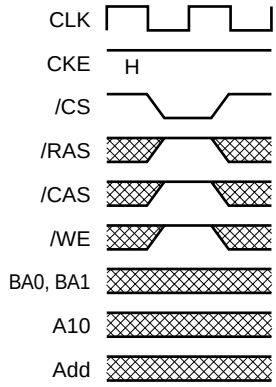
This command can stop the current burst operation.



Burst stop command

No operation (/CS = Low, /RAS, /CAS, /WE = High)

This command is not an execution command. No operations begin or terminate by this command.



No operation

Truth Table

Command Truth Table

		CKE									A11,A12
Function	Symbol	n – 1	n	/CS	/RAS	/CAS	/WE	BA1	BA0	A10	A9 - A0
Device deselect	DESL	H	×	H	×	×	×	×	×	×	×
No operation	NOP	H	×	L	H	H	H	×	×	×	×
Burst stop	BST	H	H	L	H	H	L	×	×	×	×
Read	READ	H	×	L	H	L	H	V	V	L	V
Read with auto precharge	READA	H	×	L	H	L	H	V	V	H	V
Write	WRIT	H	×	L	H	L	L	V	V	L	V
Write with auto precharge	WRITA	H	×	L	H	L	L	V	V	H	V
Bank activate	ACT	H	×	L	L	H	H	V	V	V	V
Precharge select bank	PRE	H	×	L	L	H	L	V	V	L	×
Precharge all banks	PALL	H	×	L	L	H	L	×	×	H	×
Mode register set	MRS	H	×	L	L	L	L	L	L	L	V
Extended mode register set	EMRS	H	×	L	L	L	L	H	L	L	V

Remark: H: VIH. L: VIL. ×: VIH or VIL, V = Valid data

DQM Truth Table

		CKE		DQM	
Function	Symbol	n – 1	n	U	L
Data write / output enable	ENB	H	×	L	L
Data mask / output disable	MASK	H	×	H	H
Upper byte write enable / output enable	ENBU	H	×	L	×
Lower byte write enable / output enable	ENBL	H	×	×	L
Upper byte write inhibit / output disable	MASKU	H	×	H	×
Lower byte write inhibit / output disable	MASKL	H	×	×	H

Remark: H: VIH. L: VIL. ×: VIH or VIL

CKE Truth Table

			CKE						
Current state	Function	Symbol	n – 1	n	/CS	/RAS	/CAS	/WE	Address
Activating	Clock suspend mode entry		H	L	×	×	×	×	×
Any	Clock suspend mode		L	L	×	×	×	×	×
Clock suspend	Clock suspend mode exit		L	H	×	×	×	×	×
Idle	Auto refresh command	REF	H	H	L	L	L	H	×
Idle	Self refresh entry	SELF	H	L	L	L	L	H	×
Idle	Power down entry	PD	H	L	L	H	H	H	×
			H	L	H	×	×	×	×
Idle	Deep power down entry	DPD	H	L	L	H	H	L	×
Self refresh	Self refresh exit		L	H	L	H	H	H	×
			L	H	H	×	×	×	×
Power down	Power down exit		L	H	L	H	H	H	×
			L	H	H	×	×	×	×
Deep power down	Deep power down exit		L	H	×	×	×	×	×

Remark: H: VIH. L: VIL. ×: VIH or VIL

Function Truth Table

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Idle	H	×	×	×	×	DESL	Nop	
	L	H	H	H	×	NOP	Nop	
	L	H	H	L	×	BST	Nop	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	→ Row activating	
	L	L	H	L	BA, A10	PRE/PALL	Nop	
	L	L	L	H	×	REF	Auto refresh	
	L	L	L	L	OC, BA1= L	MRS	Mode register set	
	L	L	L	L	OC, BA1= H	EMRS	Extended mode register set	
Row active	H	×	×	×	×	DESL	Nop	
	L	H	H	H	×	NOP	Nop	
	L	H	H	L	×	BST	Nop	
	L	H	L	H	BA, CA, A10	READ/READA	Begin read	3
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	Begin write	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	Precharge/Precharge all banks	4
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Read	H	×	×	×	×	DESL	Continue burst to end → Row active	
	L	H	H	H	×	NOP	Continue burst to end → Row active	
	L	H	H	L	×	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, begin new read	5
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, begin write	5, 6
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst → Precharging	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Write	H	×	×	×	×	DESL	Continue burst to end → Write recovering	
	L	H	H	H	×	NOP	Continue burst to end → Write recovering	
	L	H	H	L	×	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, start read : Determine AP	5, 6
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, new write : Determine AP	5
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst → Precharging	7
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Read with auto precharge	H	×	×	×	×	DESL	Continue burst to end → Precharging	
	L	H	H	H	×	NOP	Continue burst to end → Precharging	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Write with auto precharge	H	×	×	×	×	DESL	Continue burst to end → Write recovering with auto precharge	
	L	H	H	H	×	NOP	Continue burst to end → Write recovering with auto precharge	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Precharging	H	×	×	×	×	DESL	Nop → Enter idle after tRP	
	L	H	H	H	×	NOP	Nop → Enter idle after tRP	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	Nop → Enter idle after tRP	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Row activating	H	×	×	×	×	DESL	Nop → Enter bank active after tRCD	
	L	H	H	H	×	NOP	Nop → Enter bank active after tRCD	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2, 8
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Write recovering	H	×	×	×	×	DESL	Nop → Enter row active after tDPL	
	L	H	H	H	×	NOP	Nop → Enter row active after tDPL	
	L	H	H	L	×	BST	Nop → Enter row active after tDPL	
	L	H	L	H	BA, CA, A10	READ/READA	Begin read	6
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	Begin new write	
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Write recovering	H	×	×	×	×	DESL	Nop → Enter precharge after tDPL	
with auto	L	H	H	H	×	NOP	Nop → Enter precharge after tDPL	
precharge	L	H	H	L	×	BST	Nop → Enter row active after tDPL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	2, 6
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Refresh	H	×	×	×	×	DESL	Nop → Enter idle after tRC1	
	L	H	H	H	×	NOP	Nop → Enter idle after tRC1	
	L	H	H	L	×	BST	Nop → Enter idle after tRC1	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Mode register	H	×	×	×	×	DESL	Nop → Enter idle after tRSC	
accessing	L	H	H	H	×	NOP	Nop → Enter idle after tRSC	
	L	H	H	L	×	BST	Nop → Enter idle after tRSC	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Extended mode	H	×	×	×	×	DESL	Nop → Enter idle after tRSC	
register	L	H	H	H	×	NOP	Nop → Enter idle after tRSC	
accessing	L	H	H	L	×	BST	Nop → Enter idle after tRSC	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	

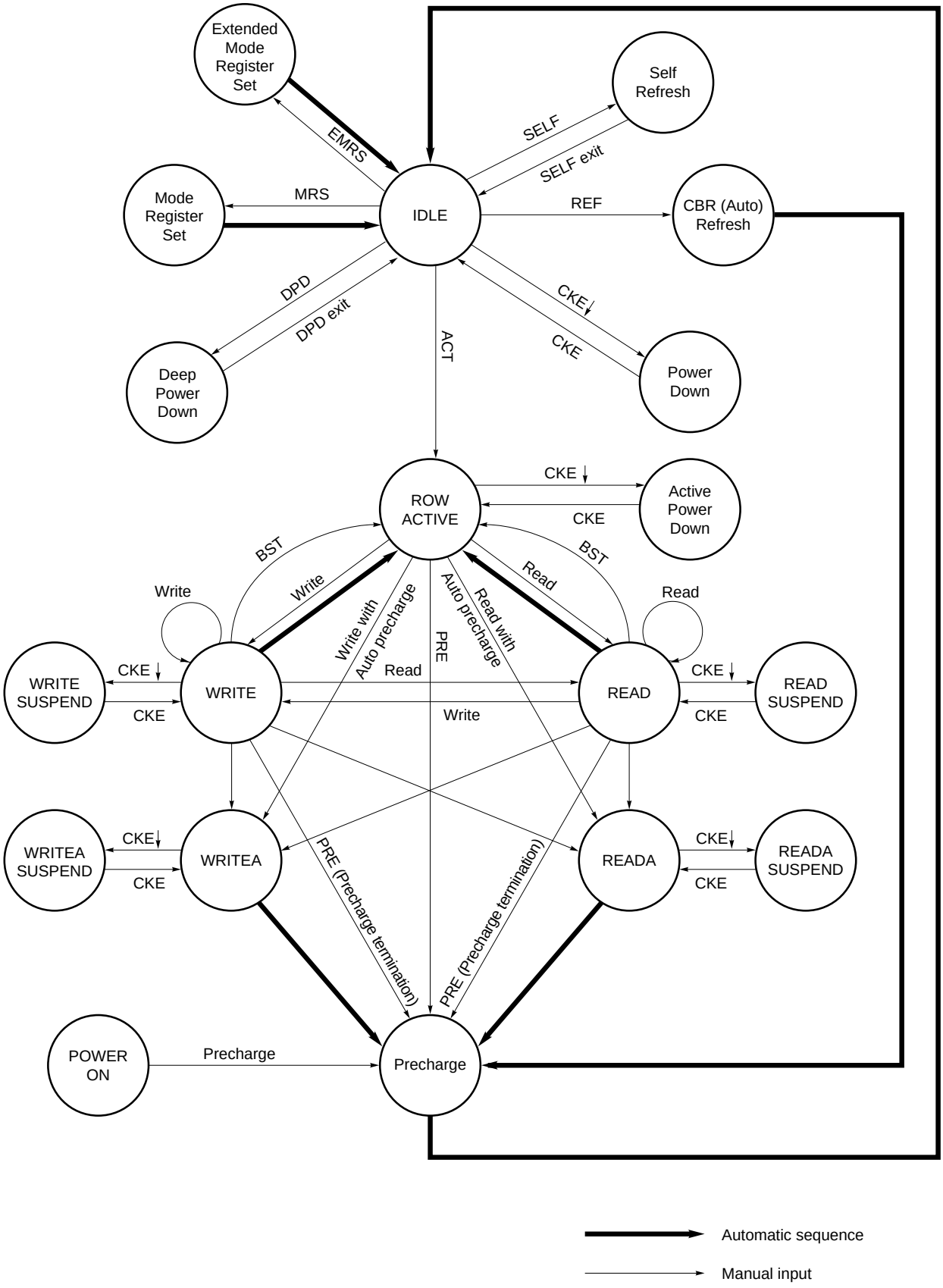
Remark: H: VIH. L: VIL. ×: VIH or VIL, V = Valid data

BA: Bank Address, CA: Column Address, RA: Row Address, OC: Op-Code

Notes: 1. All entries assume that CKE is active (CKE_{n-1}=CKE_n=H).

2. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
3. Illegal if tRCD is not satisfied.
4. Illegal if tRAS is not satisfied.
5. Must satisfy burst interrupt condition.
6. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
7. Must mask preceding data which don't satisfy tDPL.
8. Illegal if tRRD is not satisfied.

Simplified State Diagram



Initialization

The synchronous DRAM is initialized in the power-on sequence according to the following.

(1) To stabilize internal circuits, when power is applied, a 200 μs or longer pause must precede any signal toggling.

(2) After the pause, all banks must be precharged using the Precharge command (The Precharge all banks command is convenient).

(3) Once the precharge is completed and the minimum tRP is satisfied, two or more Auto refresh must be performed.

(4) Both the mode register and the extended mode register must be programmed. After the mode register set cycle or the extended mode register set cycle, tRSC (2 CLK minimum) pause must be satisfied.

Remarks:

1 The sequence of Auto refresh, mode register programming and extended mode register programming above may be transposed.

2 CKE and DQM must be held high until the Precharge command is issued to ensure data-bus High-Z.

Programming Mode Registers

The mode register and extended mode register are programmed by the Mode register set command and Extended mode register command, respectively using address bits A12 through A0, BA0 and BA1 as data inputs. The registers retain data until they are re-programmed, or the device enters into the deep power down or the device loses power.

Mode register

The mode register has three fields;

Options	:	A12 through A7
/CAS latency	:	A6 through A4
Wrap type	:	A3
Burst length	:	A2 through A0

Following mode register programming, no command can be issued before at least 2 CLK have elapsed.

/CAS Latency

/CAS latency is the most critical of the parameters being set. It tells the device how many clocks must elapse before the data will be available. The value is determined by the frequency of the clock and the speed grade of the device.

Burst Length

Burst Length is the number of words that will be output or input in a read or write cycle. After a read burst is completed, the output bus will become High-Z. The burst length is programmable as 1, 2, 4, 8 or full page.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. This order is programmable as either “Sequential” or “Interleave”. The method chosen will depend on the type of CPU in the system.
Some microprocessor cache systems are optimized for sequential addressing and others for interleaved addressing. “Burst Length Sequence” shows the addressing sequence for each burst length using them. Both sequences support bursts of 1, 2, 4 and 8. Additionally, sequence supports the full page length.

Extended Mode Register

The extended mode register has four fields;

Options	: A12 through A7
Auto Temperature Compensated Self Refresh	: A9
Drive Strength	: A6 through A5
Partial Array Self Refresh	: A2 through A0

Following extended mode register programming, no command can be issued before at least 2 CLK have elapsed.

Drive Strength

By setting specific parameter on A6 and A5, driving capability of data output drivers is selected.

Auto Temperature Compensated Self Refresh (ATCSR)

With the built-in temperature sensor, the internal self refresh frequency is controlled autonomously.

Partial Array Self Refresh

Memory array size to be refreshed during self refresh operation is programmable in order to reduce power. Data outside the defined area will not be retained during self refresh.

Mode Register Definition

BA0	BA1	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	0	LTMODE			WT	BL			Mode Register Set

Latency mode	Bits6-4	/CAS latency
	000	R
	001	R
	010	2
	011	3
	100	R
	101	R
	110	R
	111	R

Burst length	Bits2-0	WT = 0	WT = 1
	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	Full page	R

Wrap type		
	0	Sequential
	1	Interleave

BA0	BA1	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	1	0	0	0	ATCSR	0	0	DS		0	0	PASR			Extended Mode Register Set

ATCSR	Bits9	ATCSR
	0	Enable
	1	R

Partial Array Self Refresh	Bits2-0	Refresh Array
	000	All banks
	001	Bank A & Bank B (BA1=0)
	010	Bank A (BA0=BA1=0)
	011	R
	100	R
	101	R
	110	R
	111	R

Drive Strength	Bits6-5	Strength
	00	Normal
	01	1/2 strength
	10	1/4 strength
	11	1/8 strength

Remark R : Reserved

Burst Length and Sequence

[Burst of Two]

Starting address (column address A0, binary)	Sequential addressing sequence (decimal)	Interleave addressing sequence (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

[Burst of Four]

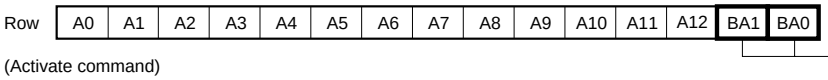
Starting address (column address A1–A0, binary)	Sequential addressing sequence (decimal)	Interleave addressing sequence (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

[Burst of Eight]

Starting address (column address A2–A0, binary)	Sequential addressing sequence (decimal)	Interleave addressing sequence (decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

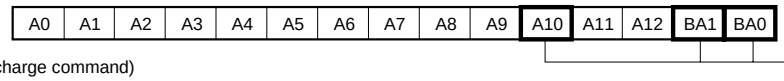
Full page burst is an extension of the above tables of sequential addressing, with the length being 512.

Address Bits of Bank-Select and Precharge



(Activate command)

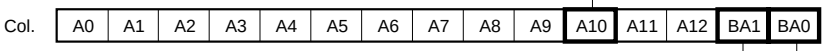
BA1	BA0	Result
0	0	**Select Bank A "Activate" command**
0	1	**Select Bank B "Activate" command**
1	0	**Select Bank C "Activate" command**
1	1	**Select Bank D "Activate" command**



(Precharge command)

A10	BA1	BA0	Result
0	0	0	**Precharge Bank A**
0	0	1	**Precharge Bank B**
0	1	0	**Precharge Bank C**
0	1	1	**Precharge Bank D**
1	x	x	**Precharge All Banks**

x : Don't care



(/CAS strobes)

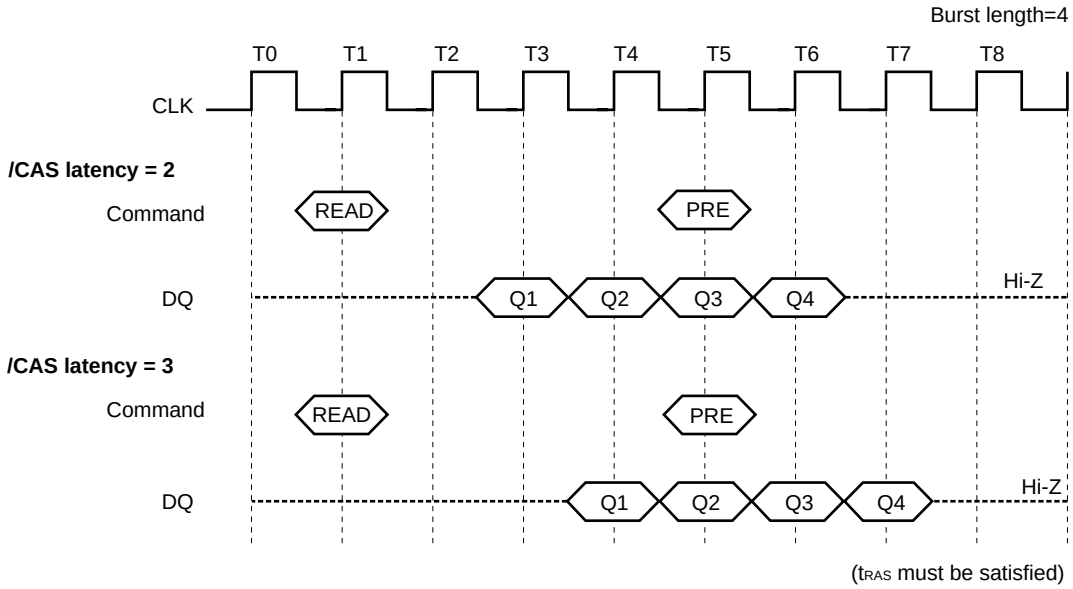
0	**disables Auto-Precharge (End of Burst)**
1	**enables Auto-Precharge (End of Burst)**

BA1	BA0	Result
0	0	**enables Read/Write commands for Bank A**
0	1	**enables Read/Write commands for Bank B**
1	0	**enables Read/Write commands for Bank C**
1	1	**enables Read/Write commands for Bank D**

Operation

Precharge

The precharge command can be issued anytime after tRAS min. is satisfied. Soon after the precharge command is issued, precharge operation performed and the synchronous DRAM enters the idle state after tRP is satisfied. The parameter tRP is the time required to perform the precharge. The earliest timing in a read cycle that a precharge command can be issued without losing any data in the burst is as follows.



Precharge

In order to write all data to the memory cell correctly, the asynchronous parameter tDPL must be satisfied. The tDPL (min.) specification defines the earliest time that a precharge command can be issued. Minimum number of clocks is calculated by dividing tDPL (min.) with clock cycle time. In summary, the precharge command can be issued relative to reference clock that indicates the last data word is valid. In the following table, minus means clocks before the reference; plus means time after the reference.

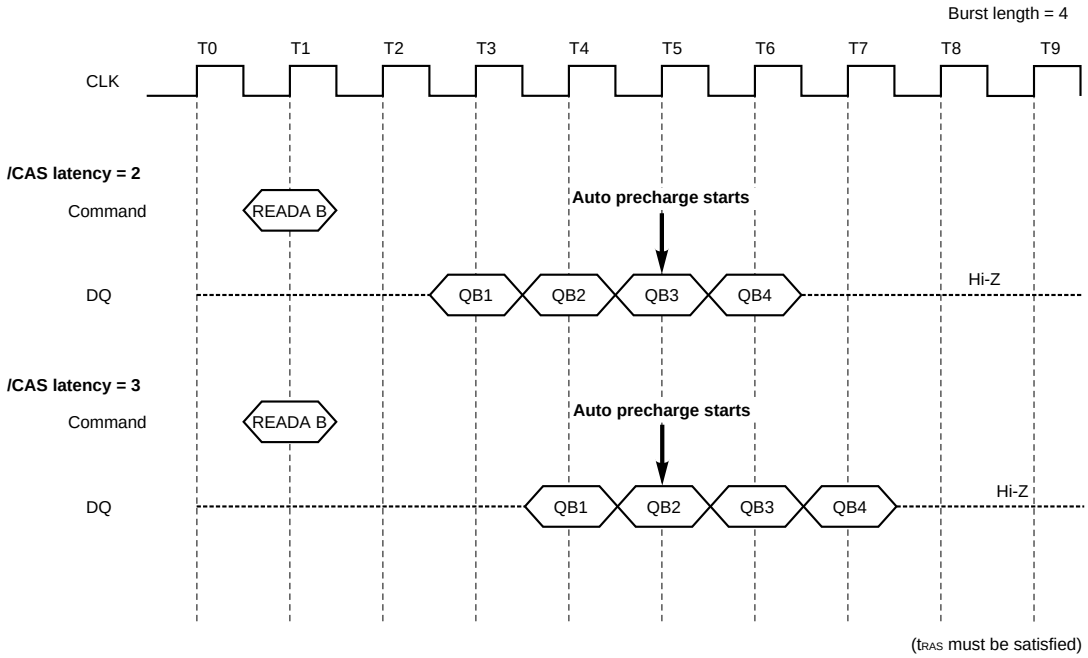
/CAS latency	Read	Write
2	-1	+tDPL(min.)
3	-2	+tDPL(min.)

Auto Precharge

During a read or write command cycle, A10 controls whether auto precharge is selected. A10 high in the Read or Write command (Read with Auto precharge command or Write with Auto precharge command), auto precharge is selected and begins automatically. The tRAS must be satisfied with a read with auto precharge or a write with auto precharge operation. In addition, the next activate command to the bank being precharged cannot be executed until the precharge cycle ends.
In read cycle, once auto precharge has started, an activate command to the bank can be issued after tRP has been satisfied.
In write cycle, the tDAL must be satisfied to issue the next activate command to the bank being precharged.
The timing that begins the auto precharge cycle depends on whether read or write cycle.

Read with Auto Precharge

During a read cycle, the auto precharge begins one clock earlier (/CAS latency of 2) or two clocks earlier (/CAS latency of 3) the last data word output.

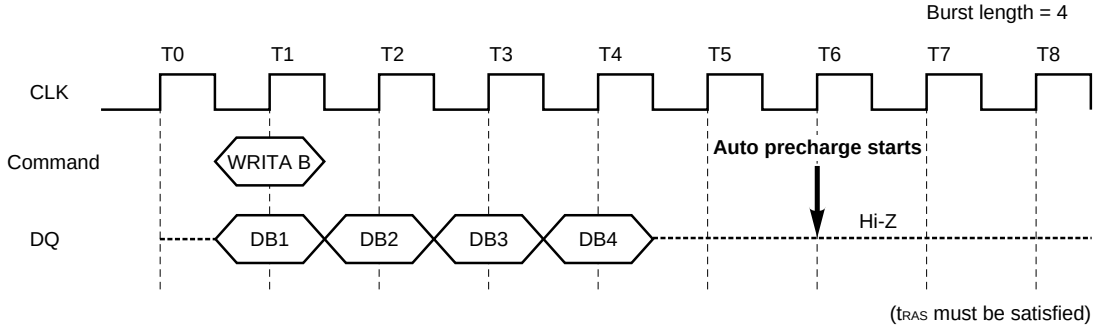


Read with Auto Precharge

Remark: READA means Read with Auto precharge

Write with Auto Precharge

During a write cycle, the auto precharge starts at the timing that is equal to the value of the tDPL (min.) after the last data word input to the device.



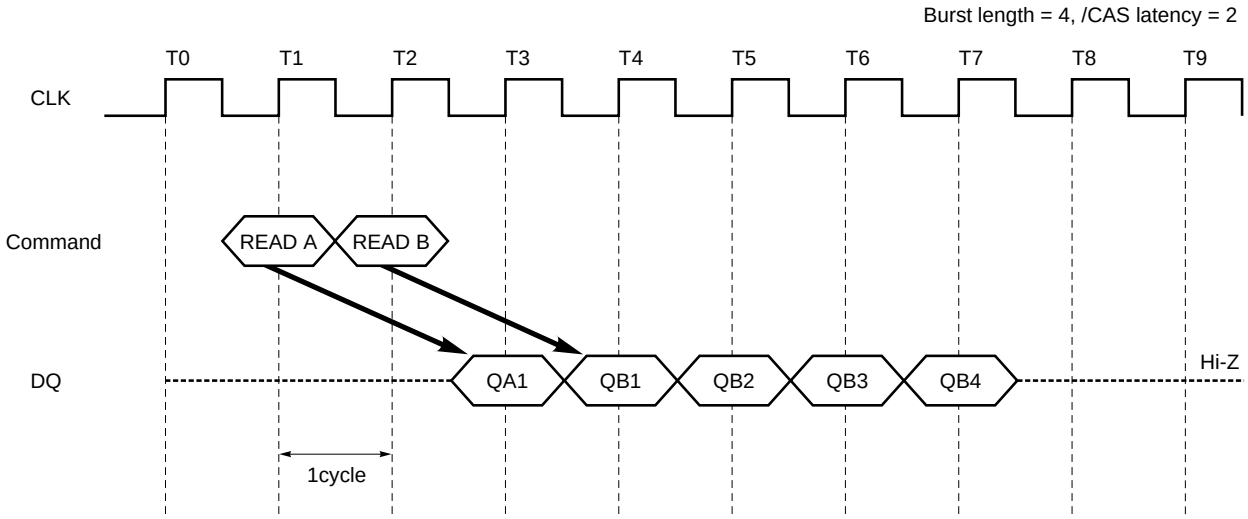
Write with Auto Precharge

Remark: WRITA means Write with Auto Precharge

Read / Write Command Interval

Read to Read Command Interval

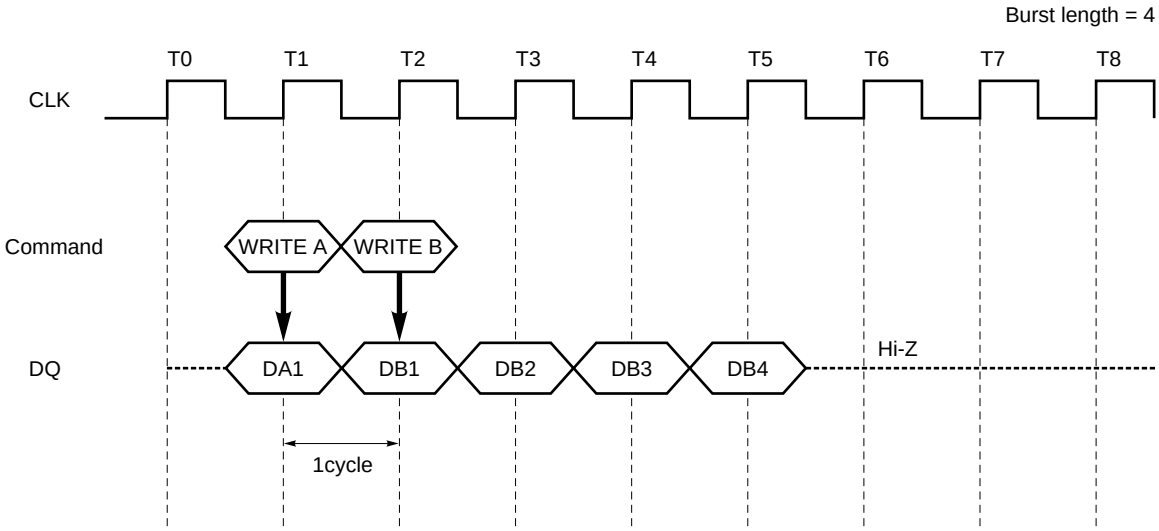
During a read cycle, when new Read command is issued, it will be effective after /CAS latency, even if the previous read operation does not completed. READ will be interrupted by another READ. The interval between the commands is 1 cycle minimum. Each Read command can be issued in every clock without any restriction.



Read to Read Command Interval

Write to Write Command Interval

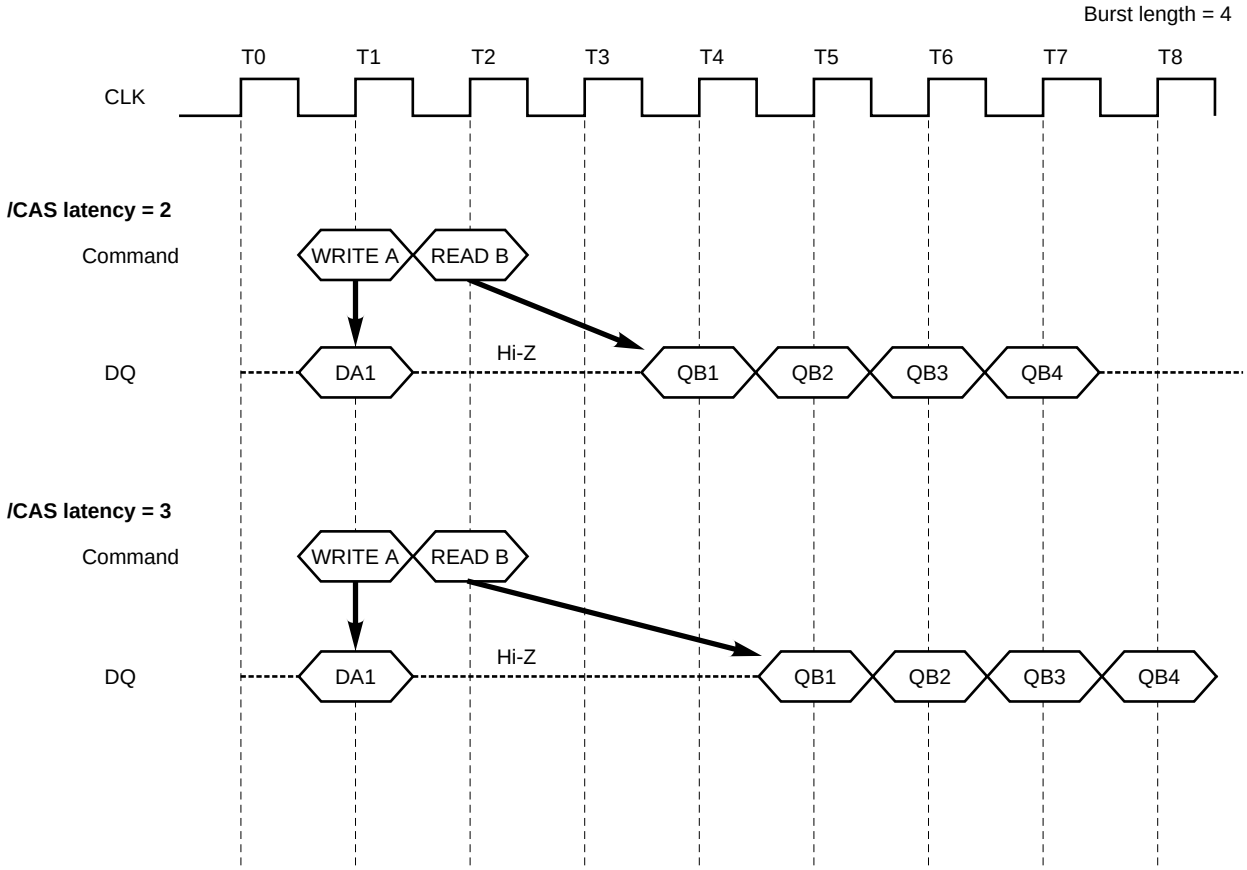
During a write cycle, when a new Write command is issued, the previous burst will terminate and the new burst will begin with a new Write command. WRITE will be interrupted by another WRITE. The interval between the commands is minimum 1 cycle. Each Write command can be issued in every clock without any restriction.



Write to Write Command Interval

Write to Read Command Interval

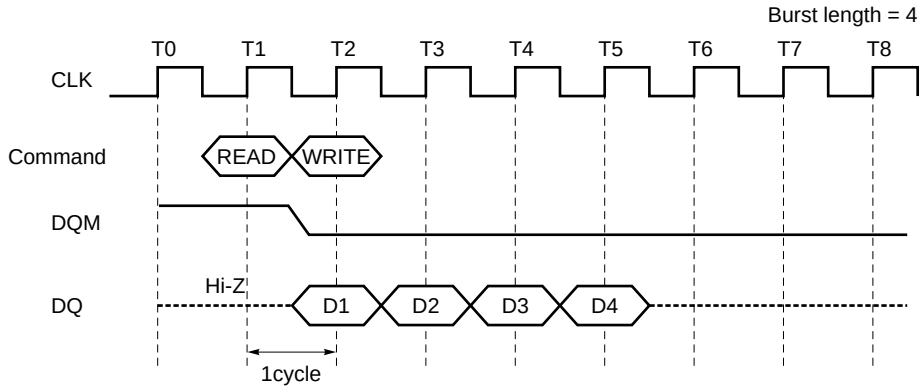
Write command and Read command interval is also 1 cycle. Only the write data before Read command will be written. The data bus must be High-Z at least one cycle prior to the first DOUT.



Write to Read Command Interval

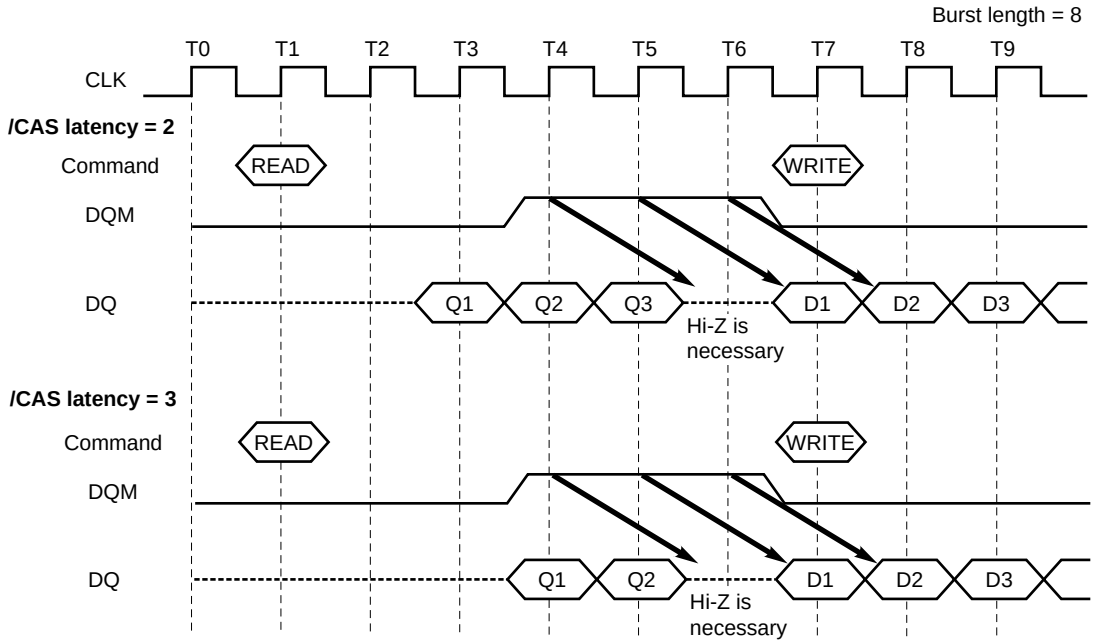
Read to Write Command Interval

During a read cycle, READ can be interrupted by WRITE. The Read and Write command interval is 1 cycle minimum. There is a restriction to avoid data conflict. The Data bus must be High-Z using DQM before WRITE.



Read to Write Command Interval 1

READ can be interrupted by WRITE. DQM must be High at least 3 clocks prior to the Write command.



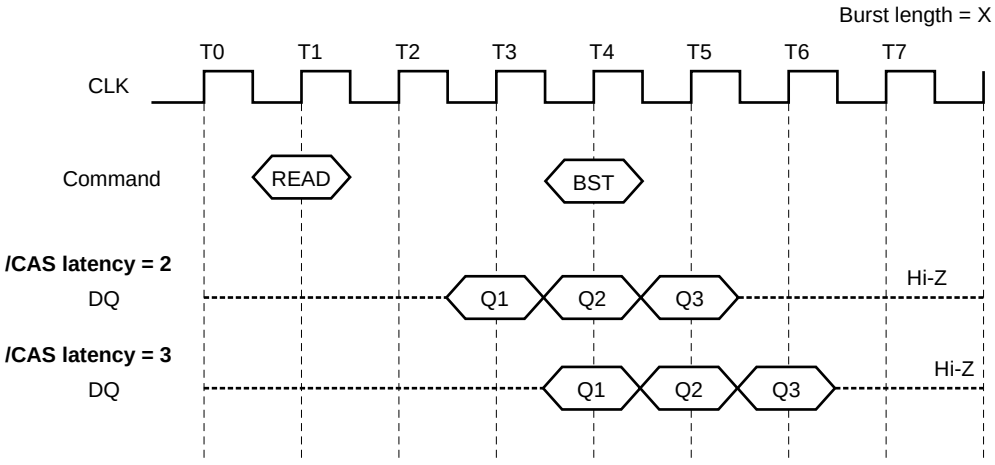
Read to Write Command Interval 2

Burst Termination

There are two methods to terminate a burst operation other than using a Read or a Write command. One is the burst stop command and the other is the precharge command.

Burst Termination in READ Cycle

During a read cycle, when the burst stop command is issued, the burst read data are terminated and the data bus goes to High-Z after the /CAS latency from the burst stop command.

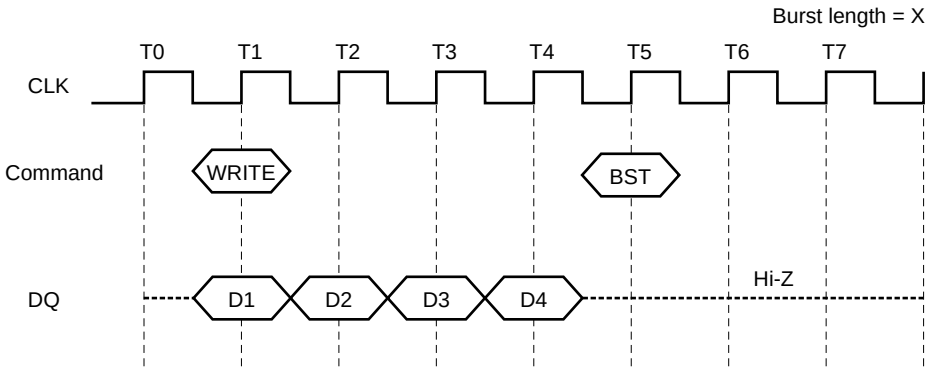


Burst Termination in READ Cycle

Remark: BST: Burst stop command

Burst Termination in WRITE Cycle

During a write cycle, when the burst stop command is issued, the burst write data are terminated and data bus goes to High-Z at the same clock with the burst stop command.



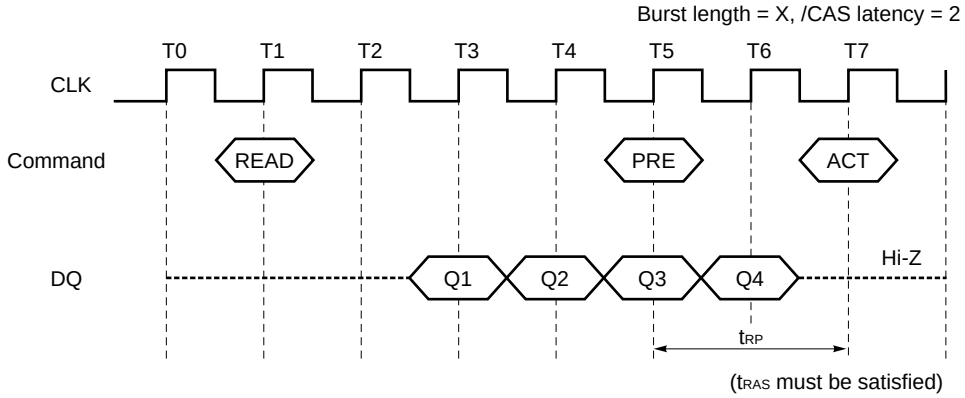
Burst Termination in WRITE Cycle

Remark: BST: Burst stop command

Precharge Termination in READ Cycle

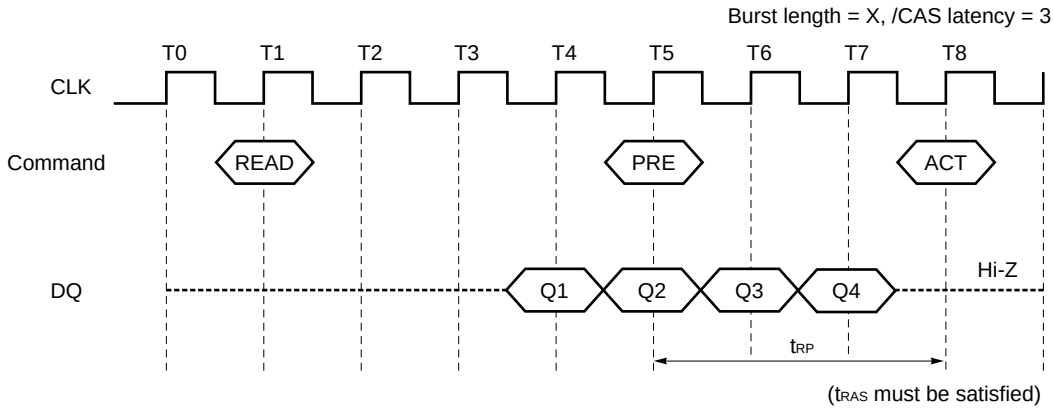
During a read cycle, the burst read operation is terminated by a precharge command. When the precharge command is issued, the burst read operation is terminated and precharge starts. The same bank can be activated again after tRP from the precharge command. To issue a precharge command, tRAS must be satisfied.

When /CAS latency is 2, the read data will remain valid until one clock after the precharge command.



Precharge Termination in READ Cycle (CL = 2)

When /CAS latency is 3, the read data will remain valid until two clocks after the precharge command.

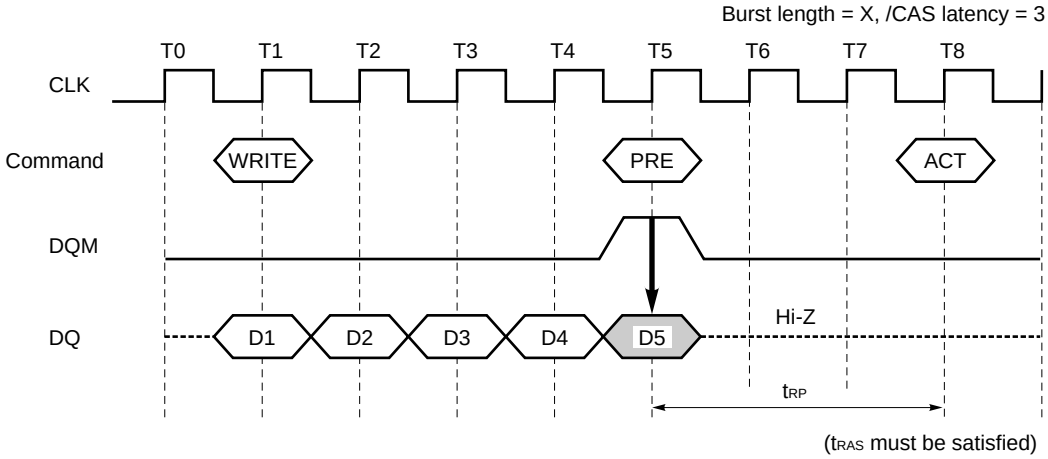


Precharge Termination in READ Cycle (CL = 3)

Precharge Termination in WRITE Cycle

During a write cycle, the burst write operation is terminated by a precharge command. When the precharge command is issued, the burst write operation is terminated and precharge starts. The same bank can be activated again after tRP from the precharge command. To issue a precharge command, tRAS must be satisfied.

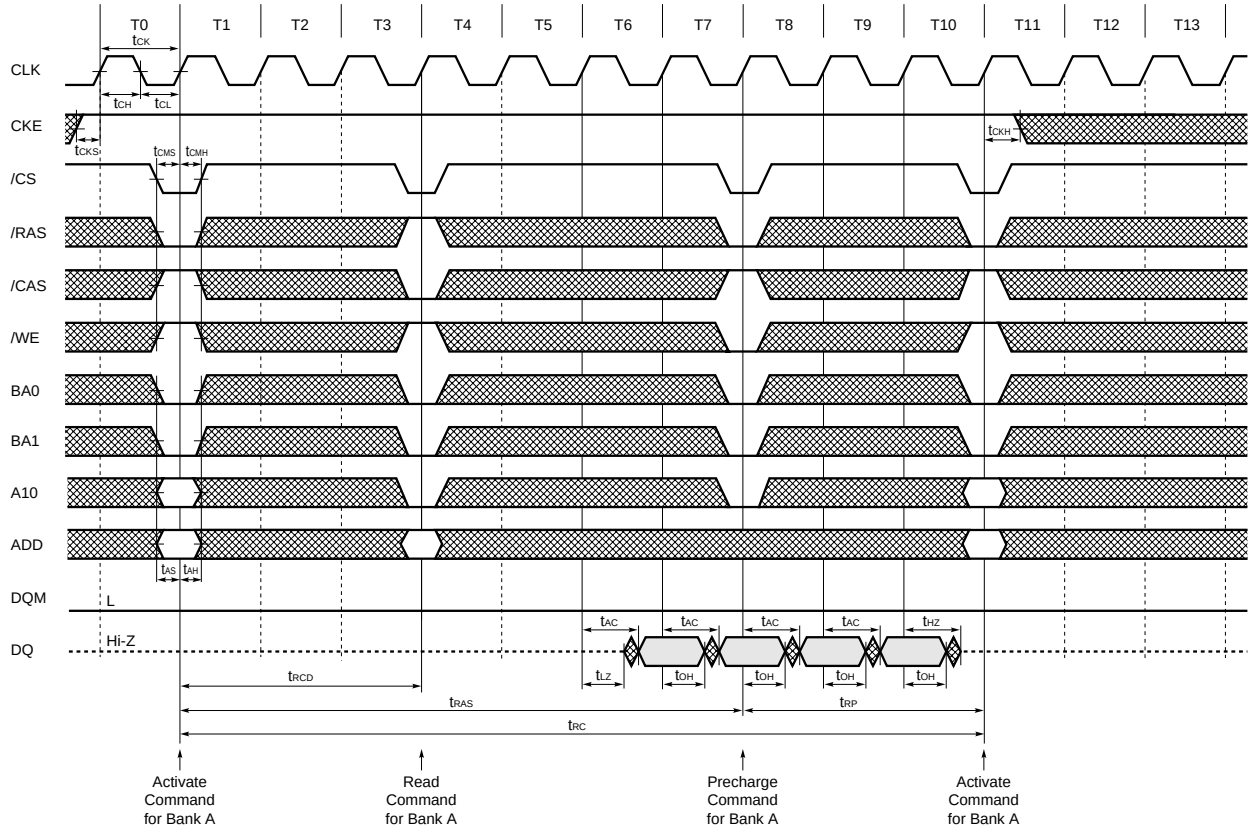
The write data written prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command. To prevent this from happening, DQM must be high at the same clock as the precharge command. This will mask the invalid data.



Precharge Termination in WRITE Cycle

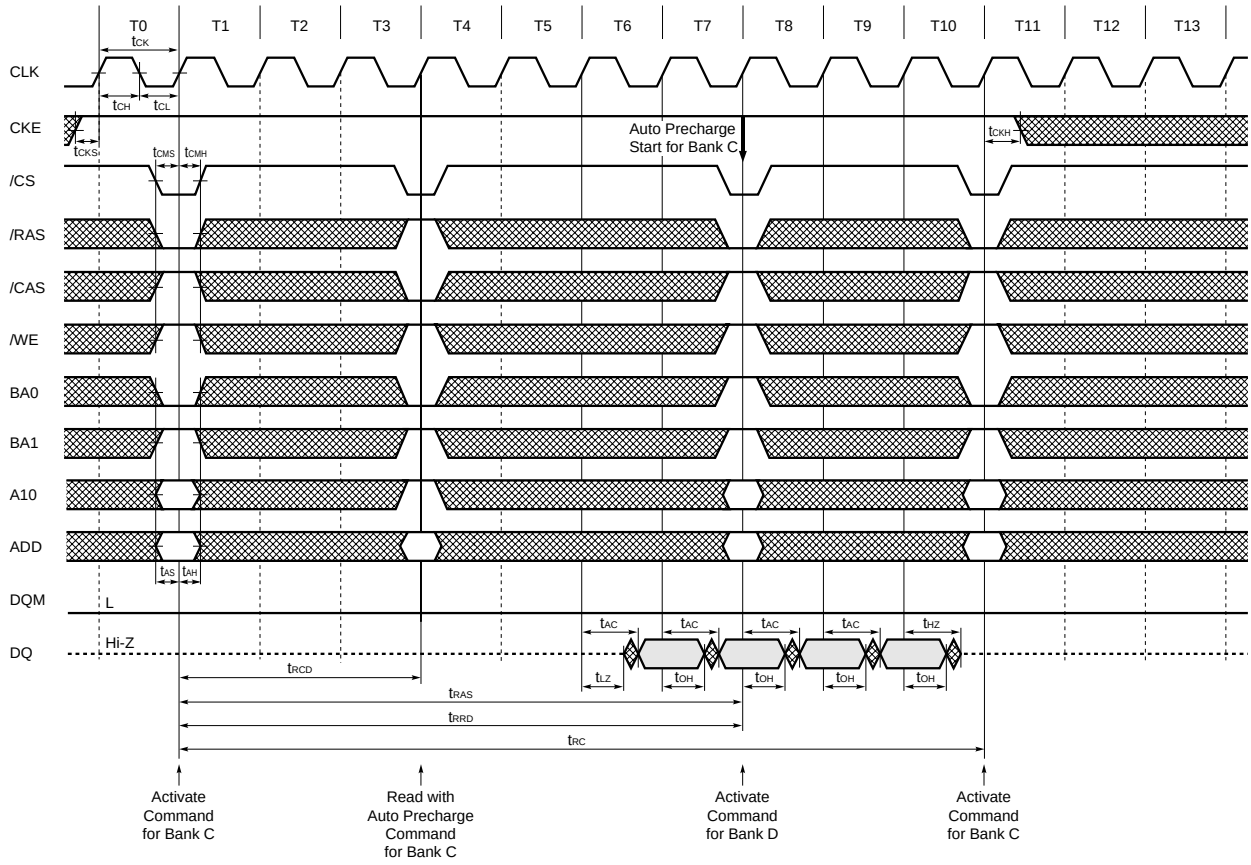
Timing Waveforms

AC Parameters for Read Timing with Manual Precharge



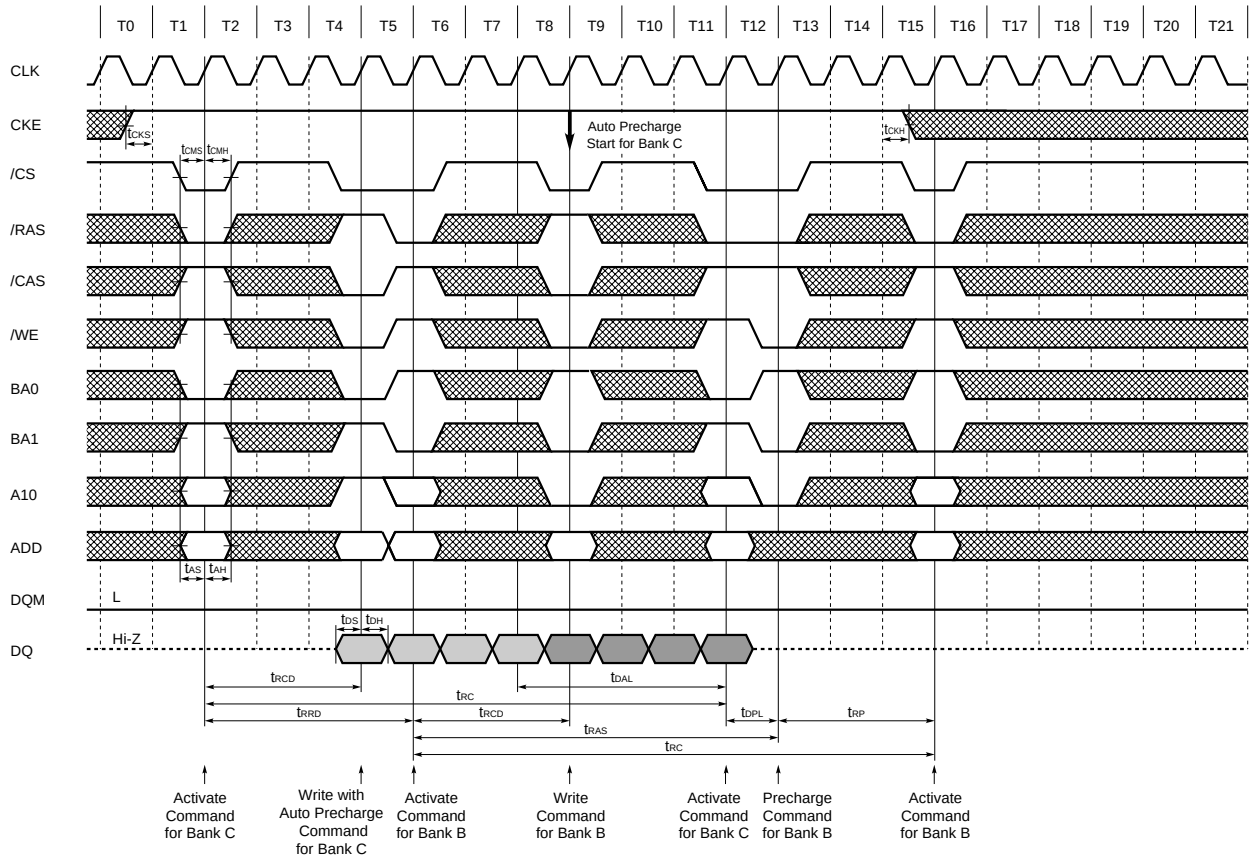
[Burst Length = 4, /CAS Latency = 3]

AC Parameters for Read Timing with Auto Precharge



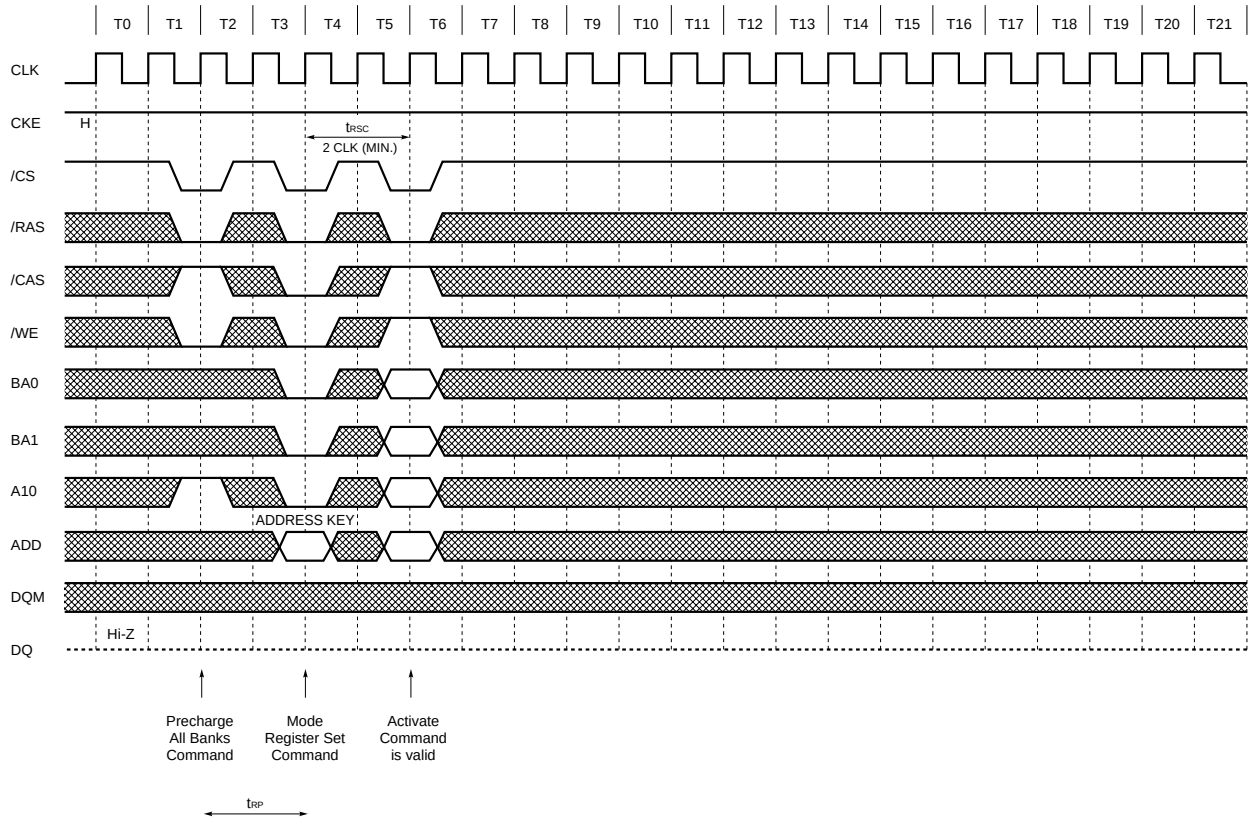
[Burst Length = 4, /CAS Latency = 3]

AC Parameters for Write Timing

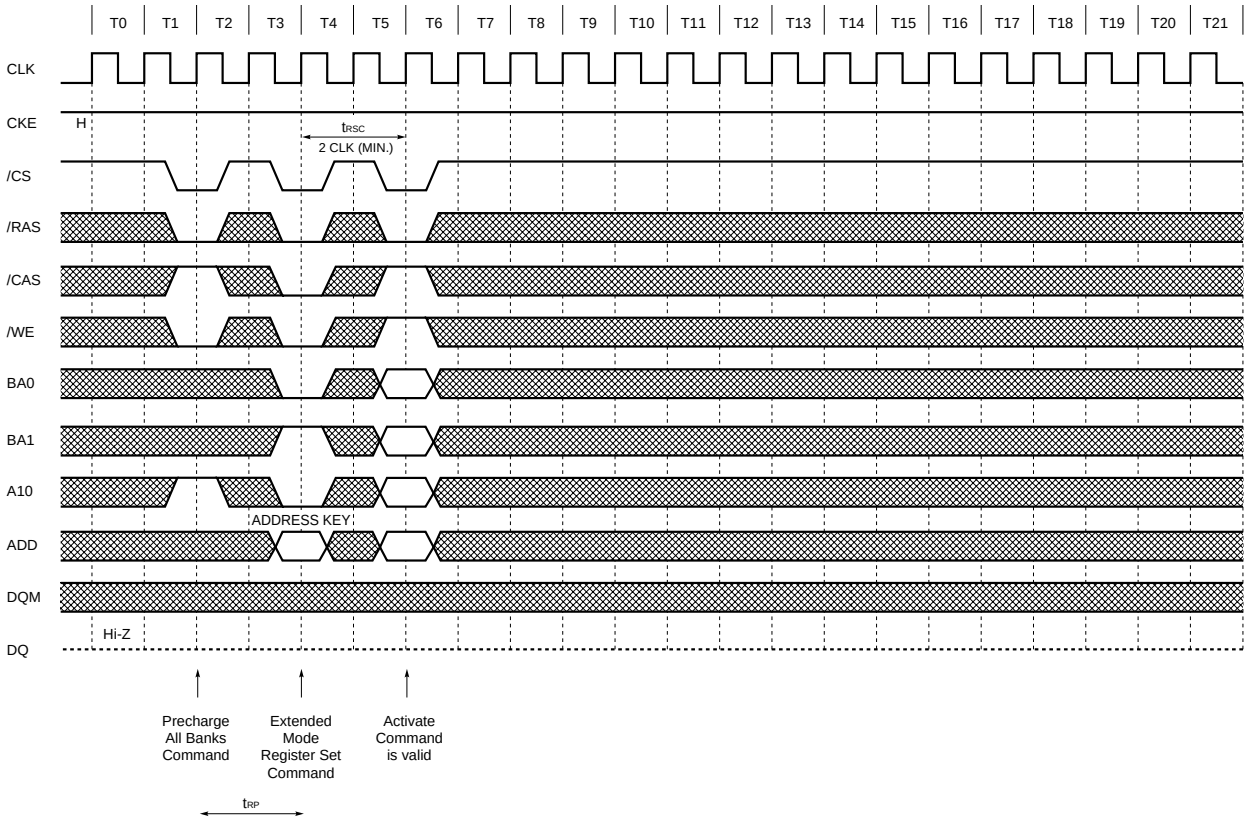


[Burst Length = 4]

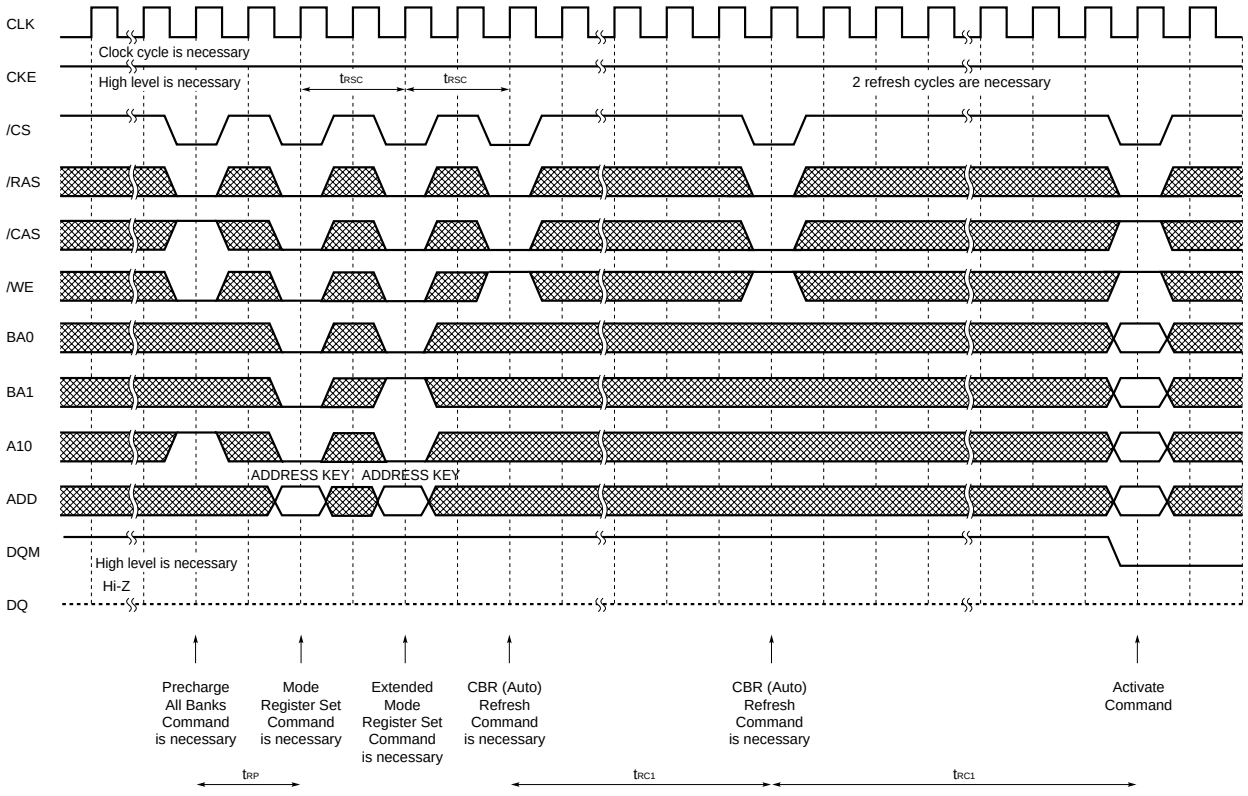
Mode Register Set



Extended Mode Register Set

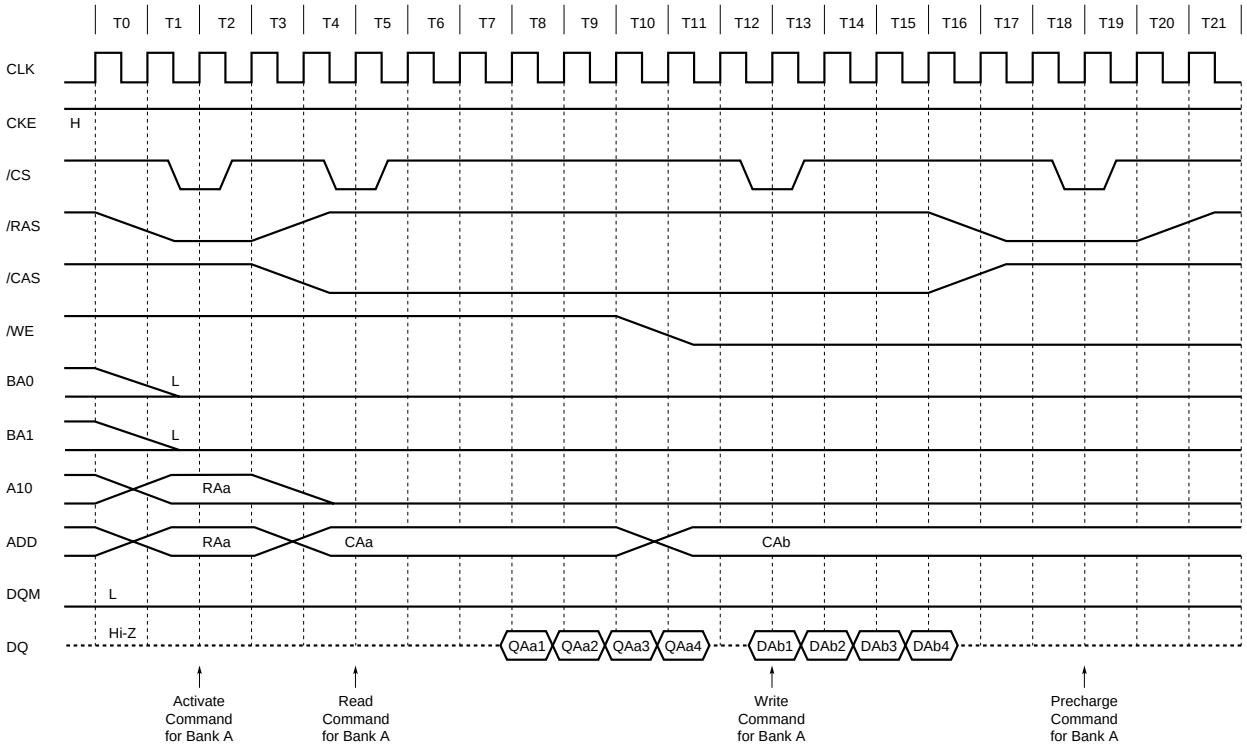


Power On Sequence



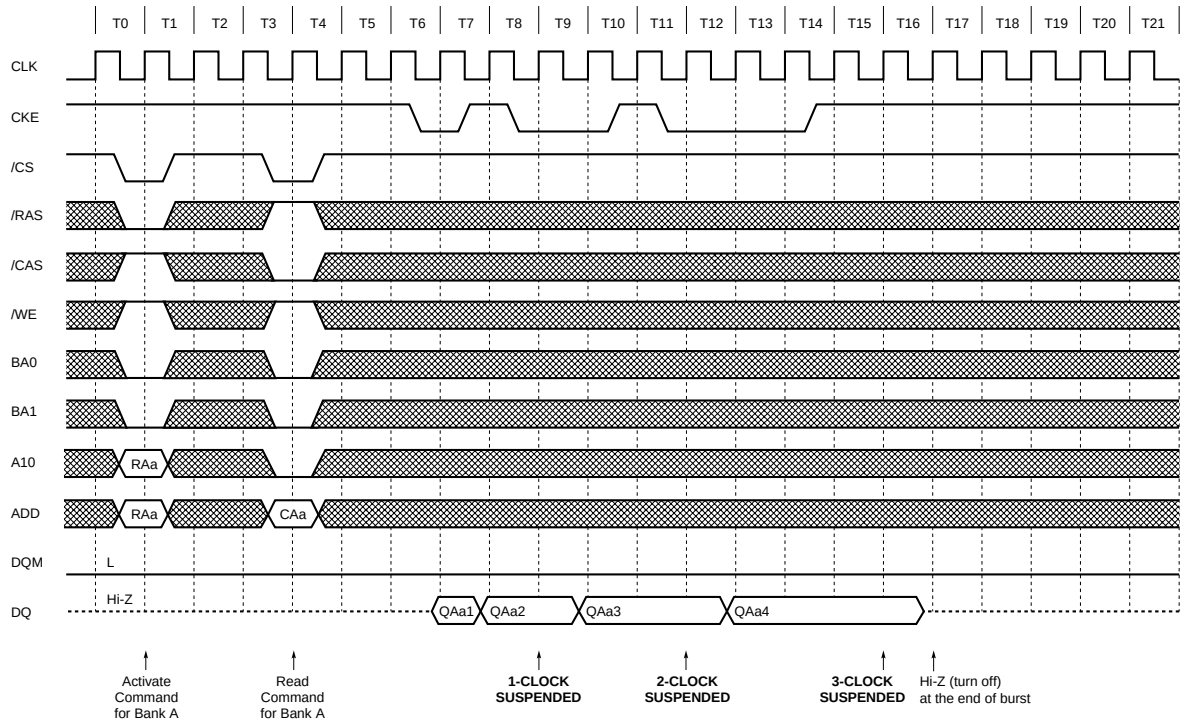
/CS Function

Only /CS signal needs to be issued at minimum rate

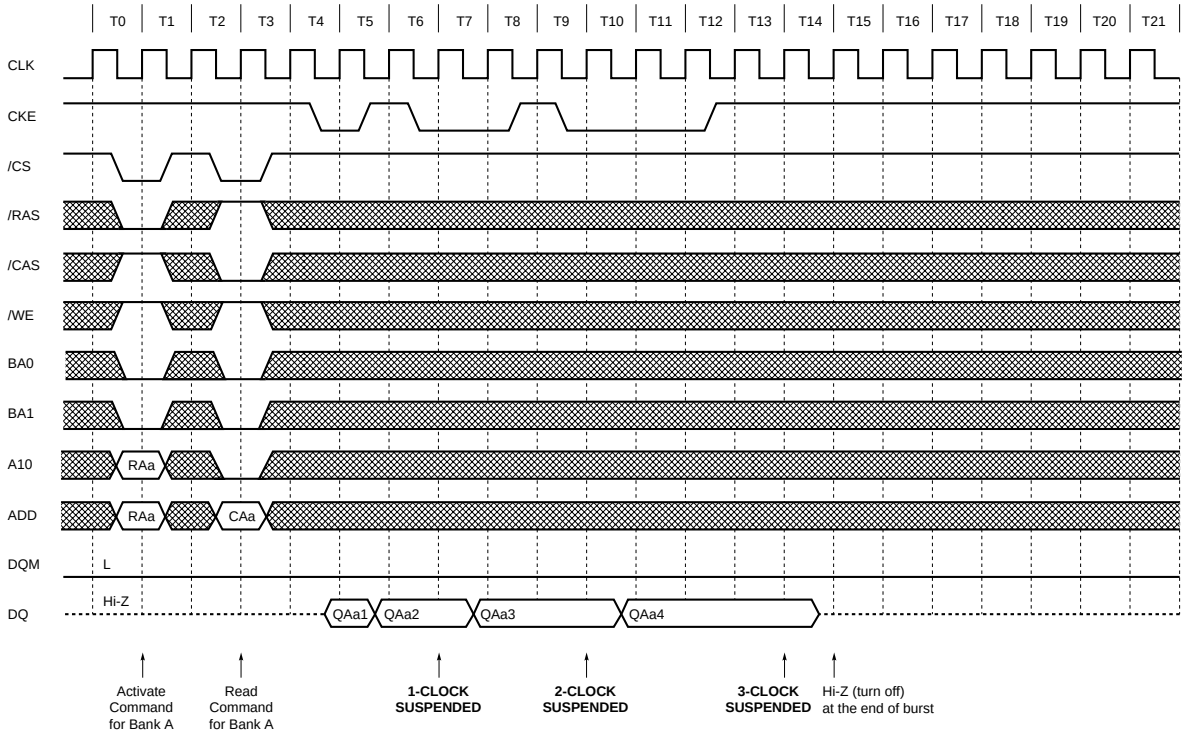


[Burst Length = 4, /CAS Latency = 3]

Clock Suspension during Burst Read

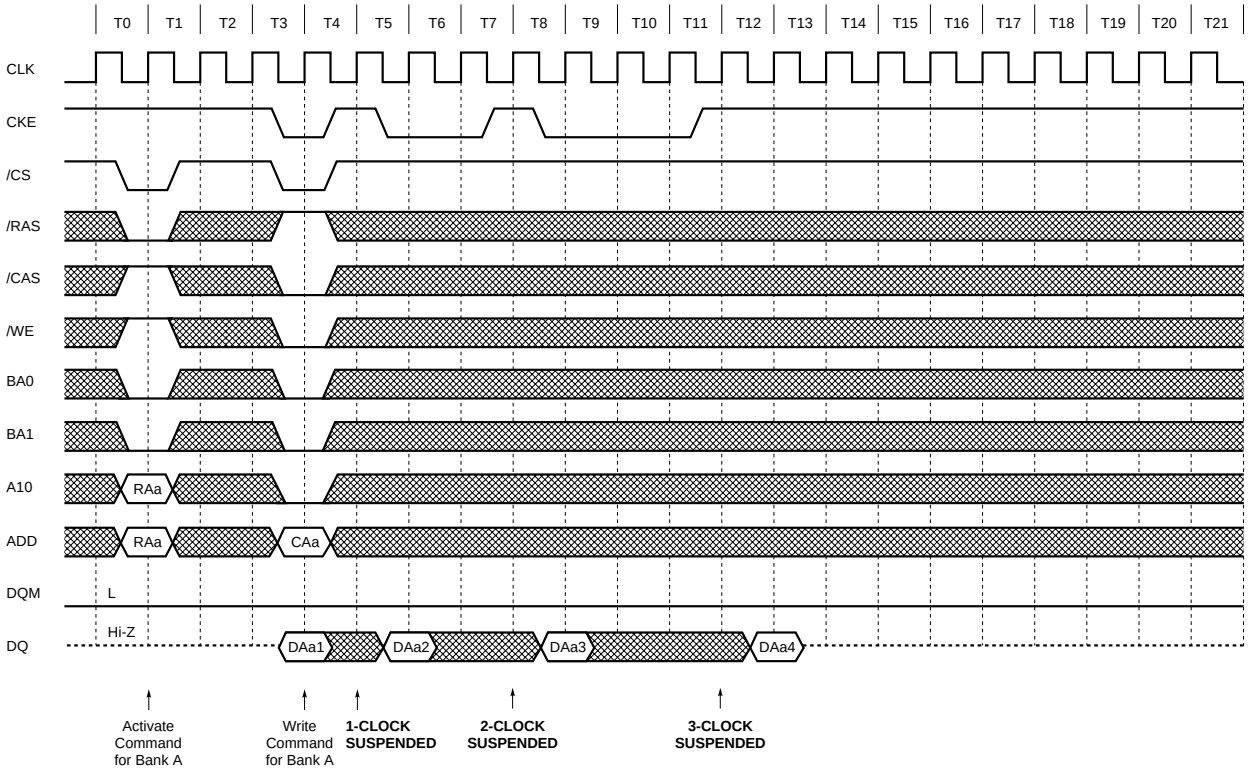


[Burst Length = 4, /CAS Latency = 3]

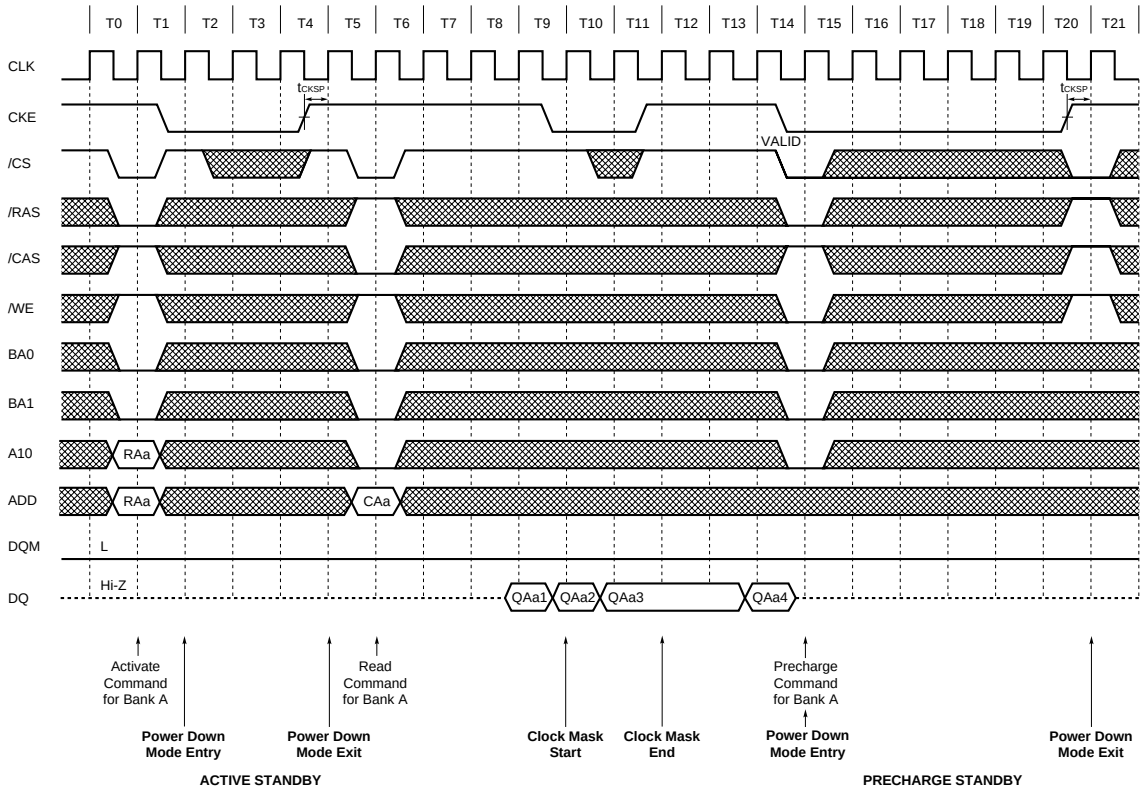


[Burst Length = 4, /CAS Latency = 2]

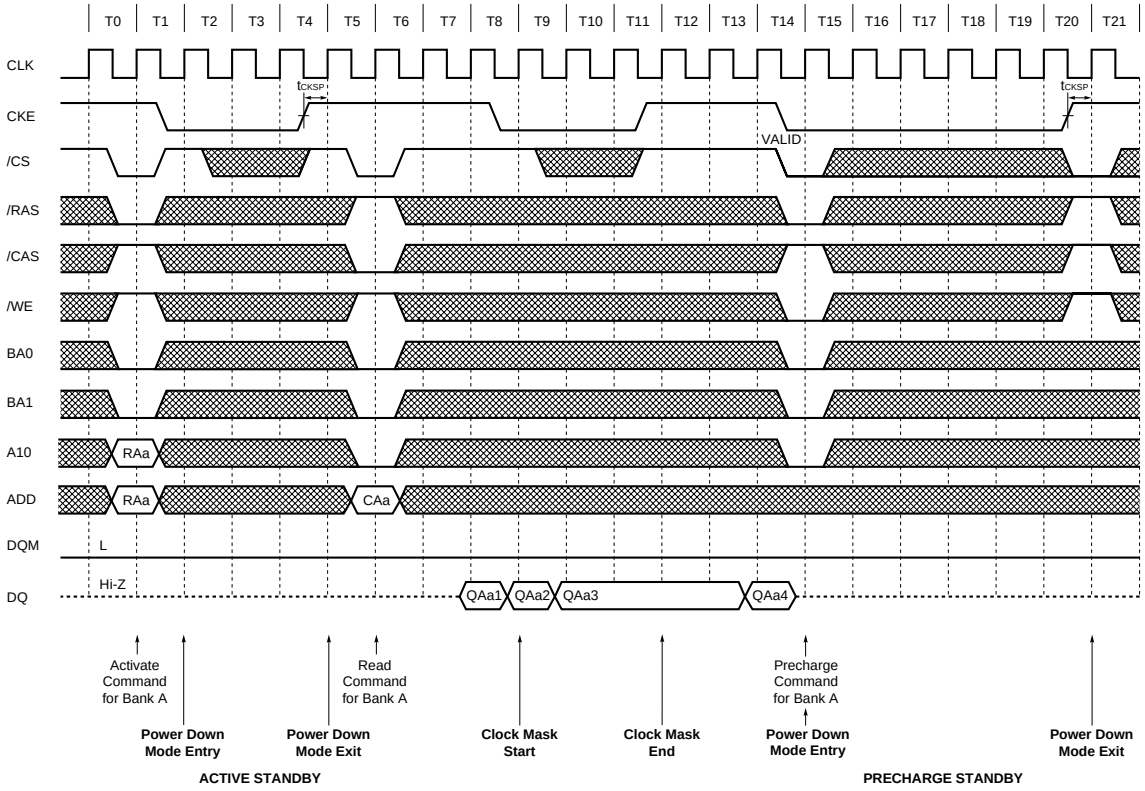
Clock Suspension during Burst Write



Power Down Mode and Clock Mask

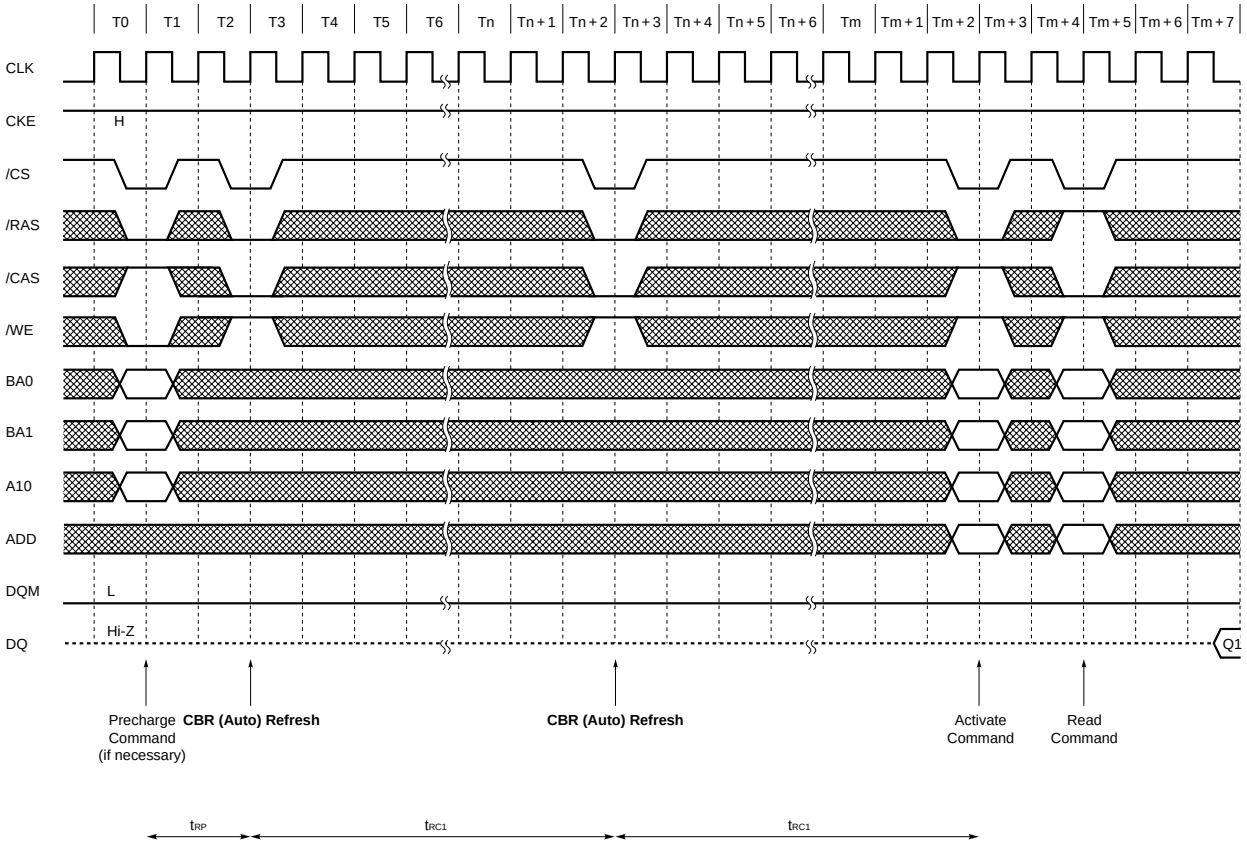


[Burst Length = 4, /CAS Latency = 3]

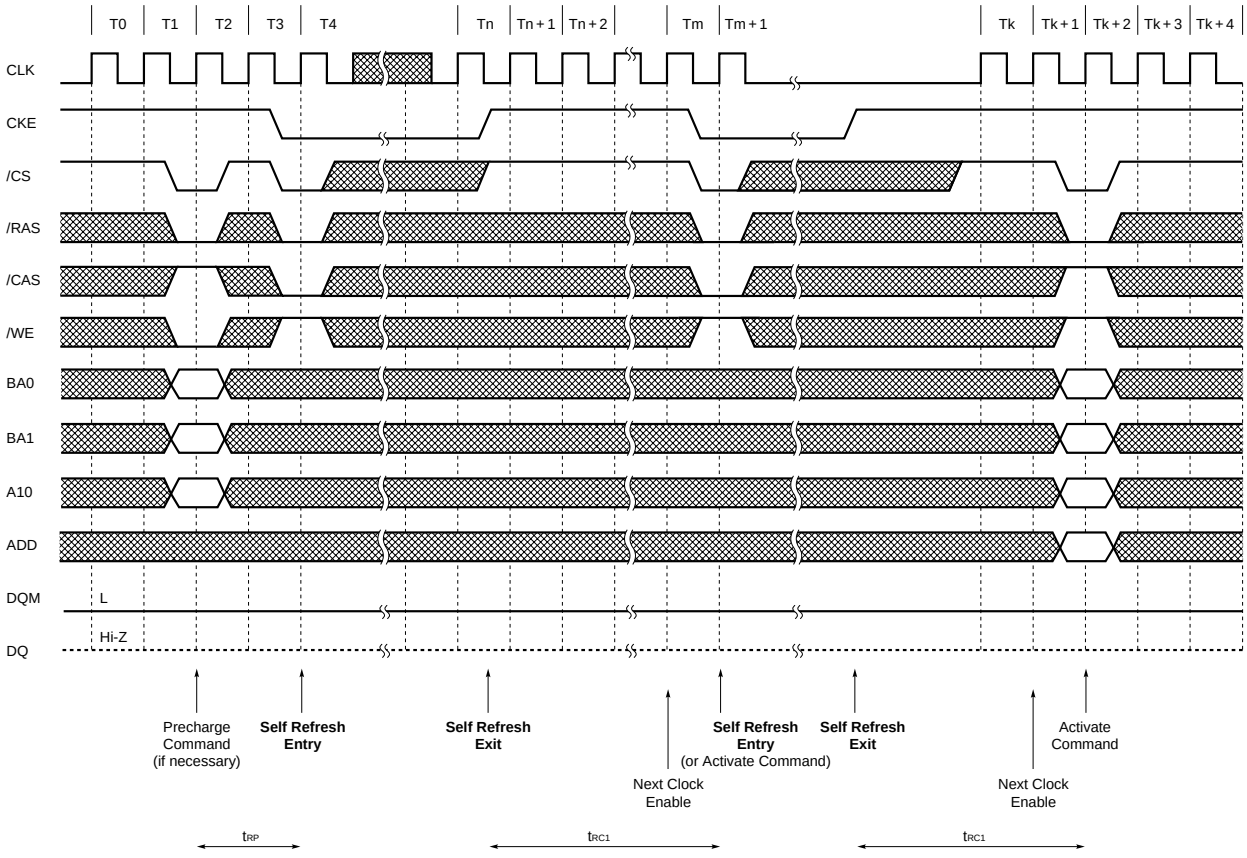


[Burst Length = 4, /CAS Latency = 2]

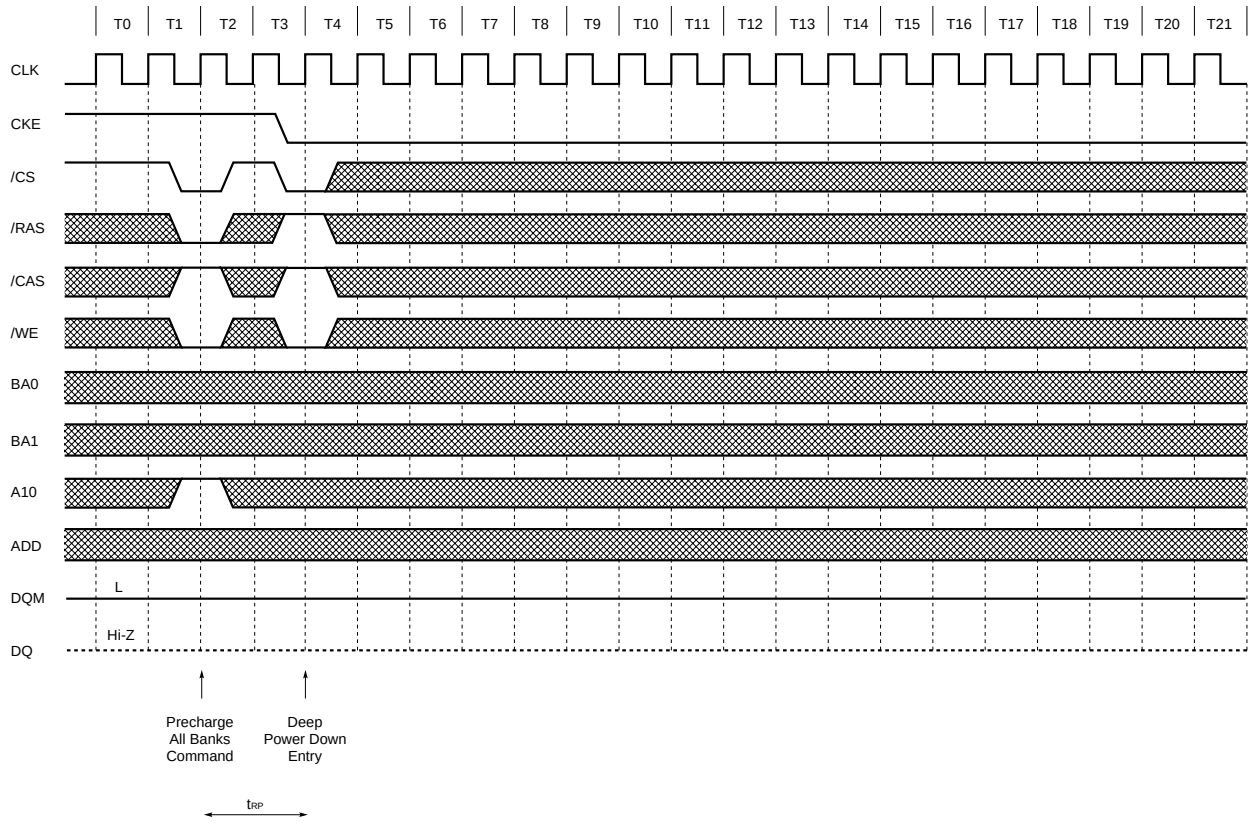
Auto Refresh



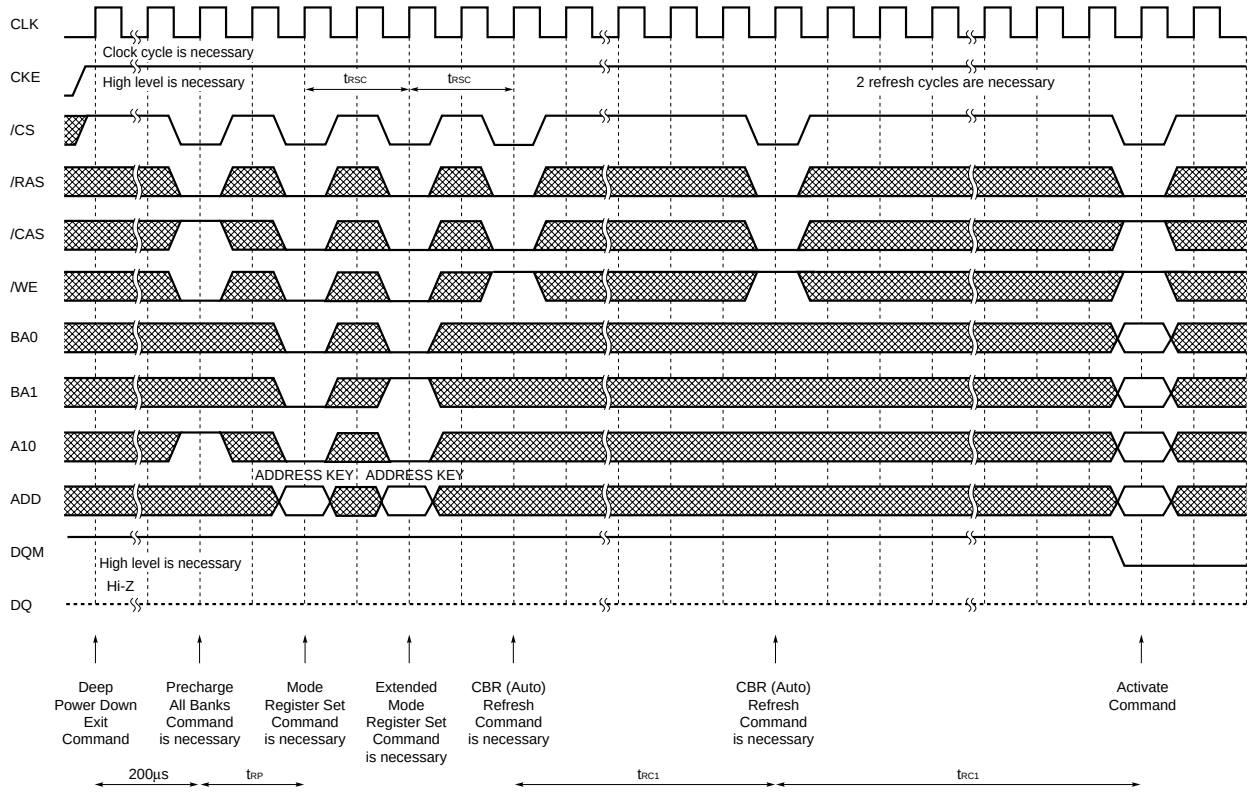
Self Refresh (Entry and Exit)



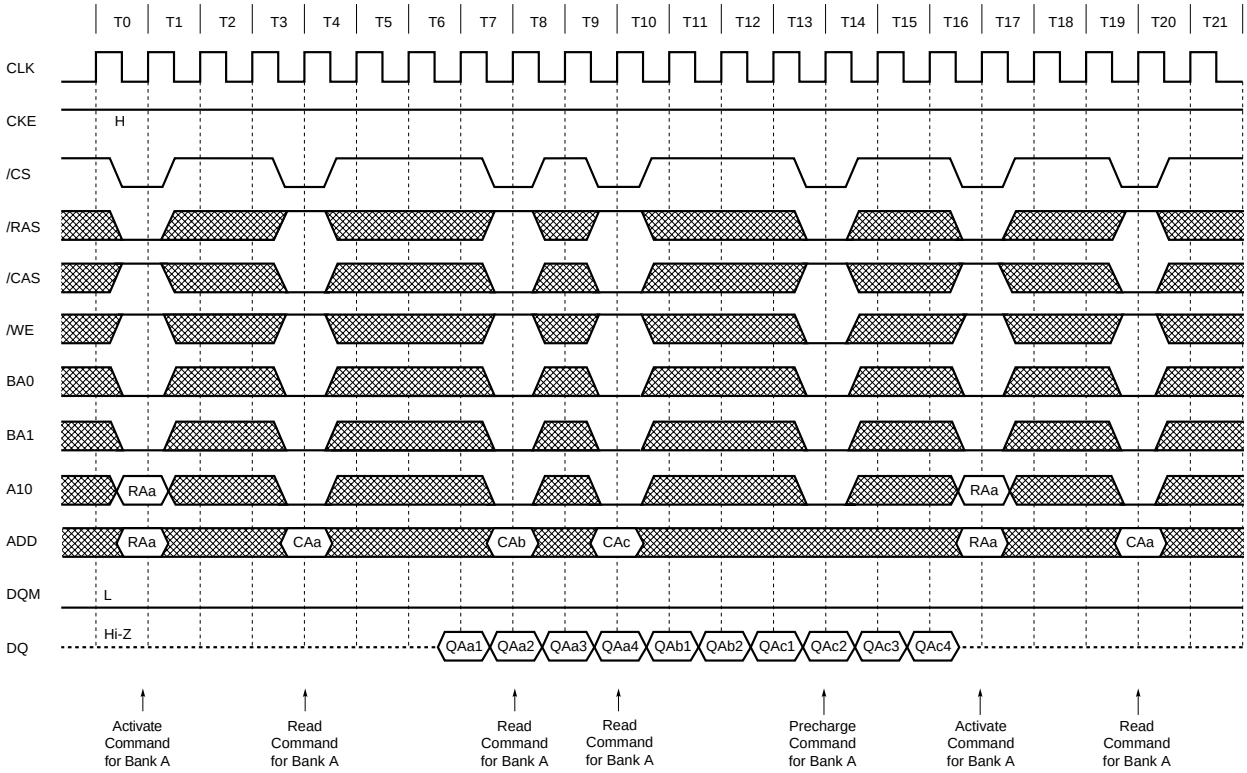
Deep Power Down Entry



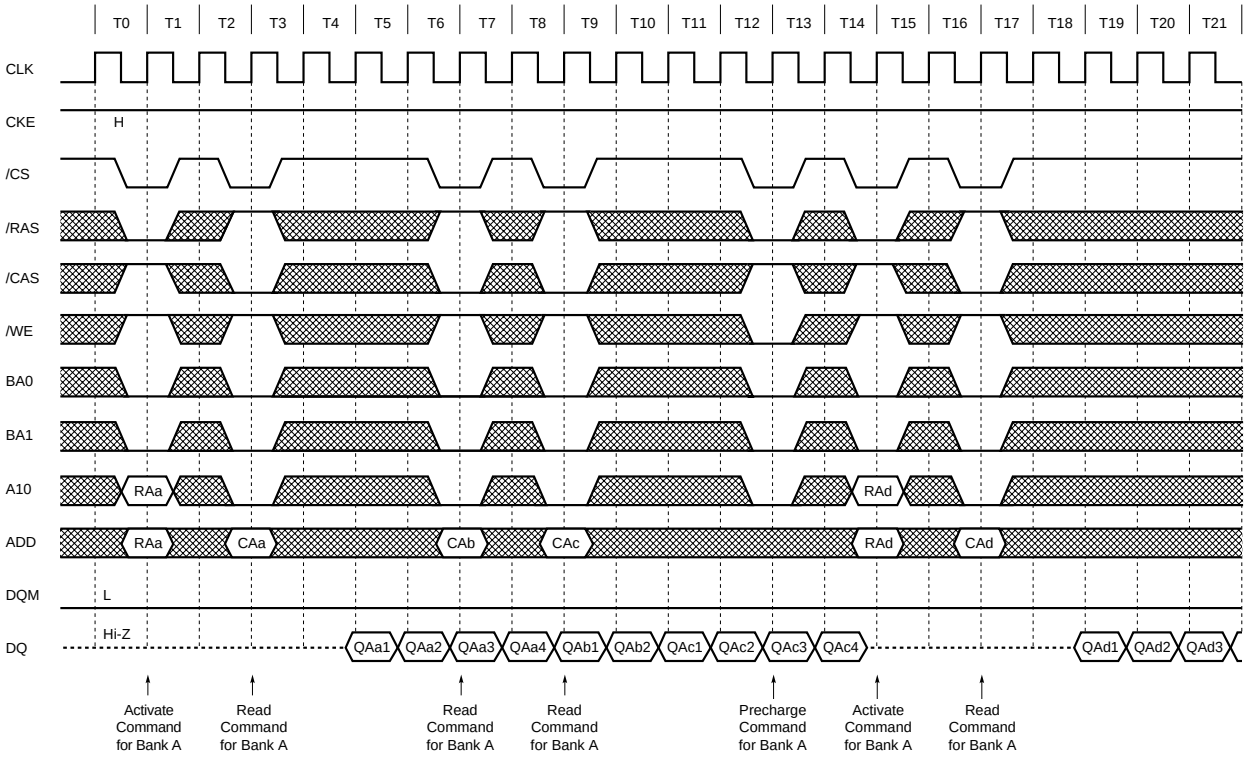
Deep Power Down Exit



Random Column Read

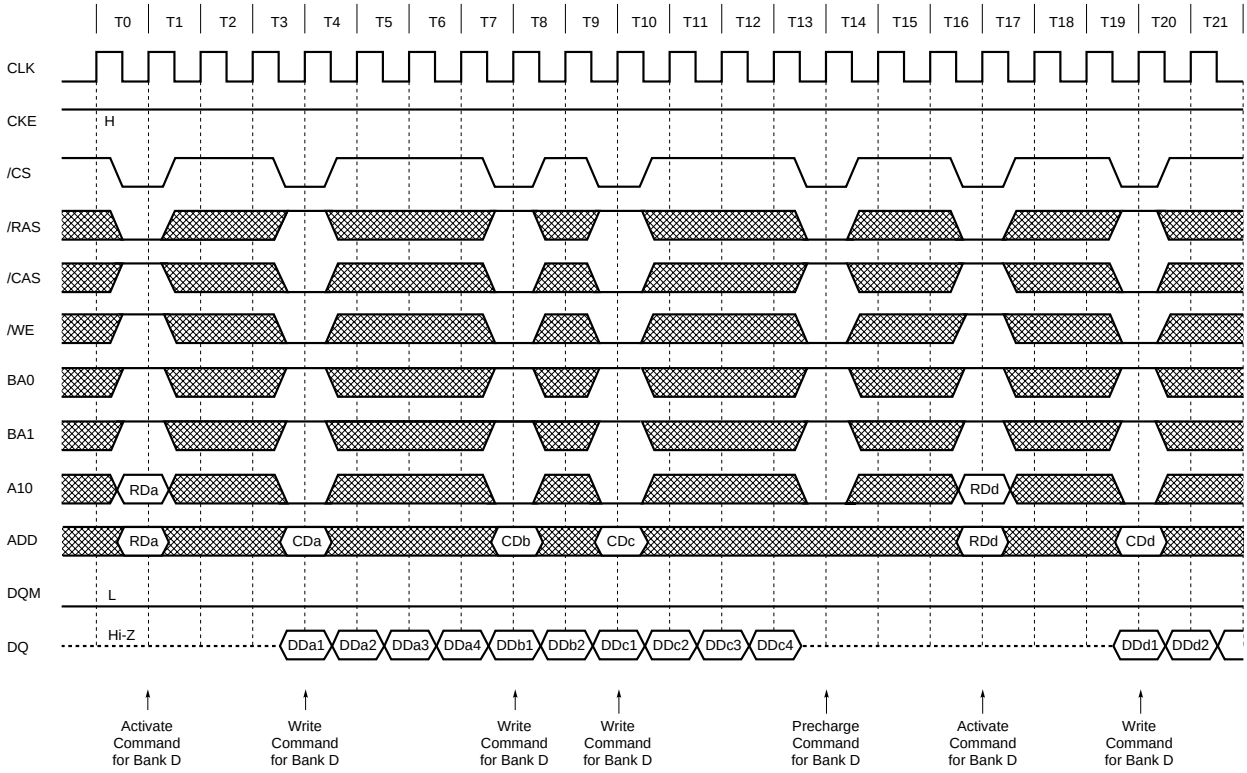


[Burst Length = 4, /CAS Latency = 3]



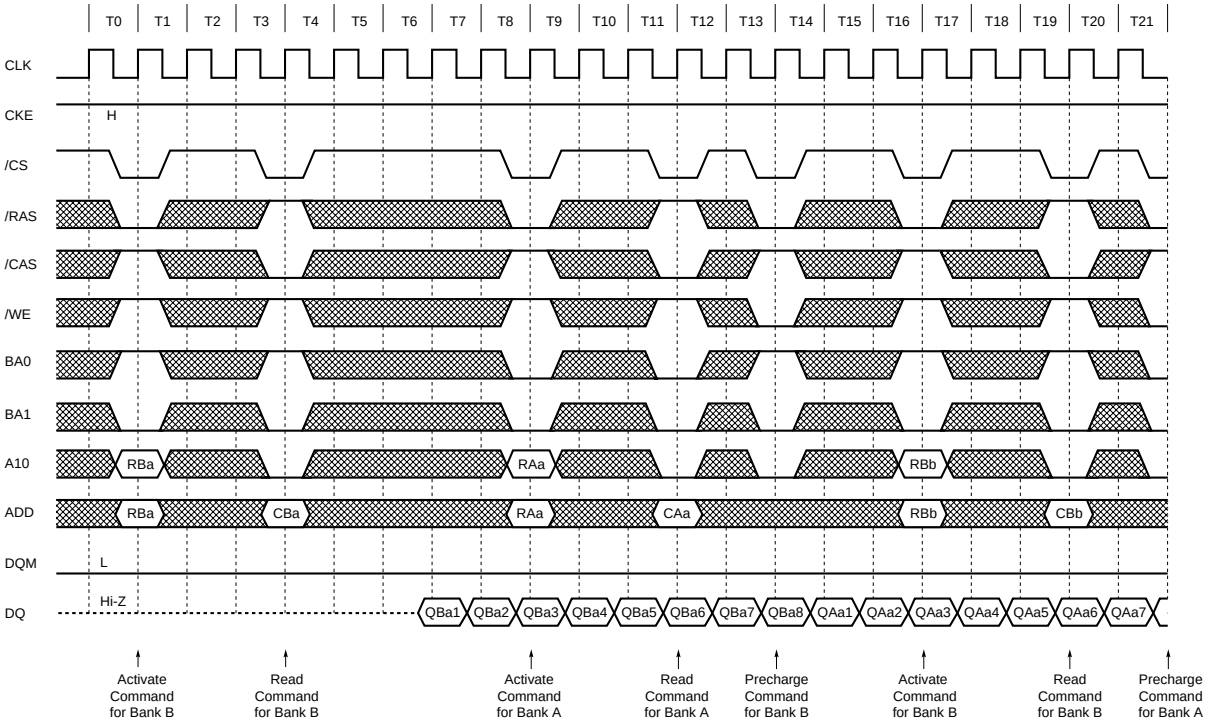
[Burst Length = 4, /CAS Latency = 2]

Random Column Write

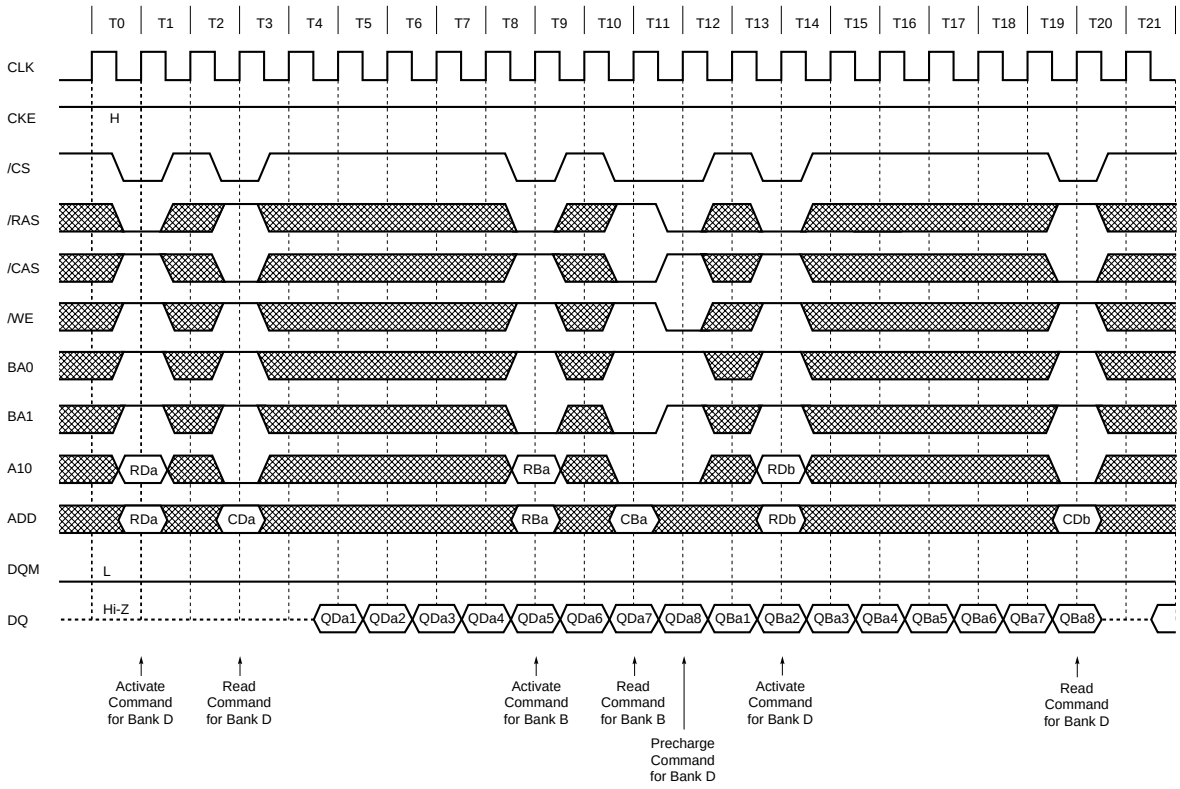


[Burst Length = 4]

Random Row Read

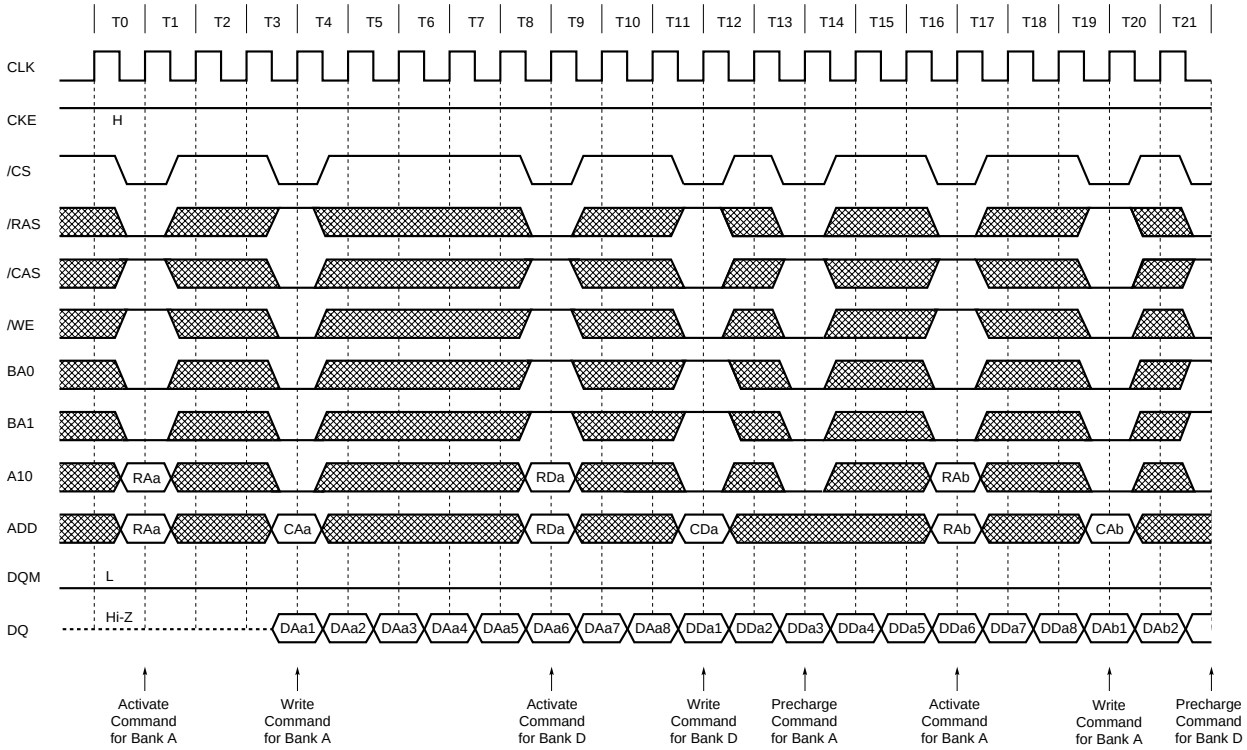


[Burst Length = 8, /CAS Latency = 3]



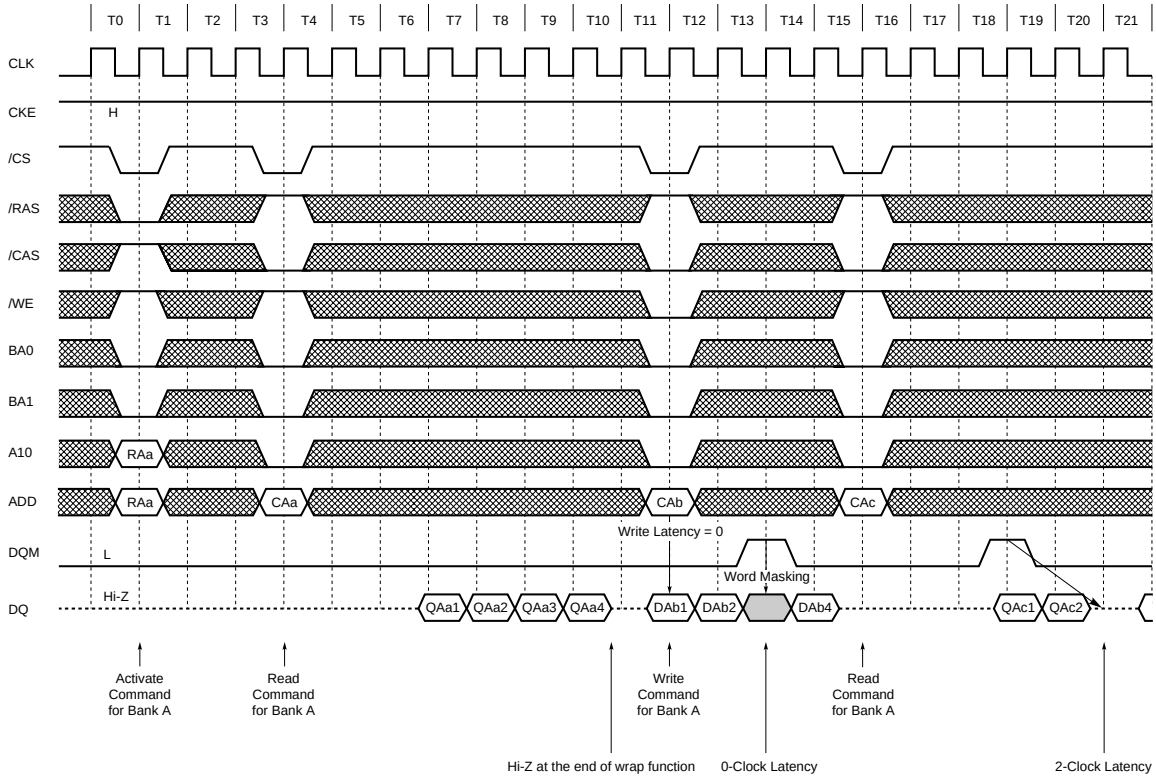
[Burst Length = 8, /CAS Latency = 2]

Random Row Write

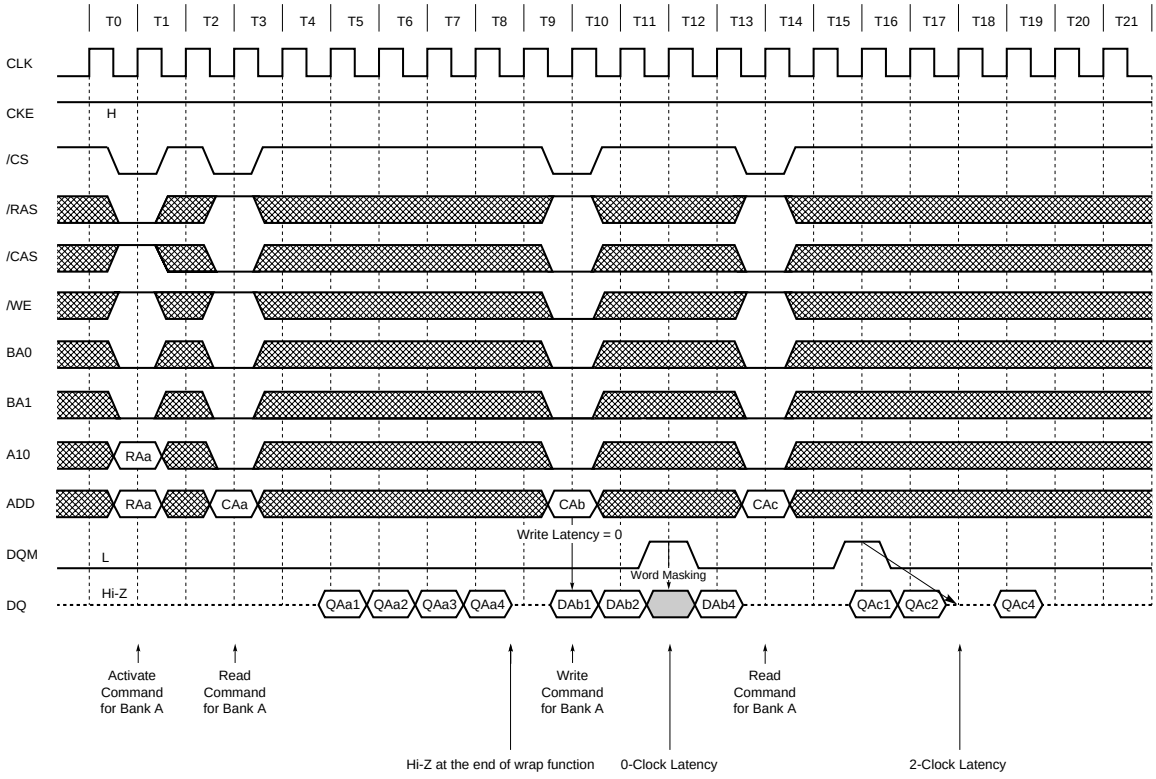


[Burst Length = 8]

Read and Write

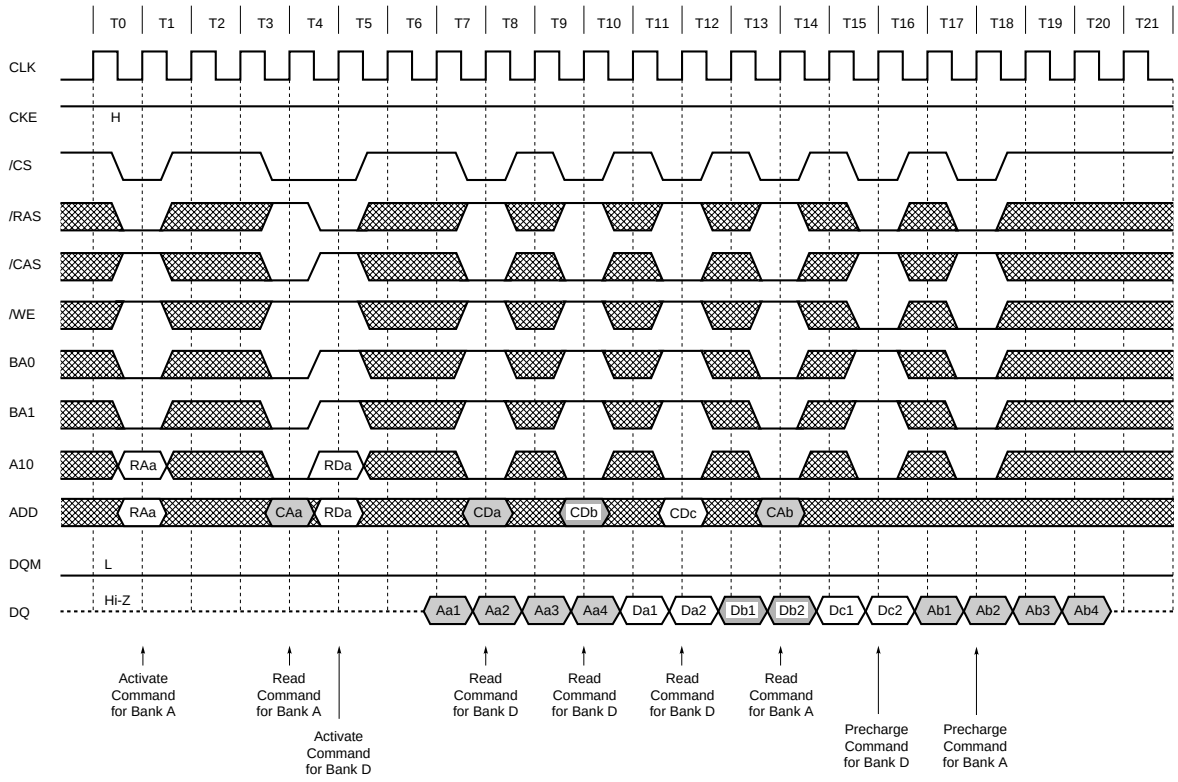


[Burst Length = 4, /CAS Latency = 3]

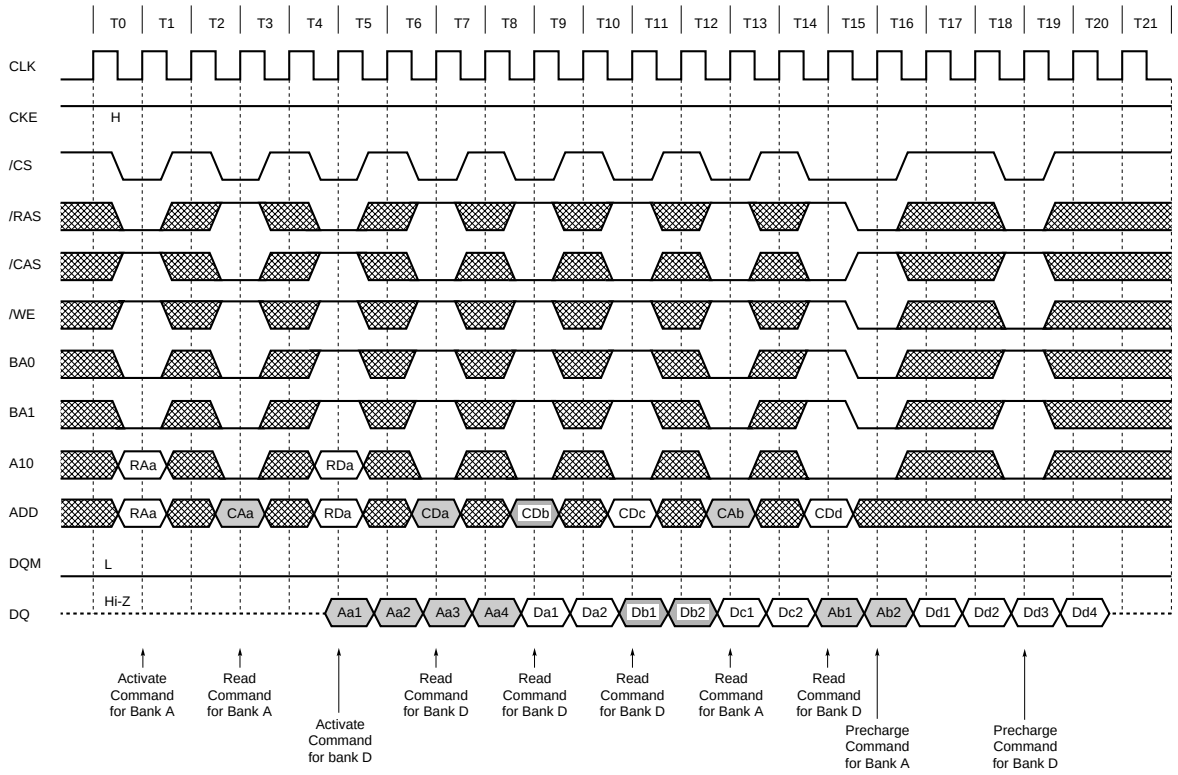


[Burst Length = 4, /CAS Latency = 2]

Interleaved Column Read Cycle

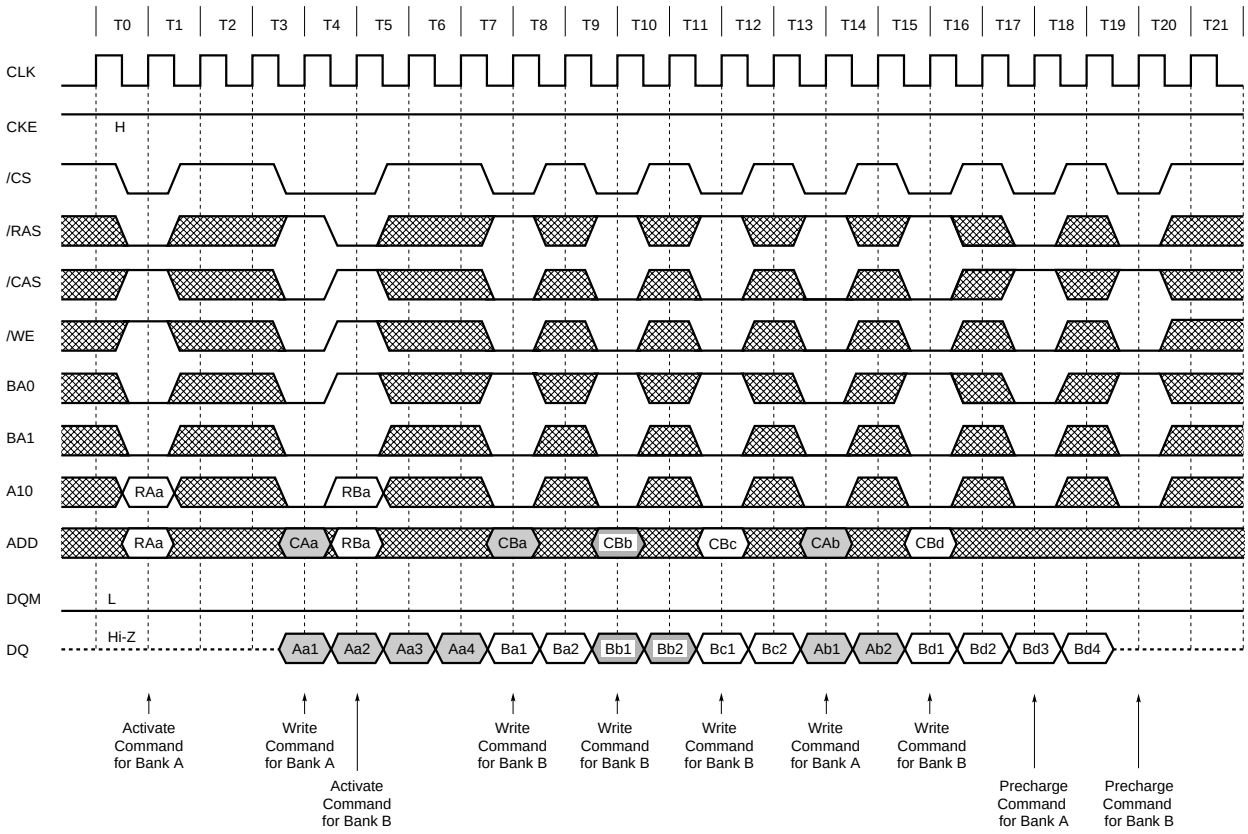


[Burst Length = 4, /CAS Latency = 3]



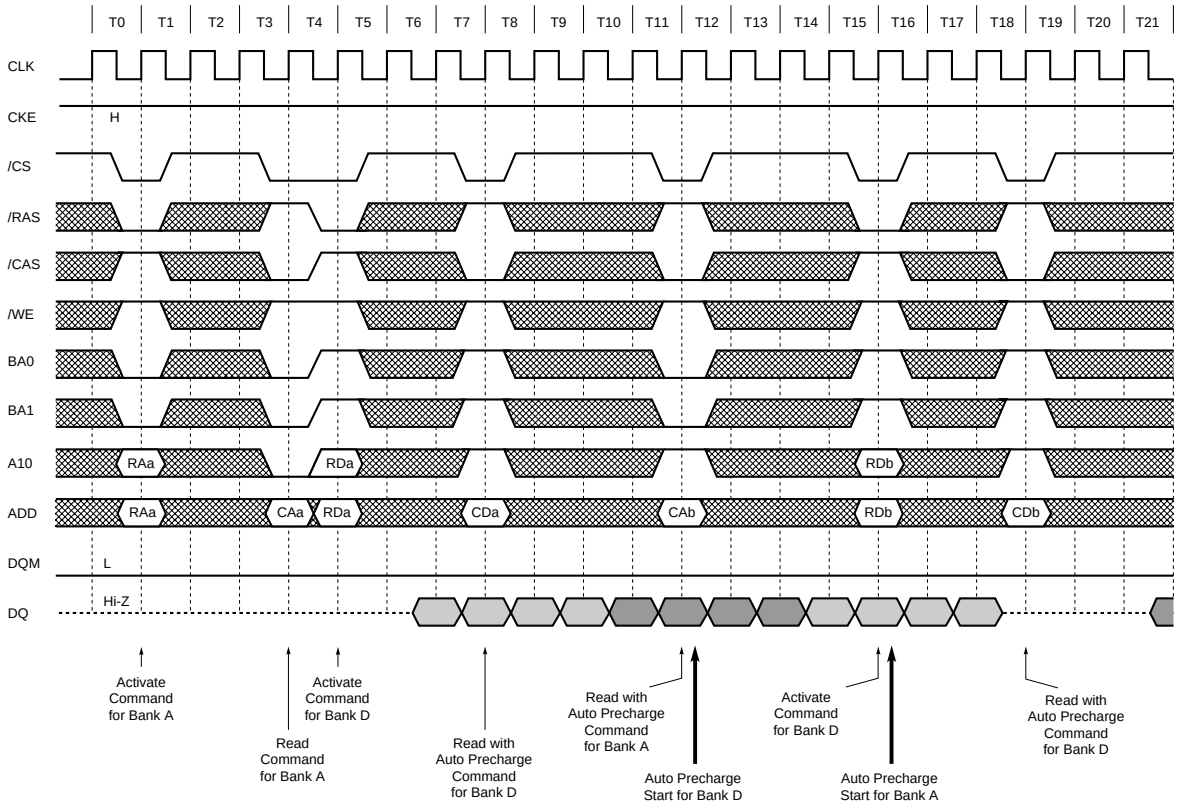
[Burst Length = 4, /CAS Latency = 2]

Interleaved Column Write Cycle

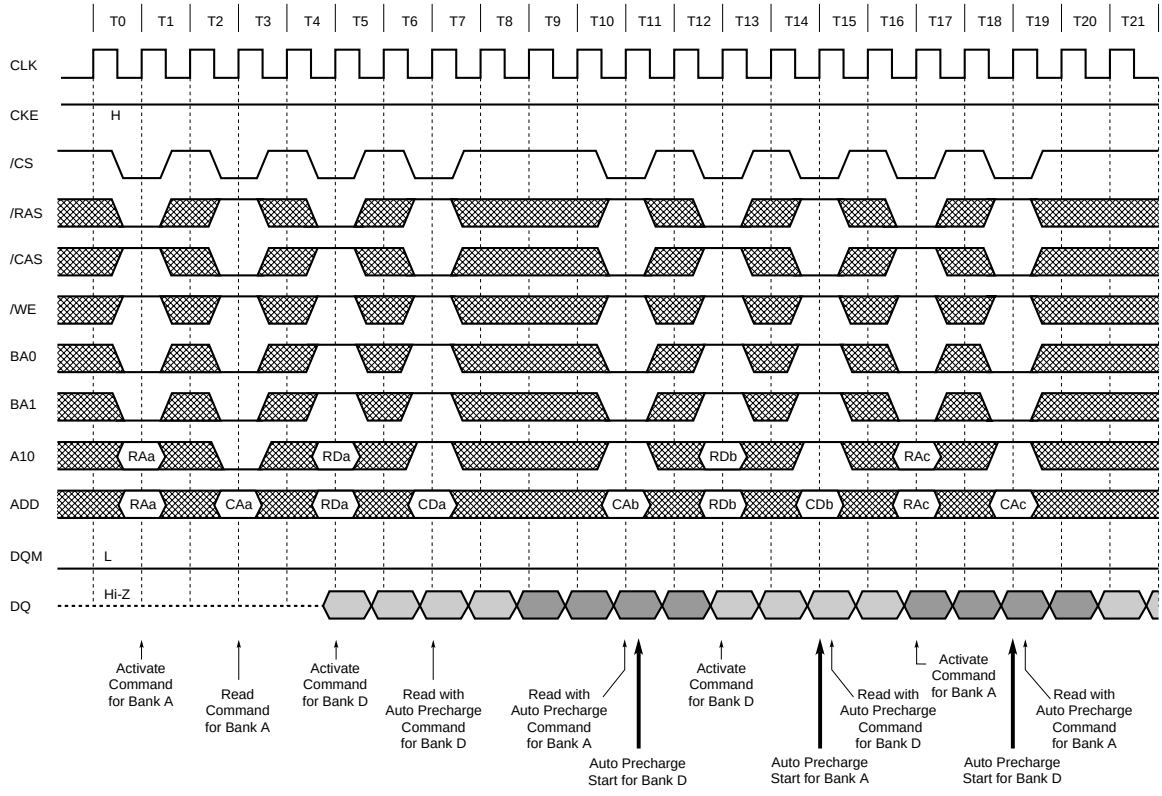


[Burst Length = 4]

Auto Precharge after Read Burst

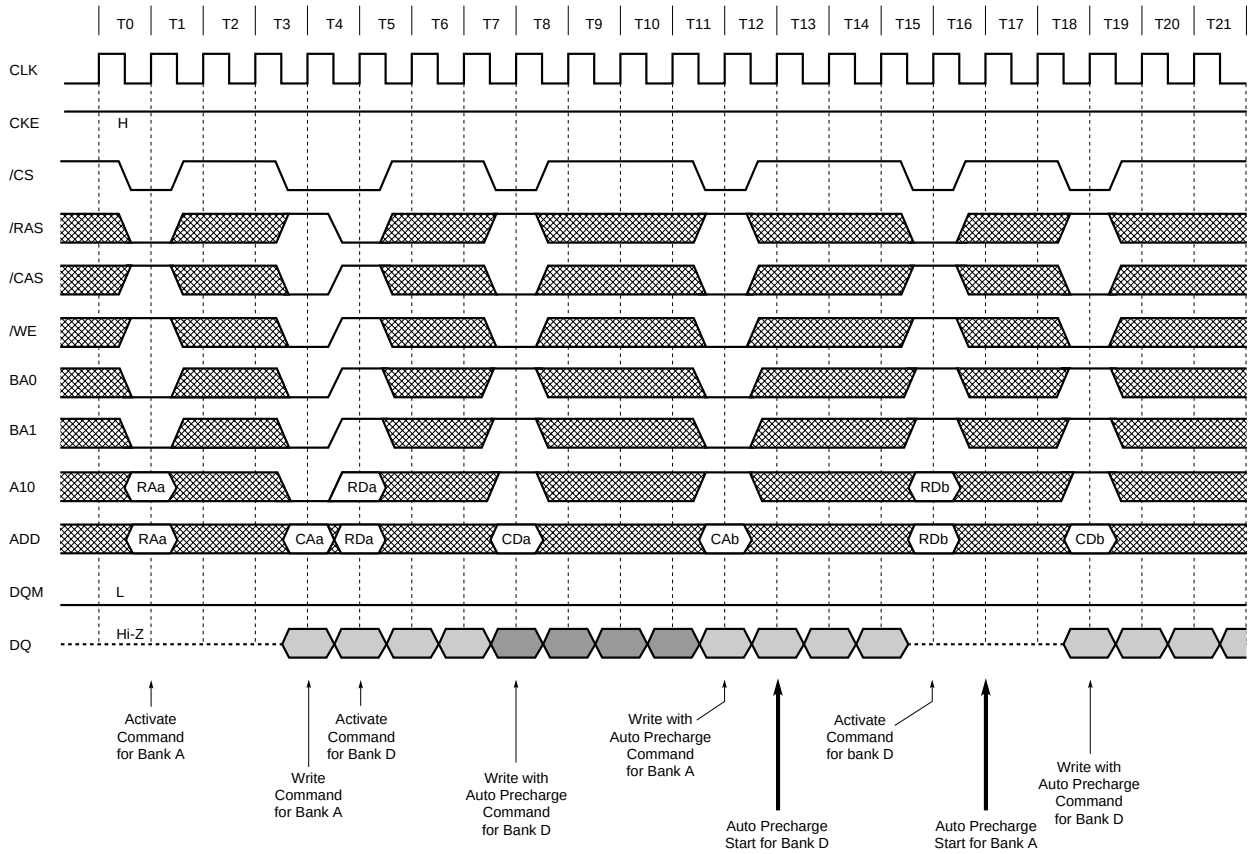


[Burst Length = 4, /CAS Latency = 3]



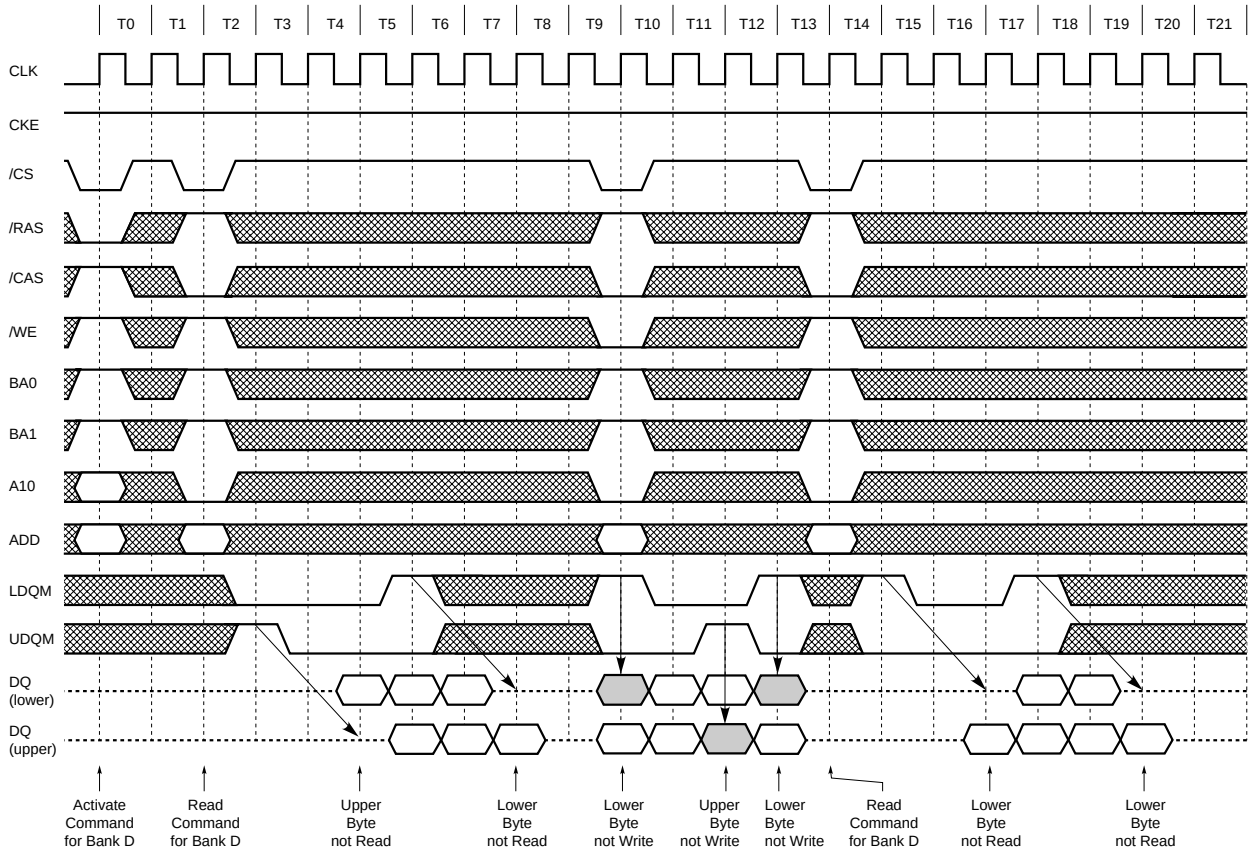
[Burst Length = 4, /CAS Latency = 2]

Auto Precharge after Write Burst



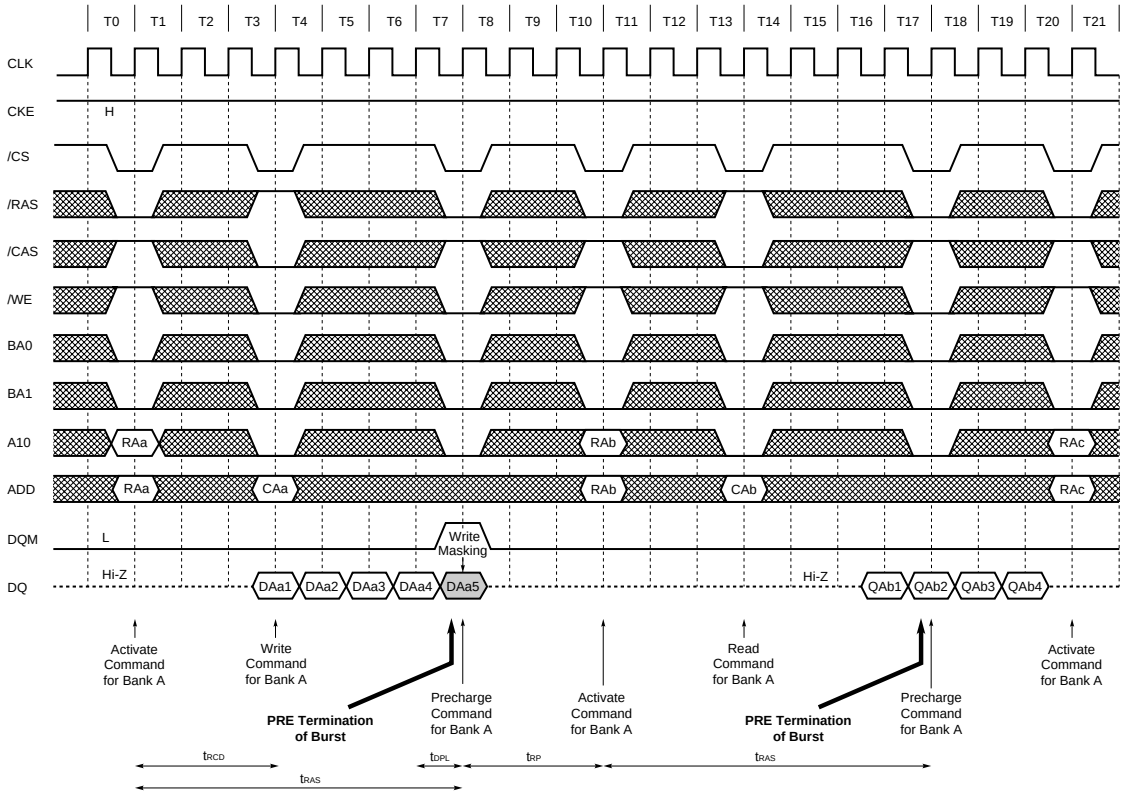
[Burst Length = 4]

Byte Write Operation

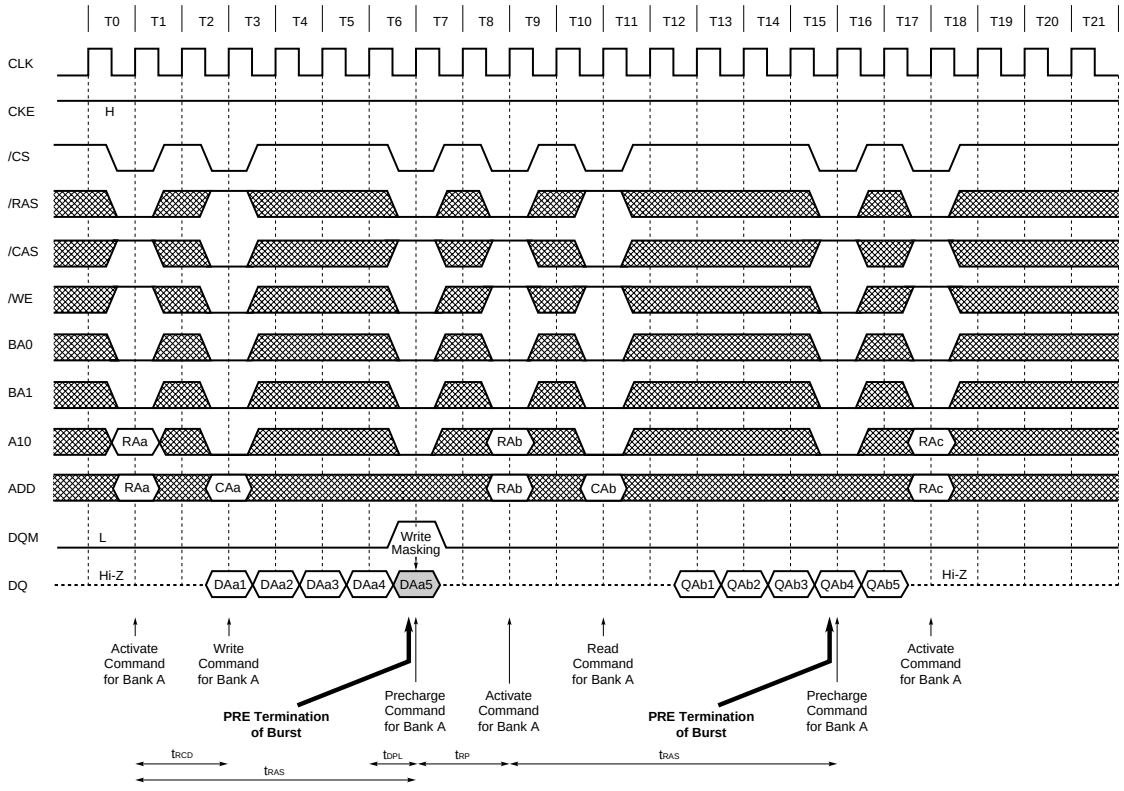


[Burst Length = 4]

Precharge Termination



[Burst Length = 8, /CAS Latency = 3]



[Burst Length = 8, /CAS Latency = 2]

1G Mbits (512 Mbits ×2pcs)
NAND E2PROM

Memory cell 528 ×256K ×8

Register 528 ×8

Page size 528 bytes

Block size (16K + 512) bytes

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(Ta = - 30° to 85°C, V_{CC} = 2.5 V to 3.0 V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
t_{CLS}	CLE Setup Time	0	—	ns	
t_{CLH}	CLE Hold Time	10	—	ns	
t_{CS}	$\overline{CE}$ Setup Time	0	—	ns	
t_{CH}	$\overline{CE}$ Hold Time	10	—	ns	
t_{WP}	Write Pulse Width	25	—	ns	
t_{ALS}	ALE Setup Time	0	—	ns	
t_{ALH}	ALE Hold Time	10	—	ns	
t_{DS}	Data Setup Time	20	—	ns	
t_{DH}	Data Hold Time	10	—	ns	
t_{WC}	Write Cycle Time	50	—	ns	
t_{WH}	$\overline{WE}$ High Hold Time	15	—	ns	
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Low	100	—	ns	
t_{RR}	Ready to $\overline{RE}$ Falling Edge	20	—	ns	
t_{RP}	Read Pulse Width	35	—	ns	
t_{RC}	Read Cycle Time	50	—	ns	
t_{REA}	$\overline{RE}$ Access Time (Serial Data Access)	—	35	ns	
t_{CEA}	$\overline{CE}$ Access Time (Serial Data Access, ID Read)	—	45	ns	
t_{ALEA}	ALE Access Time (ID Read)	—	45	ns	
t_{REAID}	$\overline{RE}$ Access Time (ID Read)	—	35	ns	
t_{OH}	Data Output Hold Time	10	—	ns	
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	—	30	ns	
t_{CHZ}	$\overline{CE}$ High to Output High Impedance	—	20	ns	
t_{REH}	$\overline{RE}$ High Hold Time	15	—	ns	
t_{IR}	Output-High-impedance-to- $\overline{RE}$ Falling Edge	0	—	ns	
t_{RSTO}	$\overline{RE}$ Access Time (Status Read)	—	35	ns	
t_{CSTO}	$\overline{CE}$ Access Time (Status Read)	—	45	ns	
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low	30	—	ns	
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low	30	—	ns	
t_R	Memory Cell Array to Starting Address	—	35	µs	
t_{WB}	$\overline{WE}$ High to Busy	—	200	ns	
t_{AR2}	ALE Low to $\overline{RE}$ Low (Read Cycle)	50	—	ns	
t_{RST}	Device Reset Time (Read/Program/Erase)	—	6/15/500	µs	

AC TEST CONDITIONS

PARAMETER	CONDITION
Input level	2.4 V, 0.4 V
Input pulse rise and fall time	3 ns
Input comparison level	1.5 V, 1.5 V
Output data comparison level	1.5 V, 1.5 V
Output load	C_L (100 pF) + 1 TTL

VALID BLOCKS (1)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N_{VB}	Number of Valid Blocks	8032	—	8192	Blocks

(1) The device occasionally contains unusable blocks. Refer to Application Note (14) toward the end of this document.

(2) The first block (block address #00) is guaranteed to be a valid block at the time of shipment.

PROGRAMMING AND ERASING CHARACTERISTICS

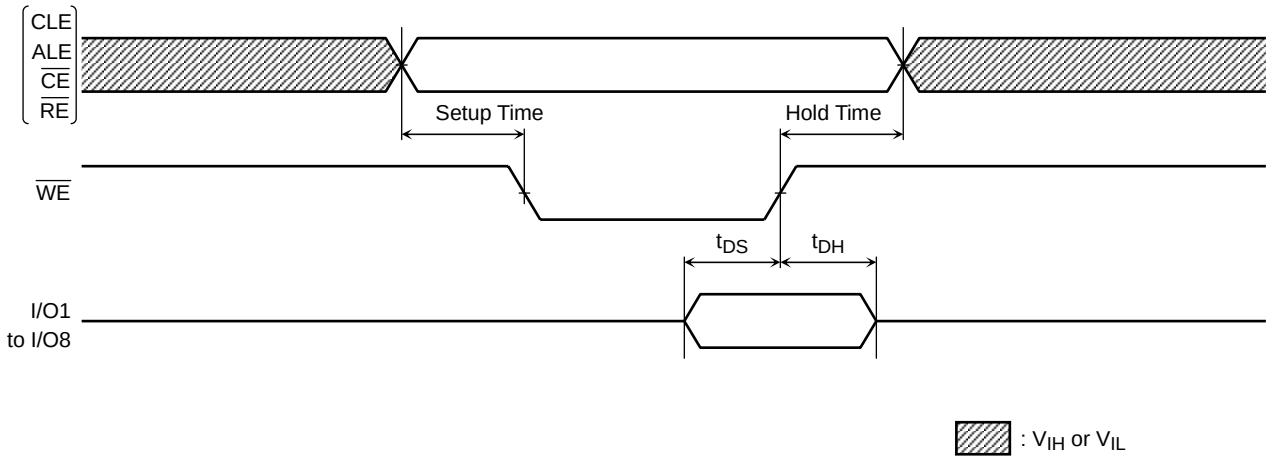
(Ta = - 30° to 85°C, V_{CC} = 2.5 V to 3.0 V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t_{PROG}	Programming Time	—	450	1000	µs	
t_{DBSY}	Dummy Busy Time for Multi Block Programming	—	3.5	10	µs	
t_{MBPBSY}	Multi Block Program Busy Time	—	450	1000	µs	
N	Number of Programming Cycles on Same Page	—	—	3		(1)
t_{BERASE}	Block Erasing Time	—	2	10	ms	

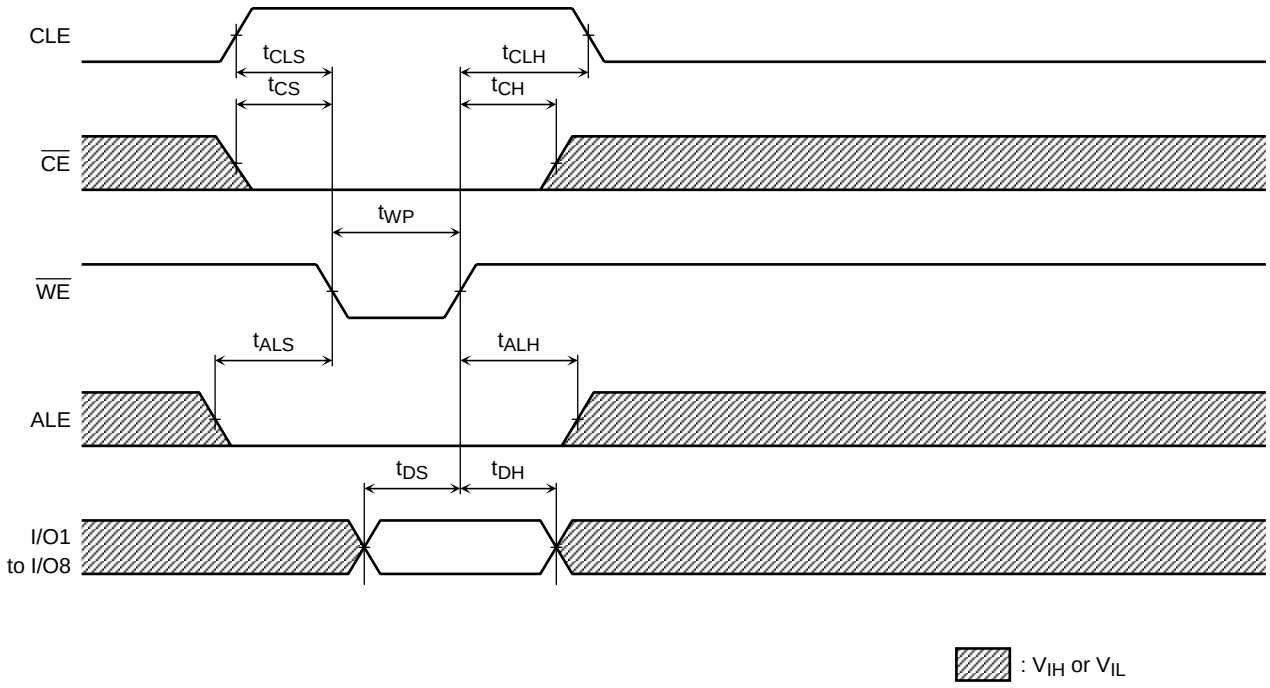
(1): Refer to Application Note (12) toward the end of this document.

TIMING DIAGRAMS

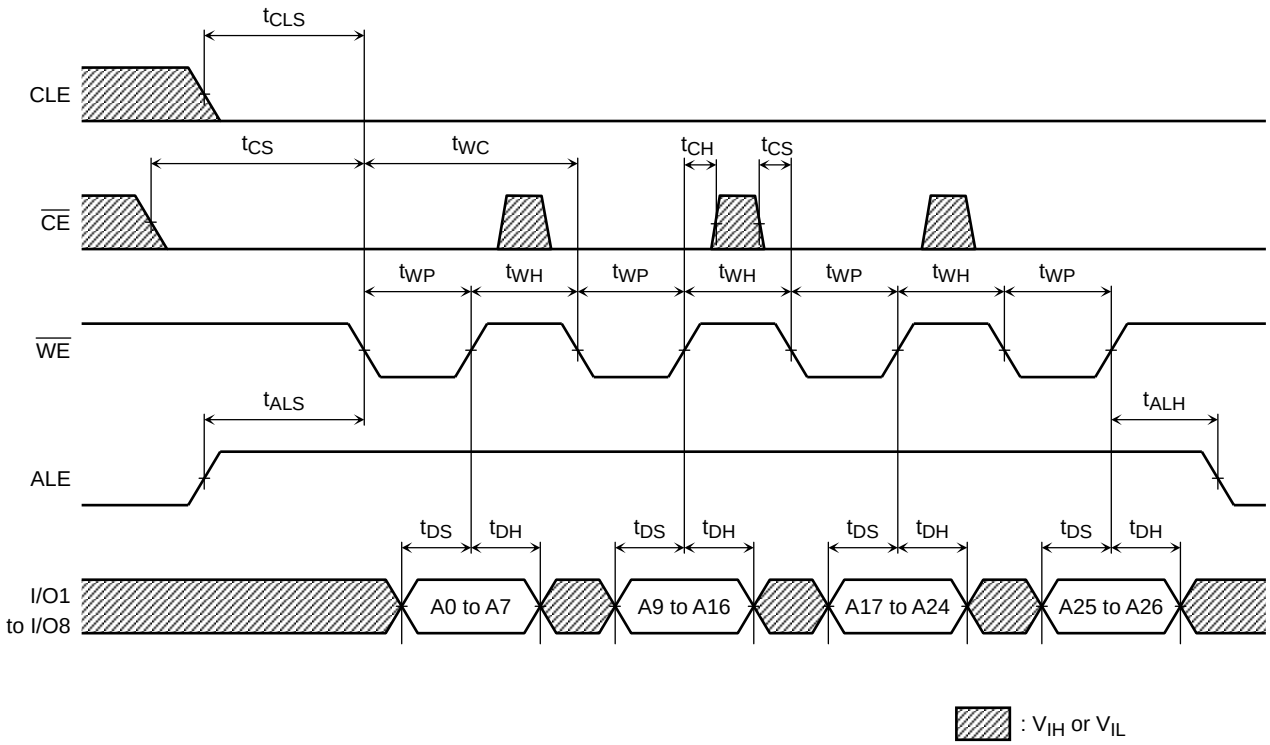
Latch Timing Diagram for Command/Address/Data



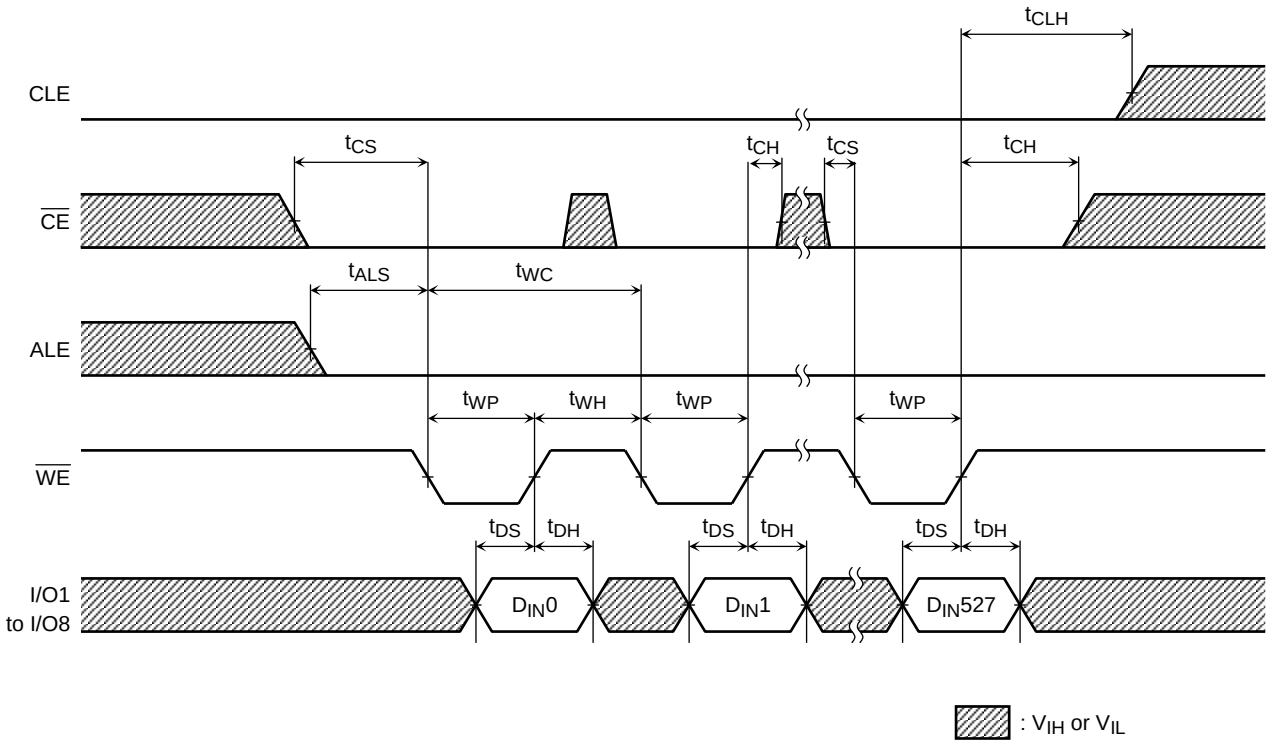
Command Input Cycle Timing Diagram



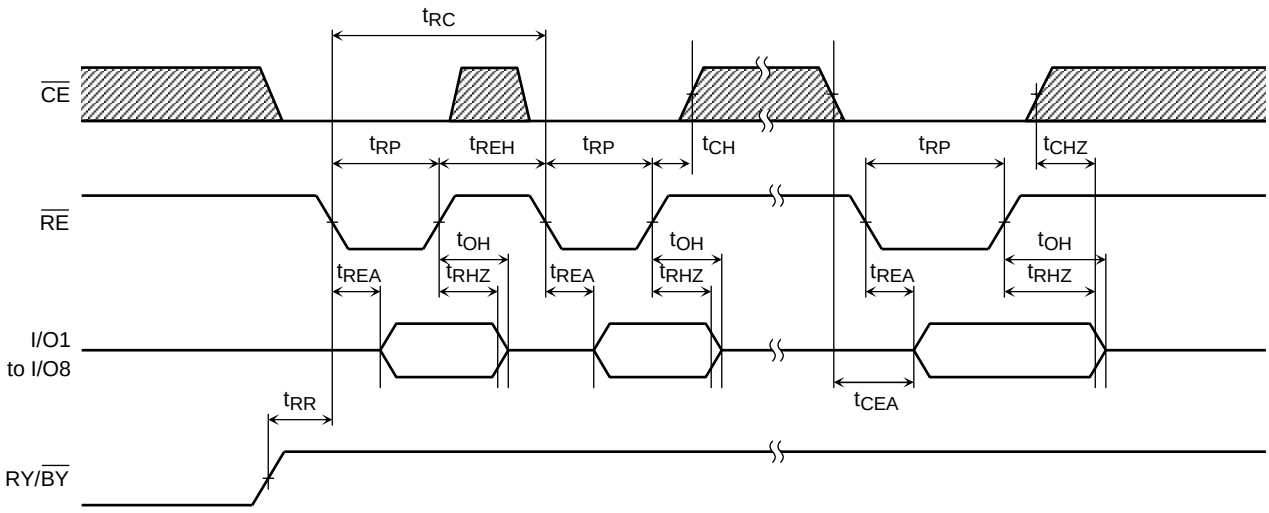
Address Input Cycle Timing Diagram



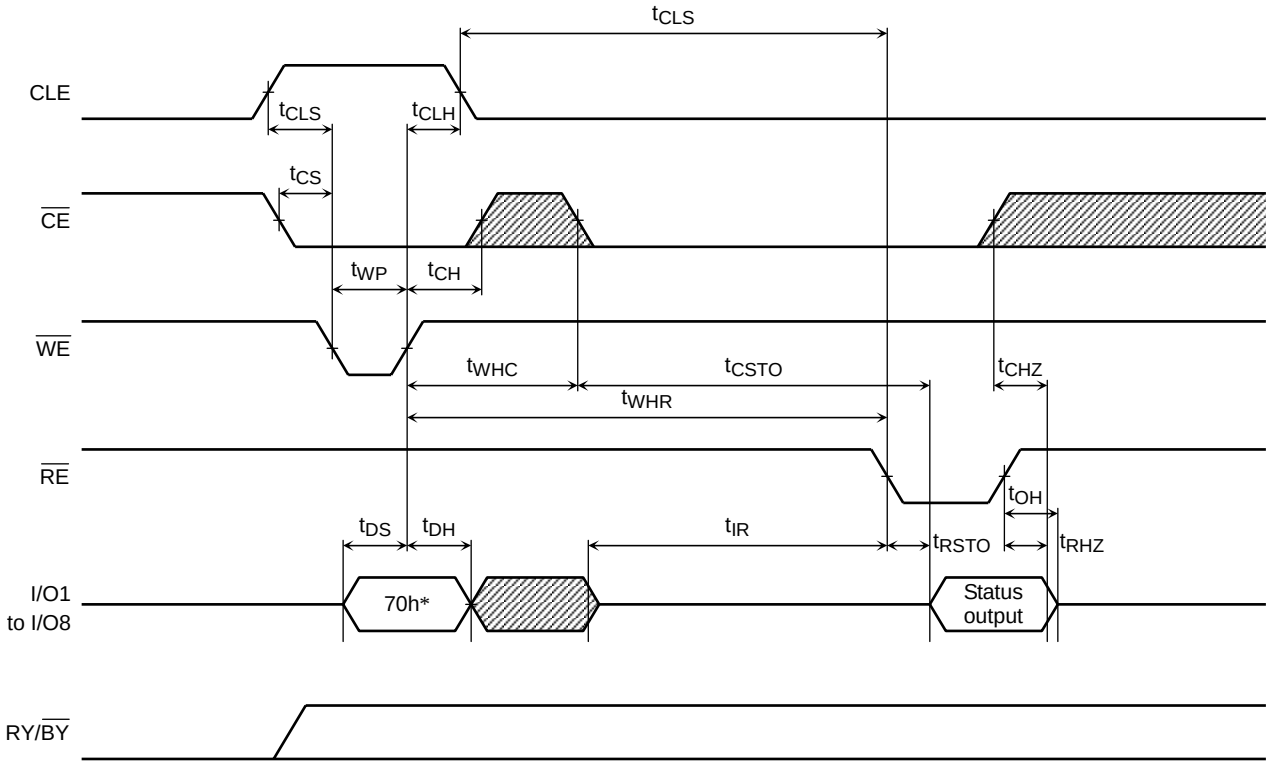
Data Input Cycle Timing Diagram



Serial Read Cycle Timing Diagram



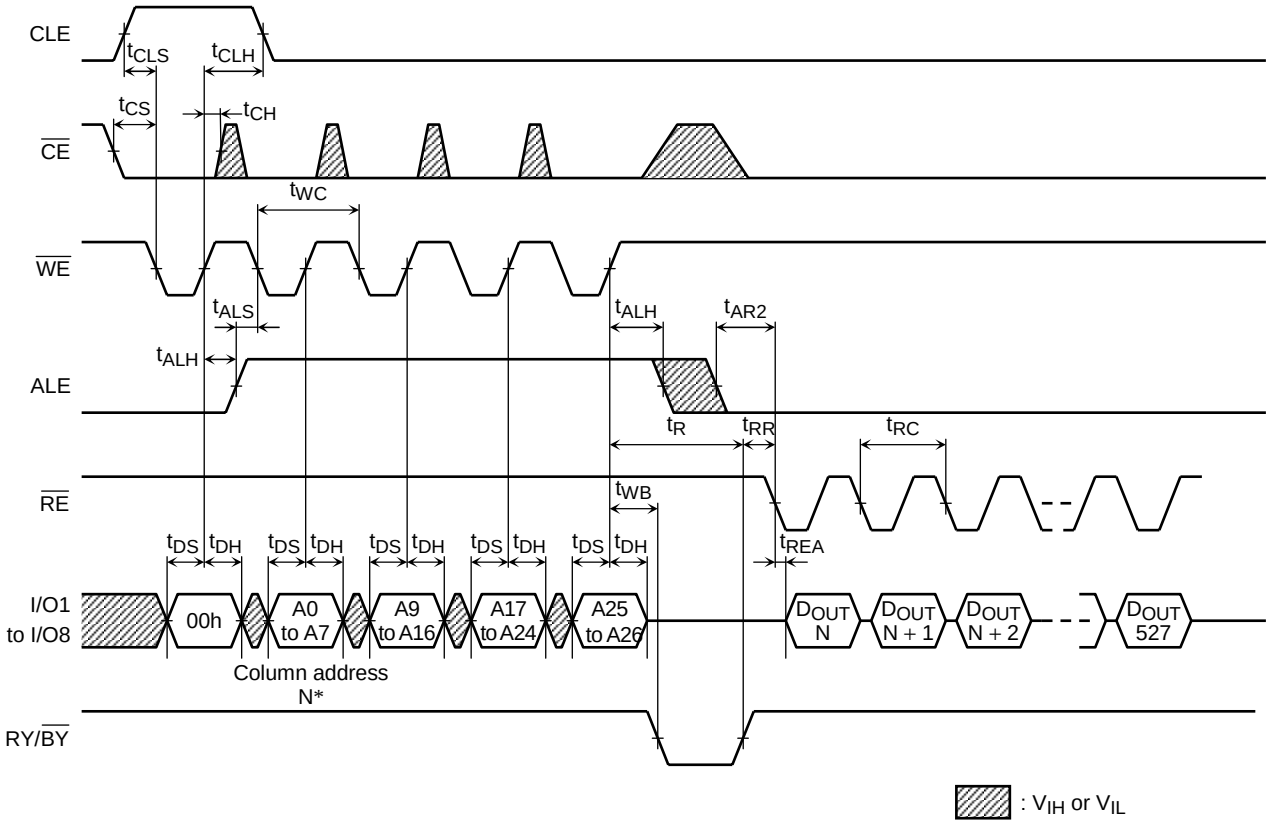
Status Read Cycle Timing Diagram



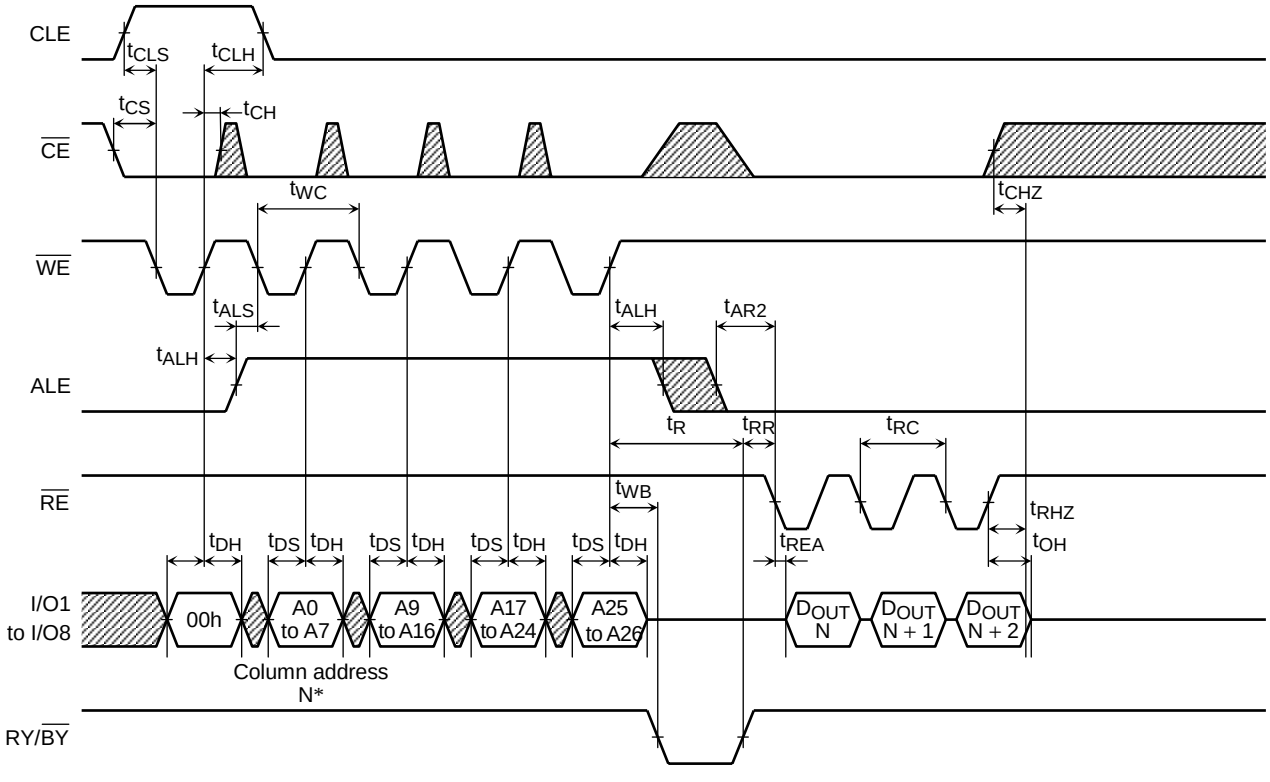
* 70h represents the hexadecimal number

: V_{IH} or V_{IL}

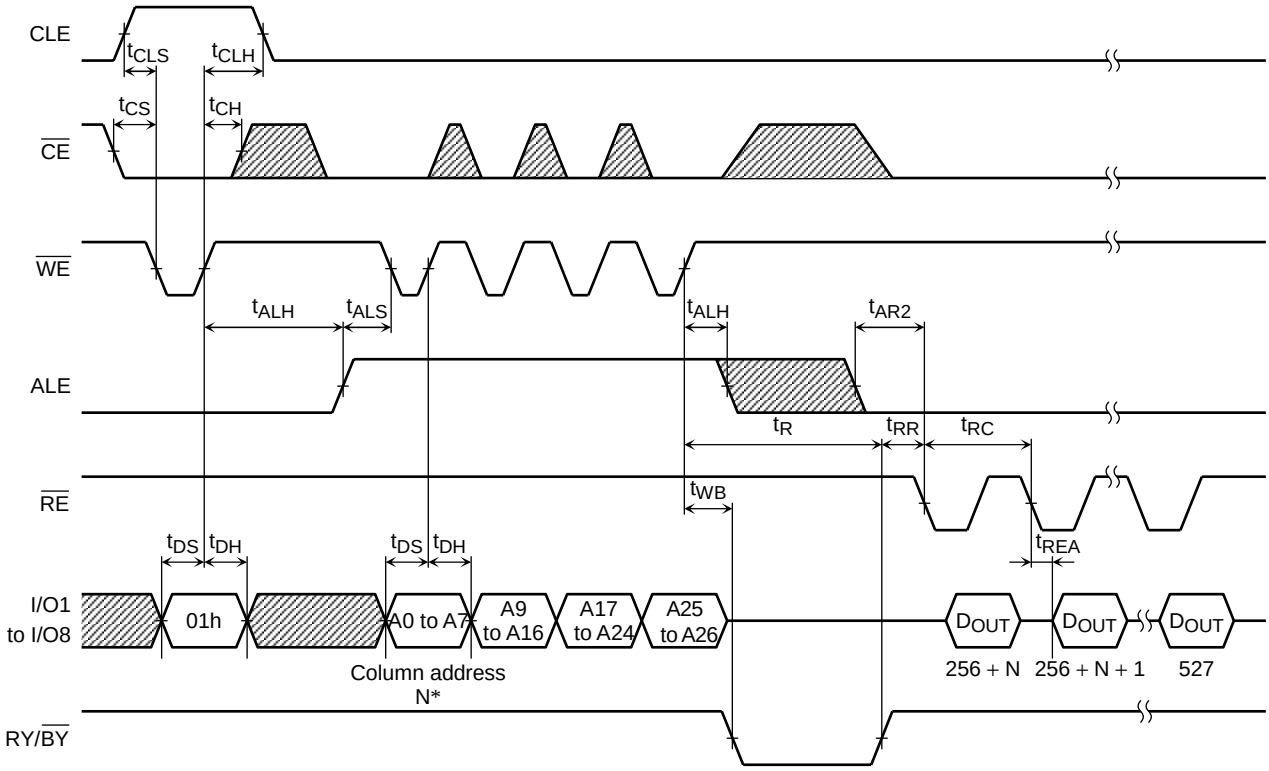
Read Cycle (1) Timing Diagram



Read Cycle (1) Timing Diagram: When Interrupted by $\overline{CE}$

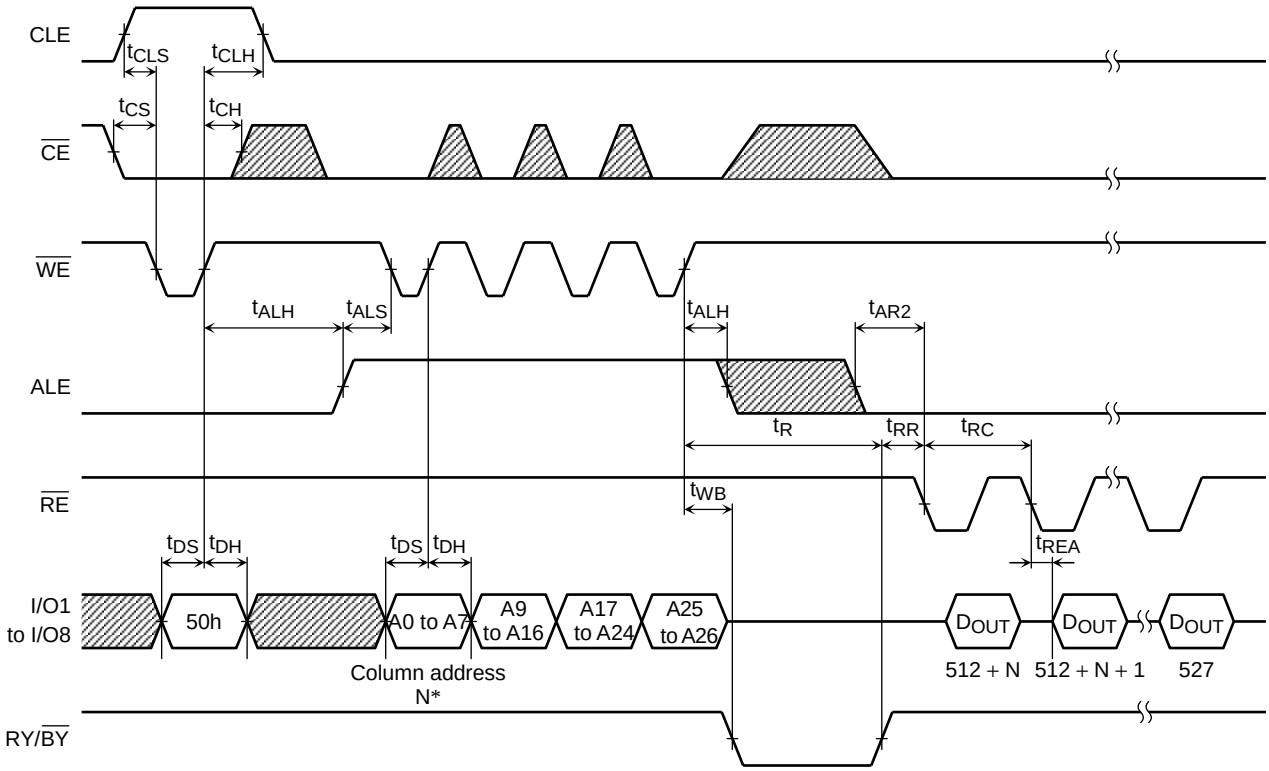


Read Cycle (2) Timing Diagram



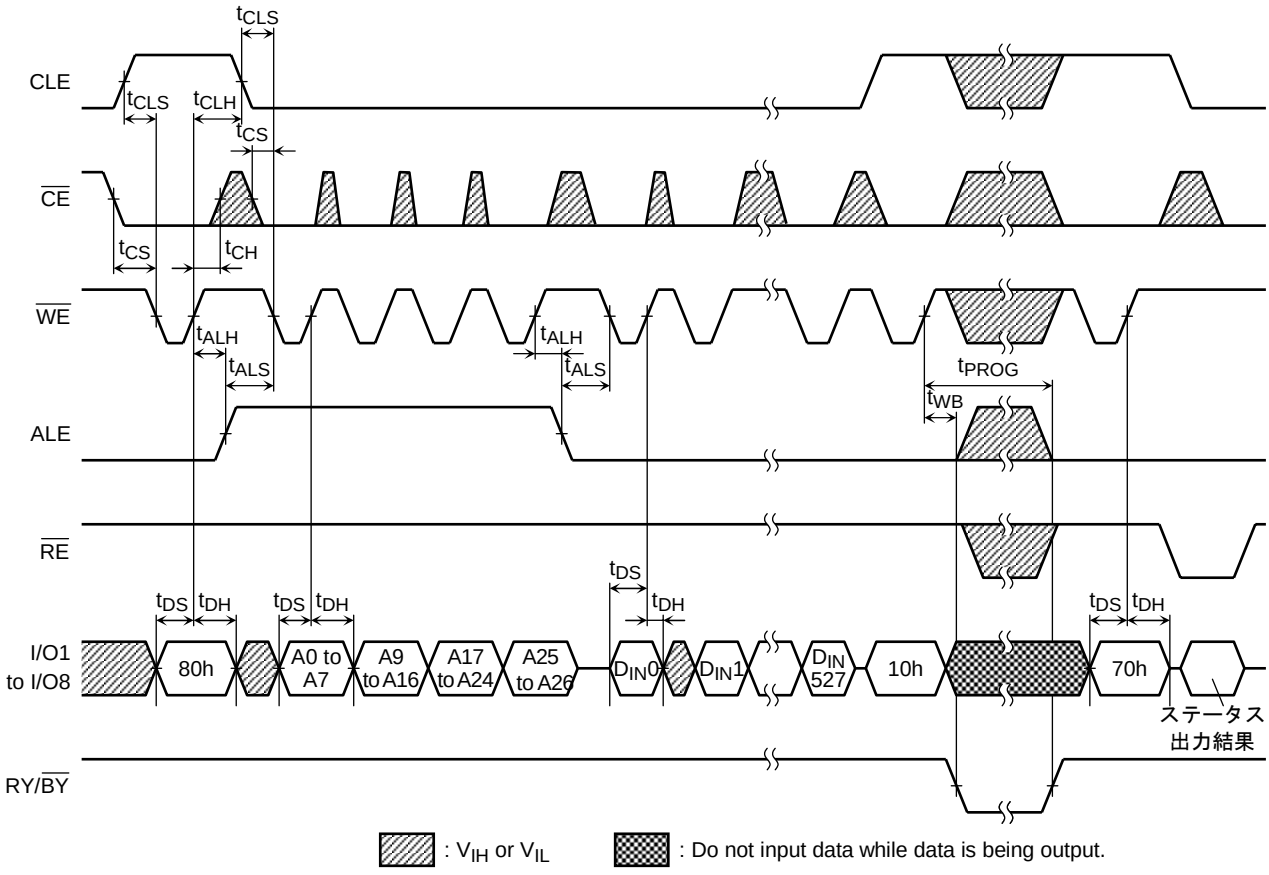
*: Read operation using 01h command N: 0 to 255

Read Cycle (3) Timing Diagram

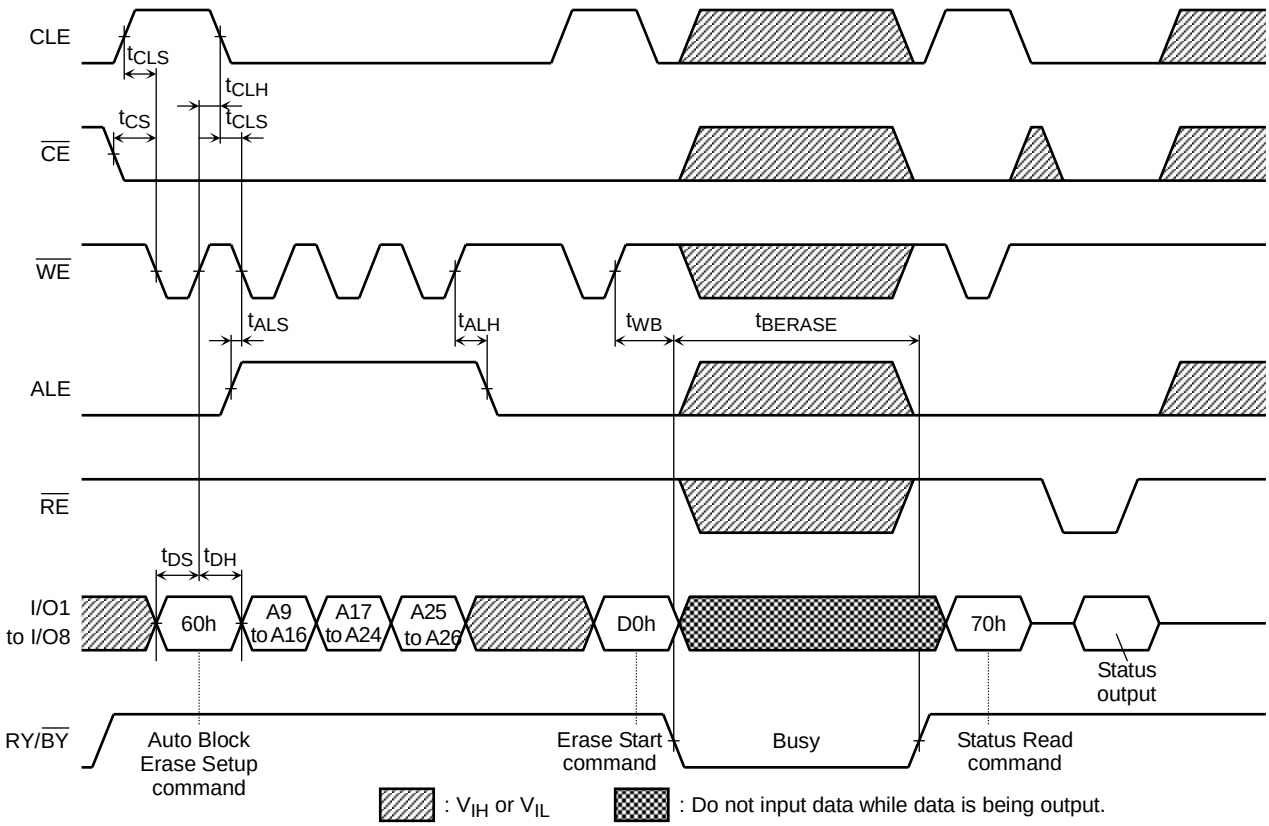


*: Read operation using 50h command N: 0 to 15

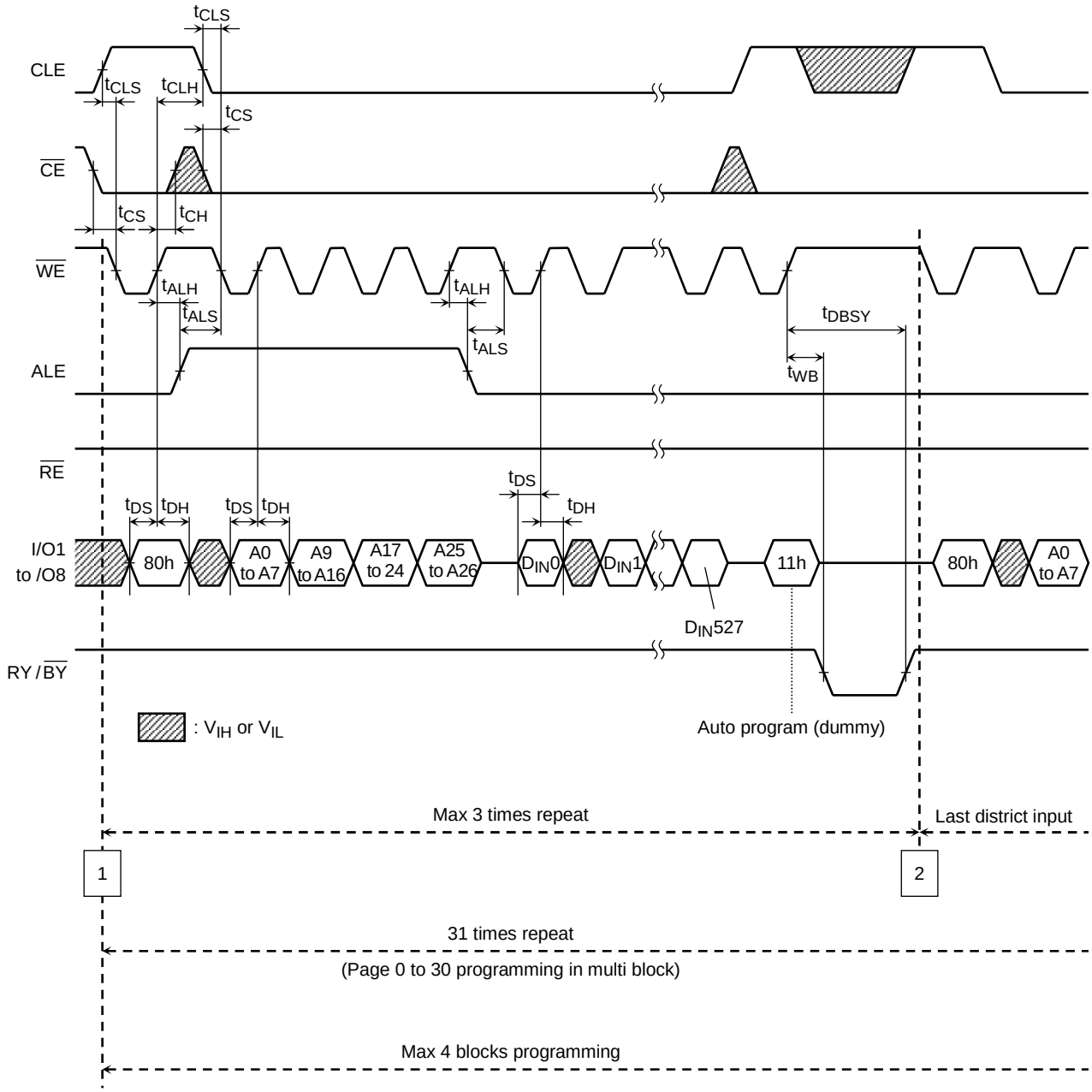
Auto-Program Operation Timing Diagram



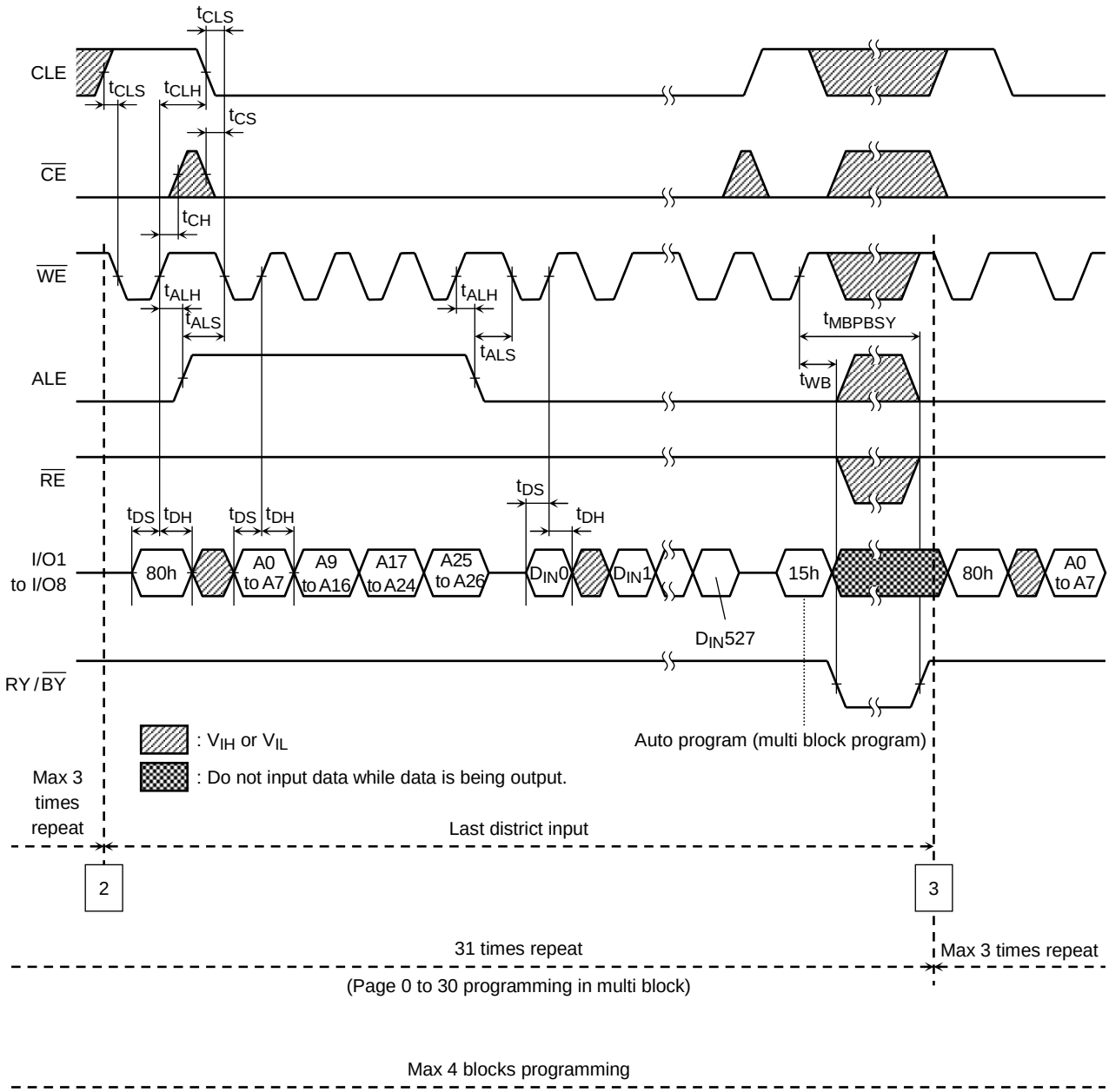
Auto Block Erase Timing Diagram



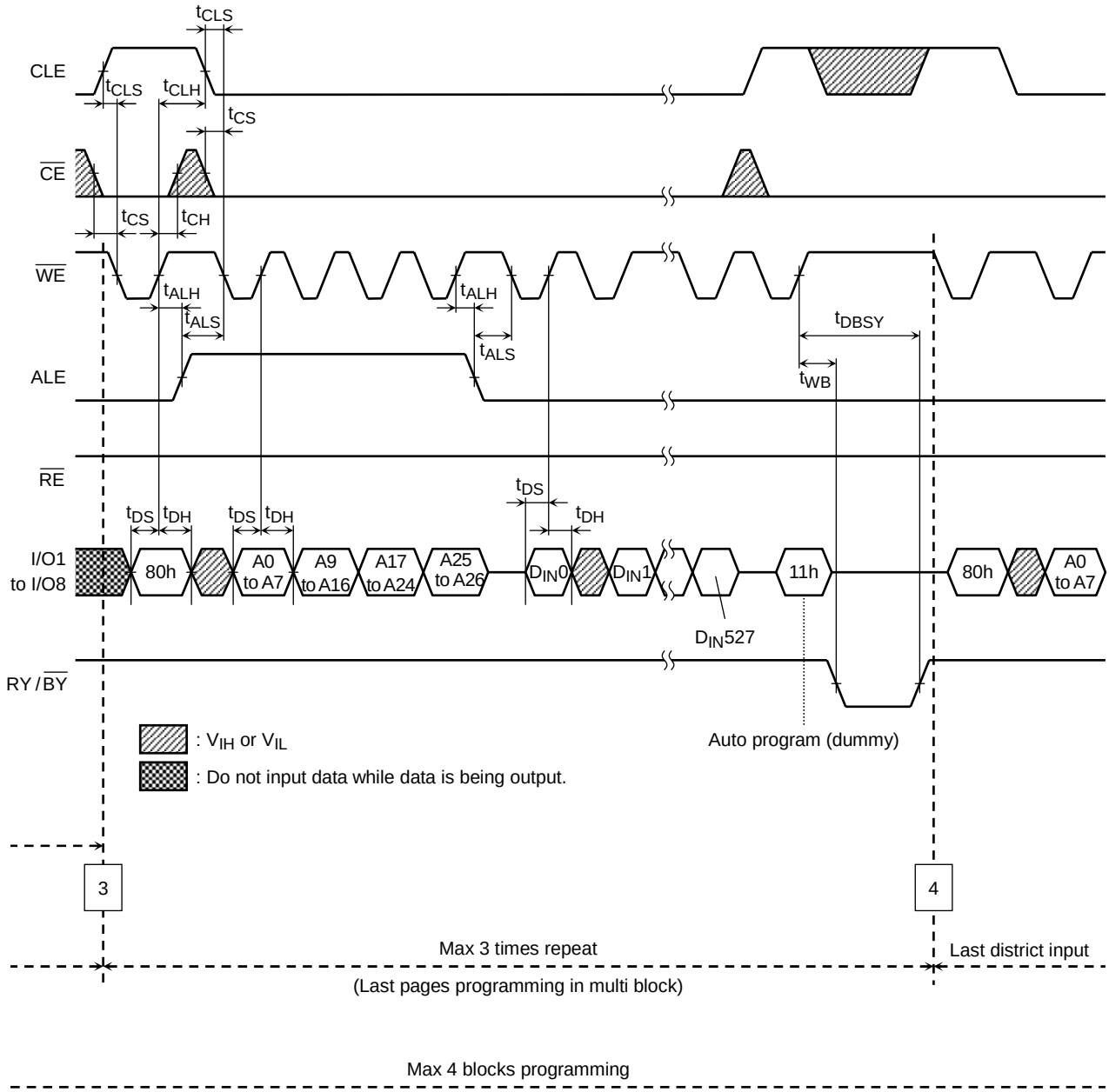
Multi Block Programming Timing (to be continued)



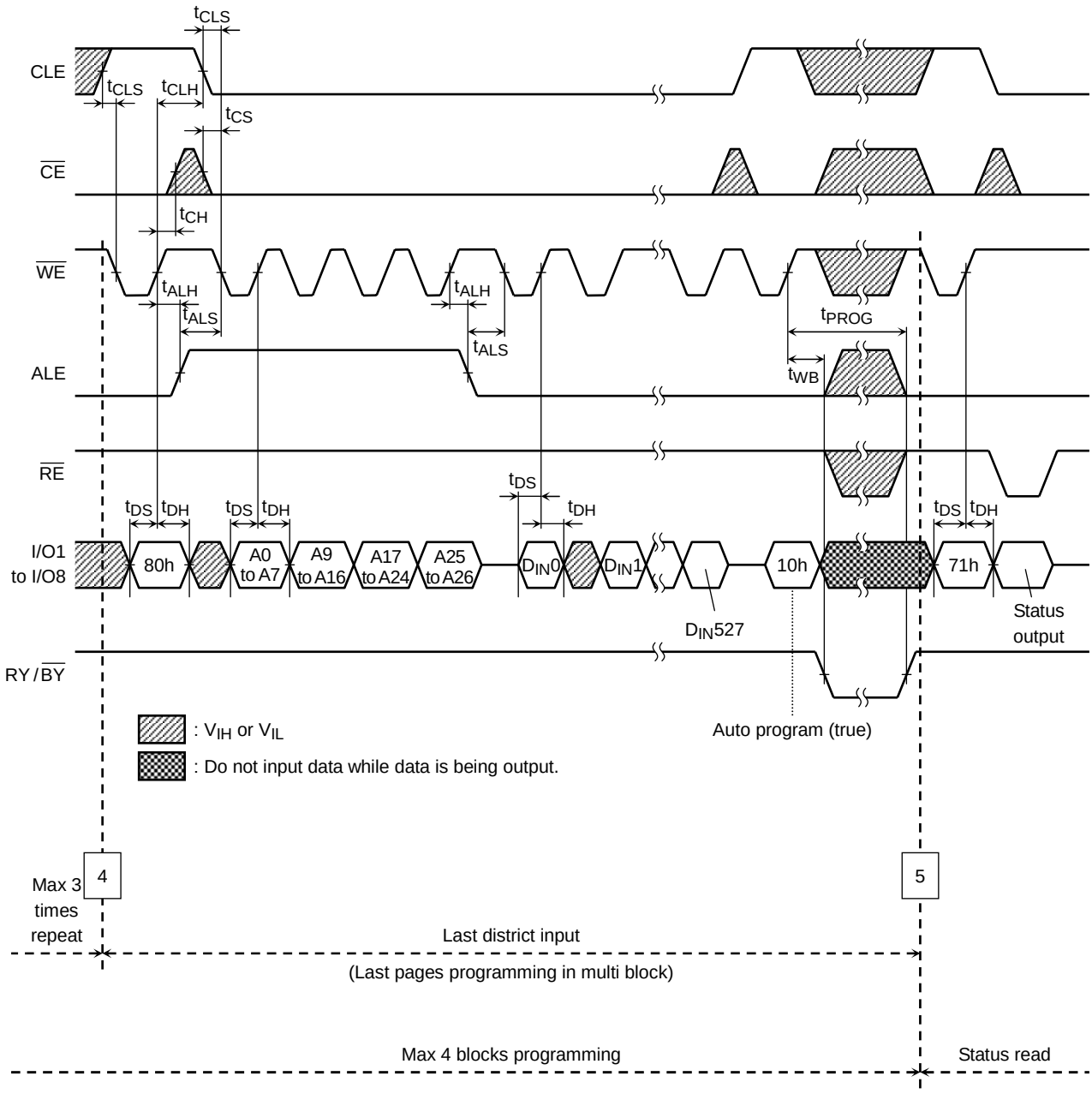
(continuation 1) Multi Block Programming Timing



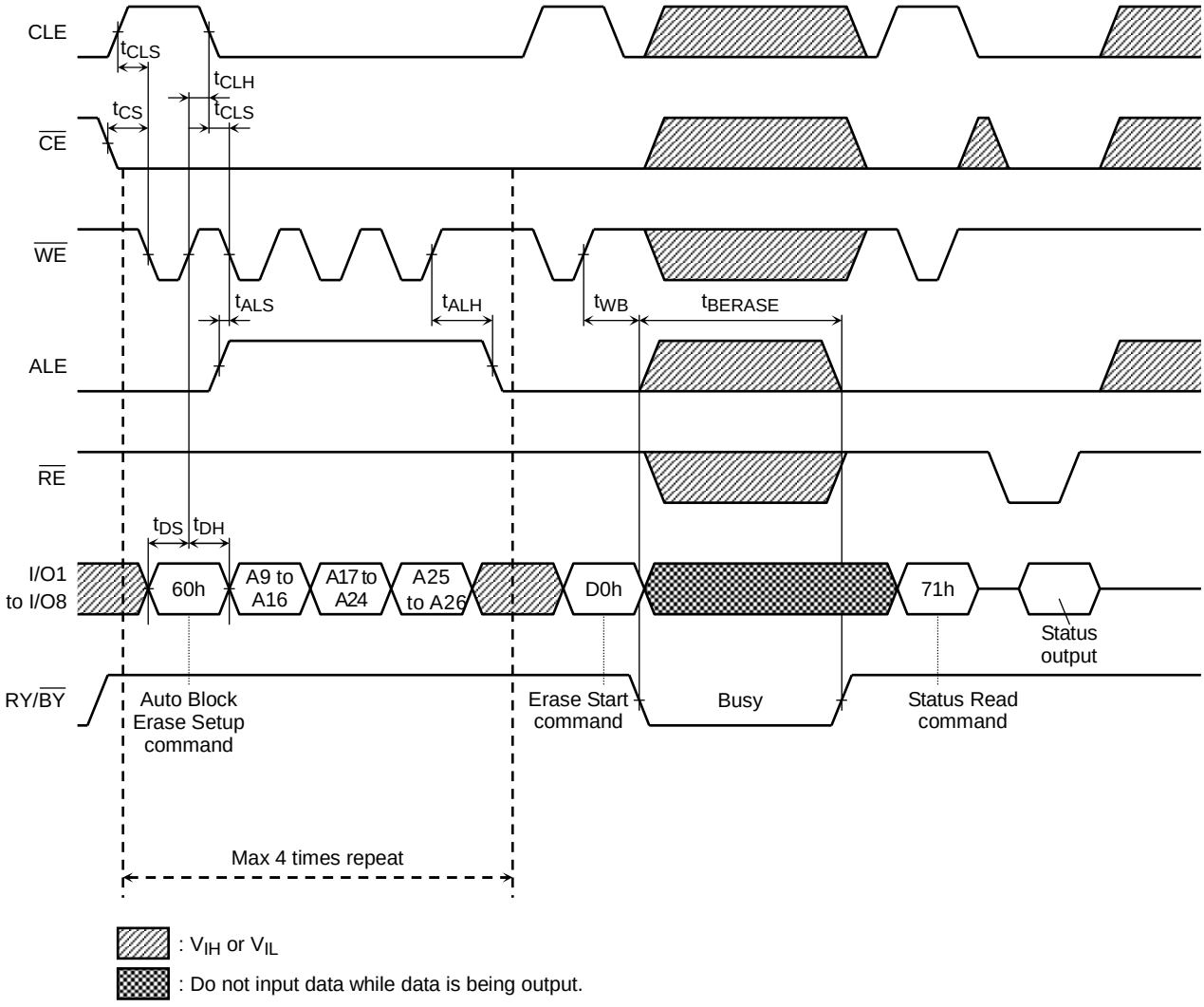
(continuation 2) Multi Block Programming Timing



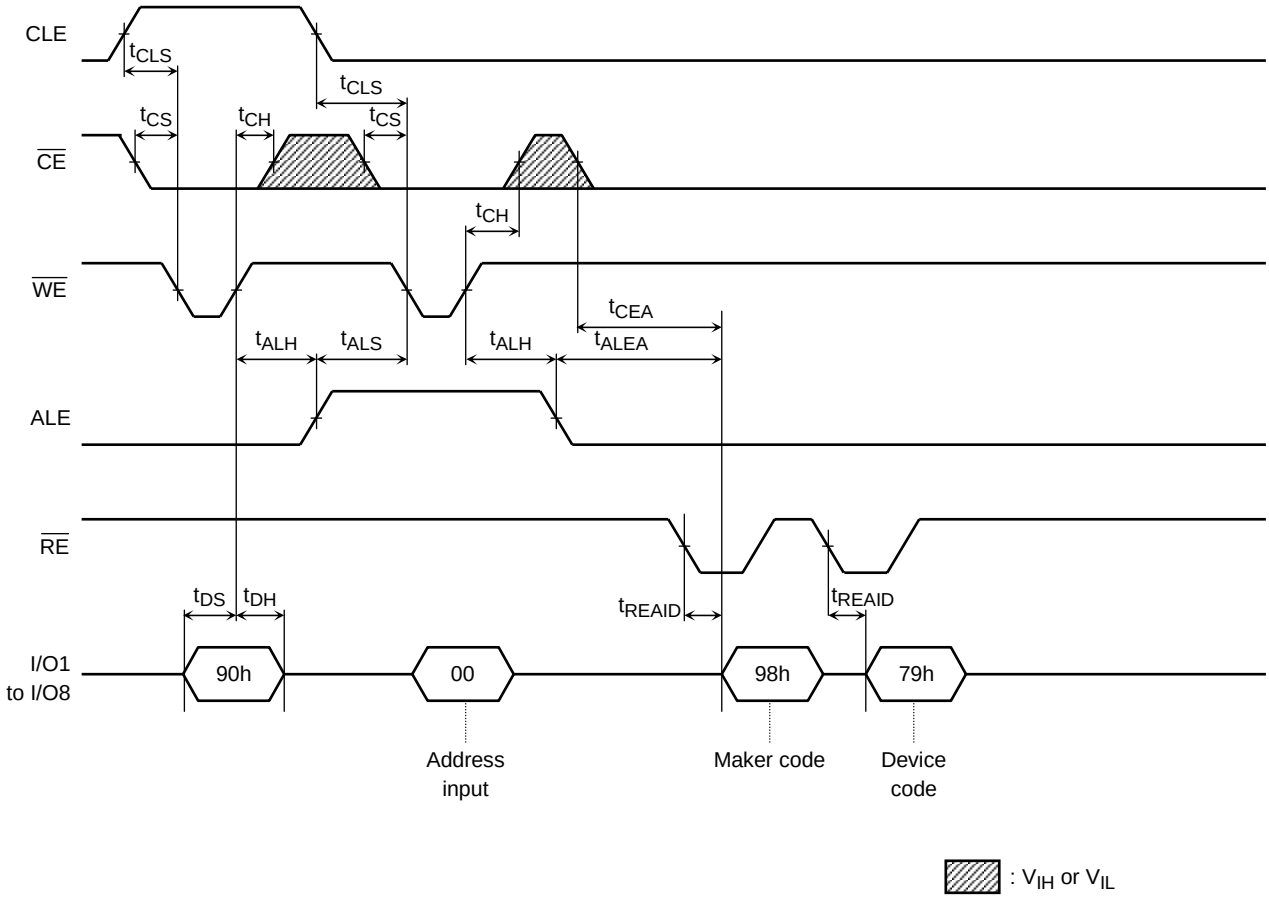
(continuation 3) Multi Block Programming Timing



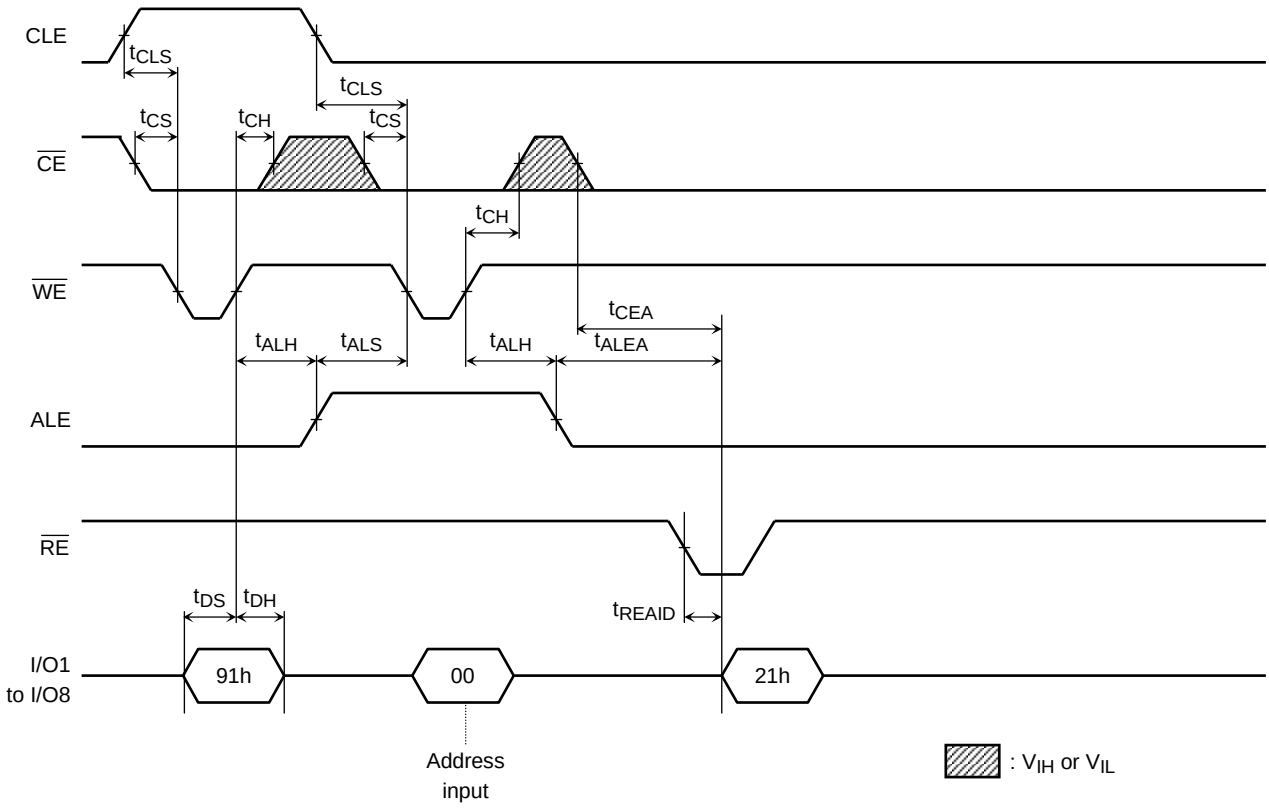
Multi Block Erase Timing Diagram



ID Read (1) Operation Timing Diagram



ID Read (2) Operation Timing Diagram



PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information.

Command Latch Enable: CLE

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is High.

Address Latch Enable: ALE

The ALE signal is used to control loading of either address information or input data into the internal address/data register.

Address information is latched on the rising edge of $\overline{WE}$ if ALE is High.

Input data is latched if ALE is Low.

Chip Enable: $\overline{CE}$

The device goes into a low-power Standby mode when $\overline{CE}$ goes High during a Read operation. The $\overline{CE}$ signal is ignored when device is in Busy state ($RY/\overline{BY}$ = L), such as during a Program or Erase operation, and will not enter Standby mode even if the $\overline{CE}$ input goes High.

Write Enable: $\overline{WE}$

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$

The $\overline{RE}$ signal controls serial data output. Data is available t_{REA} after the falling edge of $\overline{RE}$.

The internal column address counter is also incremented (Address = Address + l) on this falling edge.

I/O Port: I/O1 to 8

The I/O1 to 8 pins are used as a port for transferring address, command and input/output data to and from the device.

Write Protect: $\overline{WP}$

The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

Ready/Busy: $RY/\overline{BY}$

The $RY/\overline{BY}$ output signal is used to indicate the operating condition of the device. The $RY/\overline{BY}$ signal is in Busy state ($RY/\overline{BY}$ = L) during the Program, Erase and Read operations and will return to Ready state ($RY/\overline{BY}$ = H) after completion of the operation. The output buffer for this signal is an open drain.

Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.

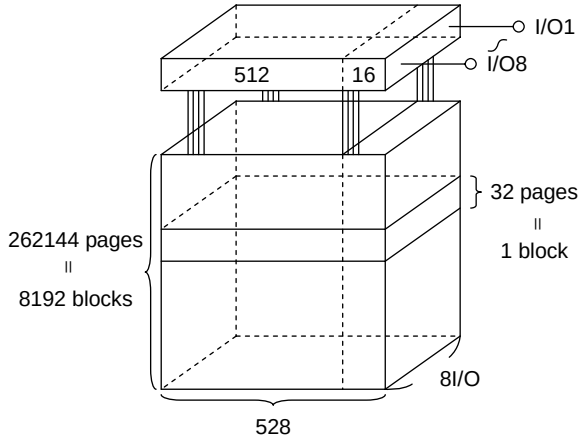


Figure 2. Schematic Cell Layout

A page consists of 528 bytes in which 512 bytes are used for main memory storage and 16 bytes are for redundancy or for other uses.

1 page = 528 bytes

1 block = 528 bytes × 32 pages = (16K + 512) bytes

Capacity = 528 bytes × 32 pages × 8192 blocks

An address is read in via the I/O port over four consecutive clock cycles, as shown in Table 1.

Table 1. Addressing

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
First cycle	A7	A6	A5	A4	A3	A2	A1	A0
Second cycle	A16	A15	A14	A13	A12	A11	A10	A9
Third cycle	A24	A23	A22	A21	A20	A19	A18	A17
Fourth cycle	*L	*L	*L	*L	*L	*L	A26	A25

A0 to A7 : Column address
A9 to A26 : Page address
A14 to A26 : Block address
A9 to A13 : NAND address in block

* : A8 is automatically set to Low or High by a 00h command or a 01h command.
* : I/O3 to I/O8 must be set to Low in the fourth cycle.

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by the nineteen different command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals, as shown in Table 2.

Table 2. Logic Table

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$ *1
Command Input	H	L	L	⌐└↑	H	*
Data Input	L	L	L	⌐└↑	H	H
Address Input	L	H	L	⌐└↑	H	*
Serial Data Output	L	L	L	H	↓└⌐	*
During Programming (Busy)	*	*	*	*	*	H
During Erasing (Busy)	*	*	*	*	*	H
Program, Erase Inhibit	*	*	*	*	*	L
Standby	*	*	H	*	*	0 V/V_{CC}

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

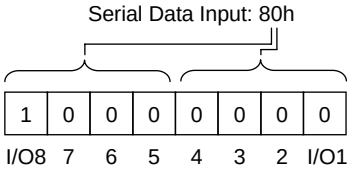
*1: Refer to Application Note (10) toward the end of this document

Table 3. Command table (HEX)

	First Cycle	Second Cycle	Acceptable while Busy
Serial Data Input	80	—	
Read Mode (1)	00	—	
Read Mode (2)	01	—	
Read Mode (3)	50	—	
Reset	FF	—	○
Auto Program (True)	10	—	
Auto Program (Dummy)	11	—	
Auto Program (Multi Block Program)	15	—	
Auto Block Erase	60	D0	
Status Read (1)	70	—	○
Status Read (2)	71	—	○
ID Read (1)	90	—	
ID Read (2)	91	—	

HEX data bit assignment

(Example)



Once the device has been set to Read mode by a 00h, 01h or 50h command, additional Read commands are not needed for sequential page Read operations.
Table 4 shows the operation states for Read mode.

Table 4. Read mode operation states

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O1 to I/O8	Power
Output Select	L	L	L	H	L	Output	Active
Output Deselect	L	L	L	H	H	High impedance	Active
Standby	L	L	H	H	*	High impedance	Standby

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

DEVICE OPERATION

Read Mode (1)

Read mode (1) is set when a "00h" command is issued to the Command register. Refer to Figure 3 below for timing details and the block diagram.

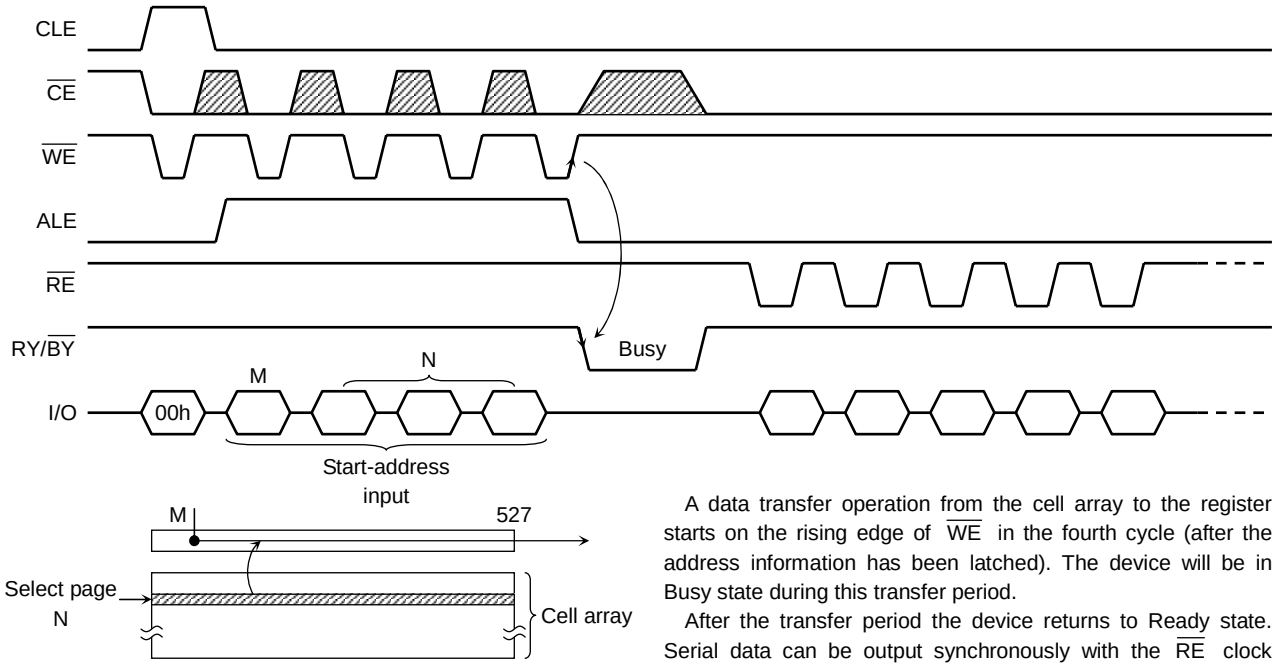


Figure 3. Read mode (1) operation

A data transfer operation from the cell array to the register starts on the rising edge of $\overline{WE}$ in the fourth cycle (after the address information has been latched). The device will be in Busy state during this transfer period.

After the transfer period the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the start pointer designated in the address input cycle.

Read Mode (2)

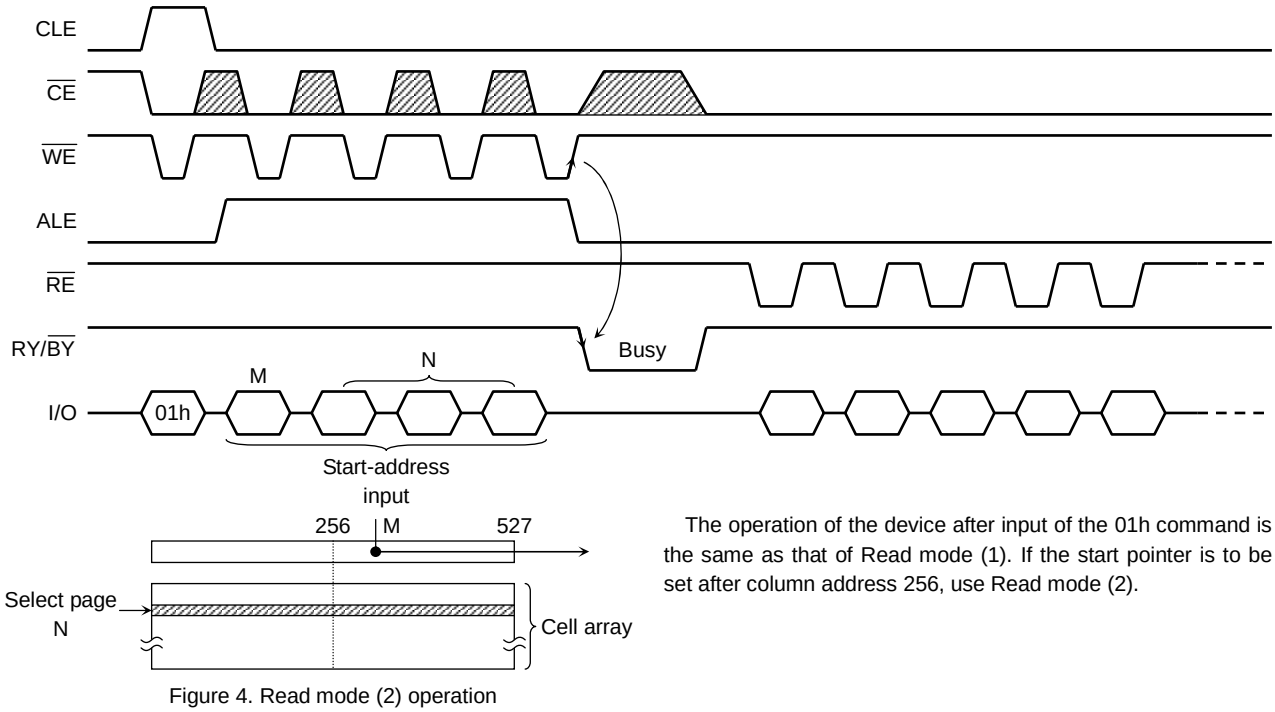


Figure 4. Read mode (2) operation

The operation of the device after input of the 01h command is the same as that of Read mode (1). If the start pointer is to be set after column address 256, use Read mode (2).

Read Mode (3)

Read mode (3) has the same timing as Read modes (1) and (2) but is used to access information in the extra 16-byte redundancy area of the page. The start pointer is therefore set to a value between byte 512 and byte 527.

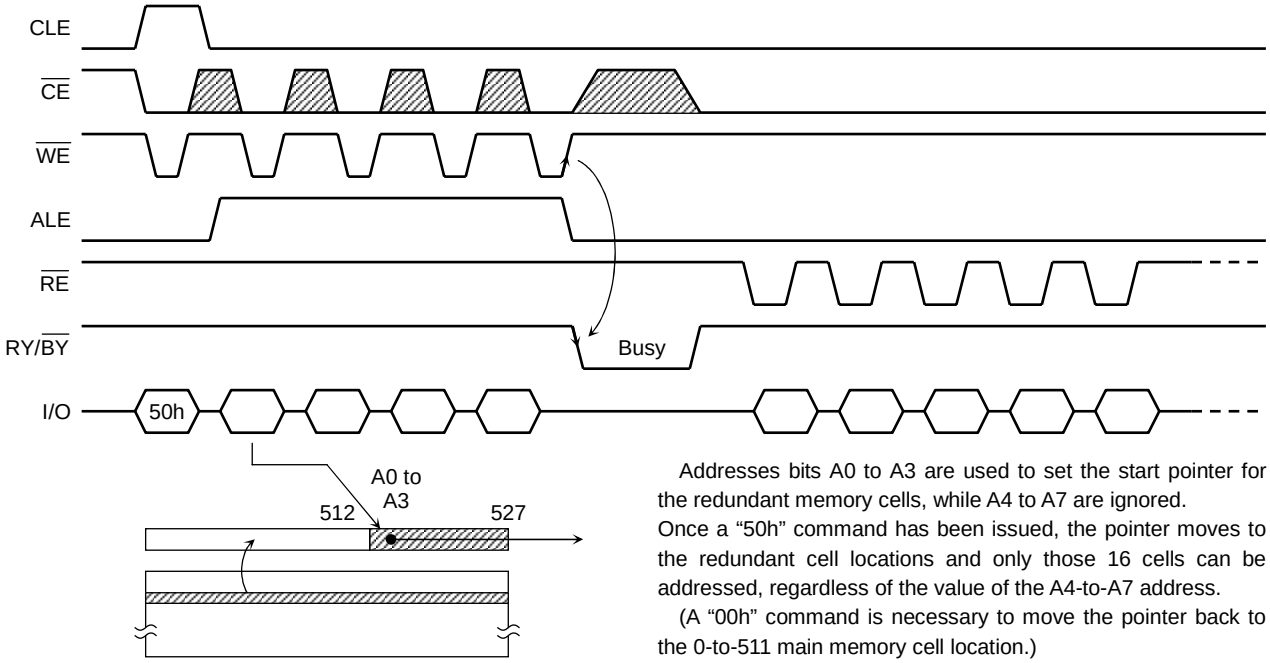


Figure 5. Read mode (3) operation

Addresses bits A0 to A3 are used to set the start pointer for the redundant memory cells, while A4 to A7 are ignored.
Once a “50h” command has been issued, the pointer moves to the redundant cell locations and only those 16 cells can be addressed, regardless of the value of the A4-to-A7 address.

(A “00h” command is necessary to move the pointer back to the 0-to-511 main memory cell location.)

Status Read

The device has three Status Read commands. There are Status Read (1) command “70h” and Status Read (2) command “71h”.

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass/fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port on the $\overline{RE}$ clock after a Status Read command “70h” or “71h” input.
The resulting information of Status Read (1) command “70h” is outlined in Table 5 below and the resulting information of Status Read (2) command “71h” are outlined in the explanation for Multi Block Program and Multi Block Erase toward the end of this document.

Table 5. Status output table for Status Read (1) command “70h”

	STATUS	OUTPUT	
I/O1	Pass/Fail	Pass: 0	Fail: 1
I/O2	Not Used	0	
I/O3	Not Used	0	
I/O4	Not Used	0	
I/O5	Not Used	0	
I/O6	Not Used	0	
I/O7	Ready/Busy	Ready: 1	Busy: 0
I/O8	Write Protect	Protect: 0	Not Protected: 1

The Pass/Fail status on I/O1 is only valid when the device is in the Ready state.

An application example with multiple devices is shown in Figure 6.

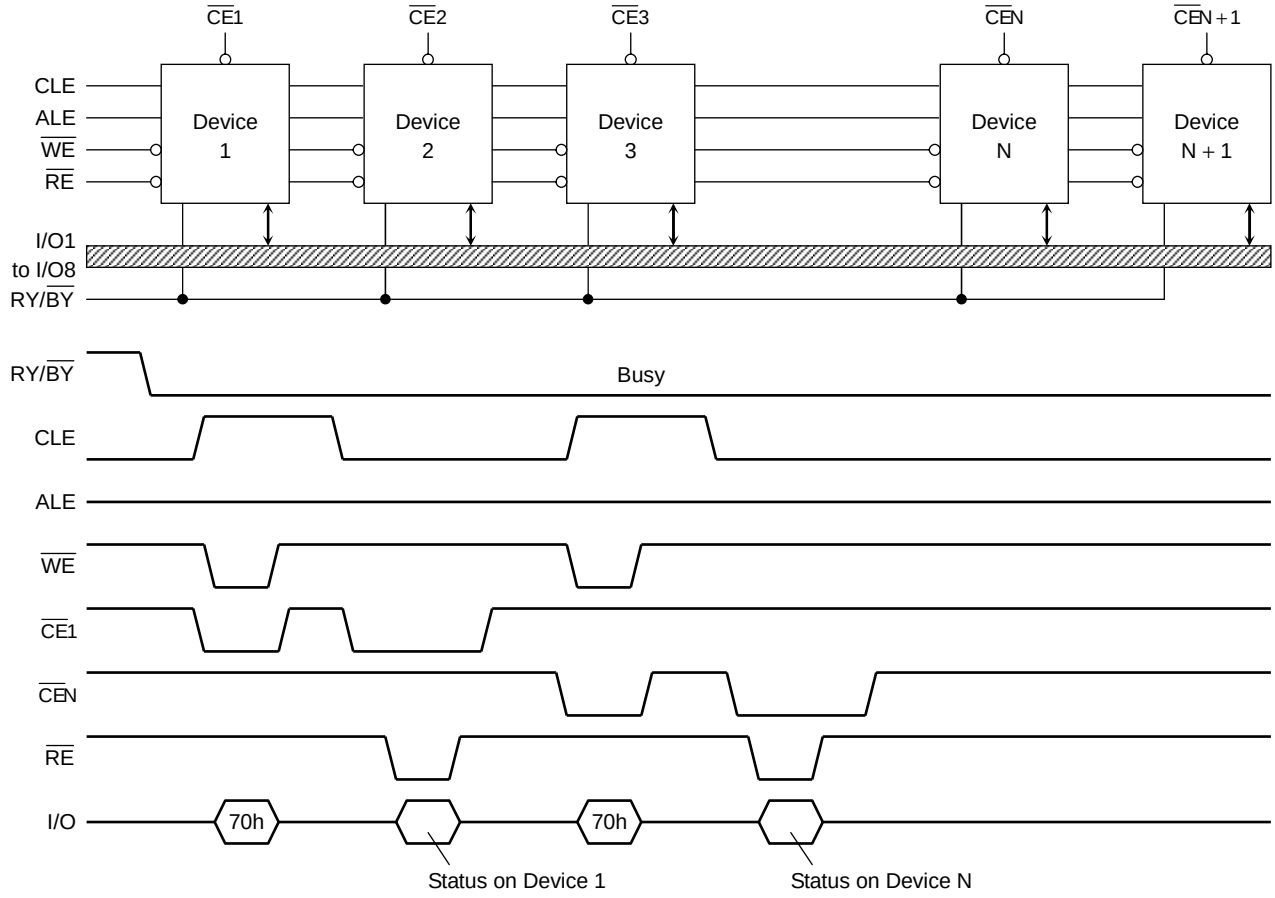


Figure 6. Status Read timing application example

System Design Note: If the RY/$\overline{BY}$ pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

Auto Page Program

The device carries out an Automatic Page Program operation when it receives a “10h” Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)

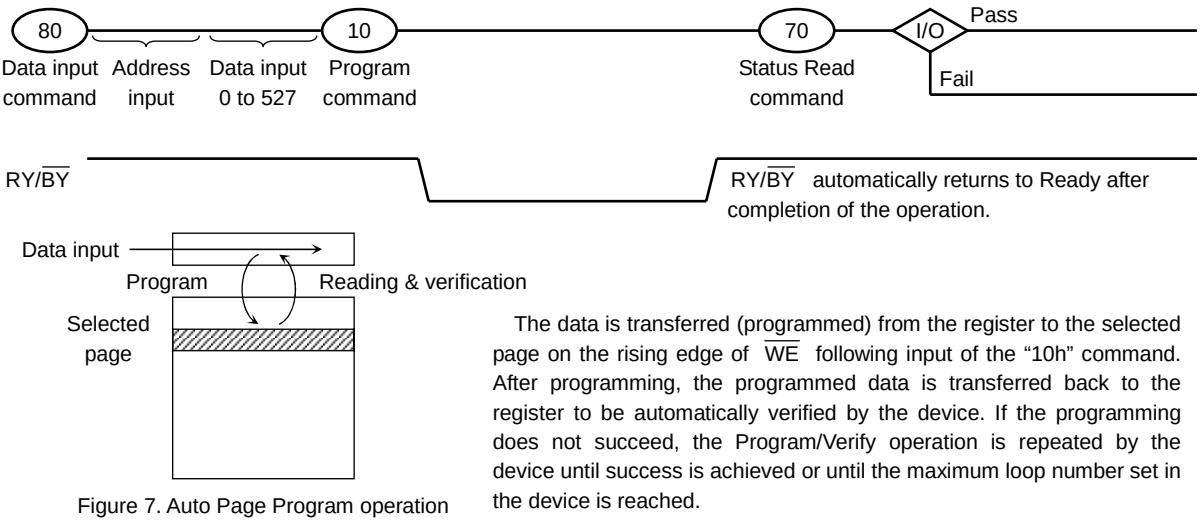
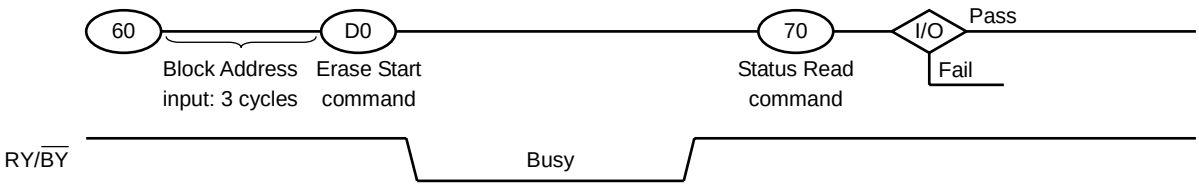


Figure 7. Auto Page Program operation

The data is transferred (programmed) from the register to the selected page on the rising edge of $\overline{WE}$ following input of the “10h” command. After programming, the programmed data is transferred back to the register to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Auto Block Erase

The Auto Block Erase operation starts on the rising edge of $\overline{WE}$ after the Erase Start command “D0h” which follows the Erase Setup command “80h”. This two-cycle process for Erase operations acts as an ertra layer of protection from aceidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.

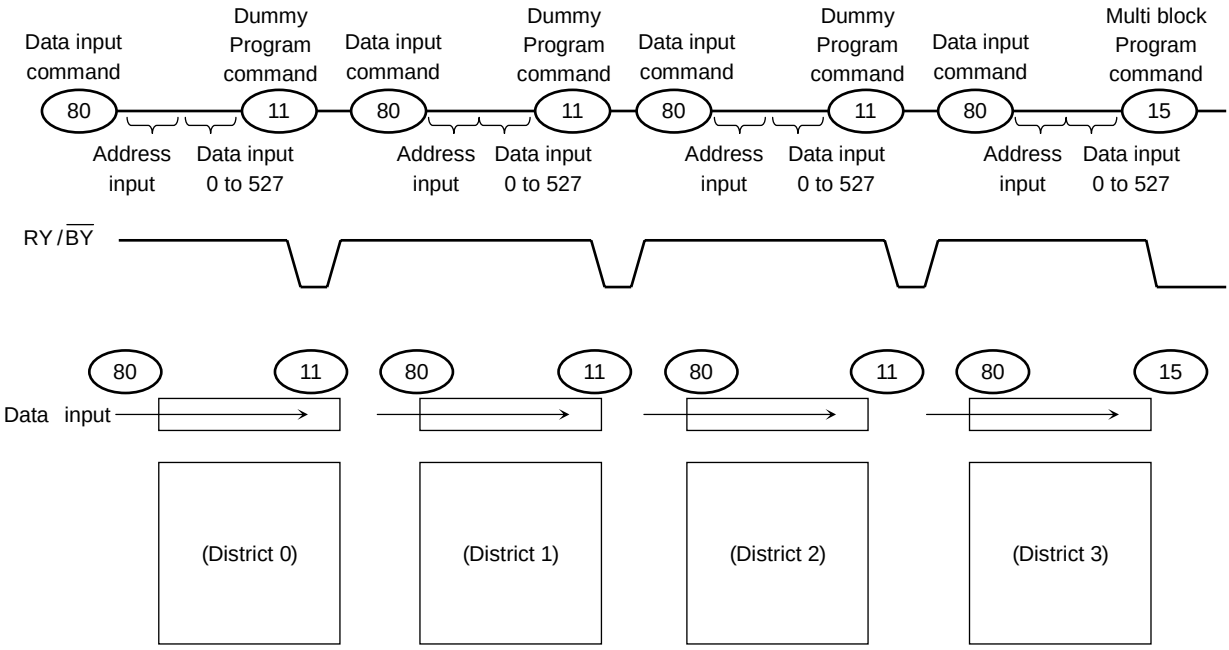


Multi Block Program

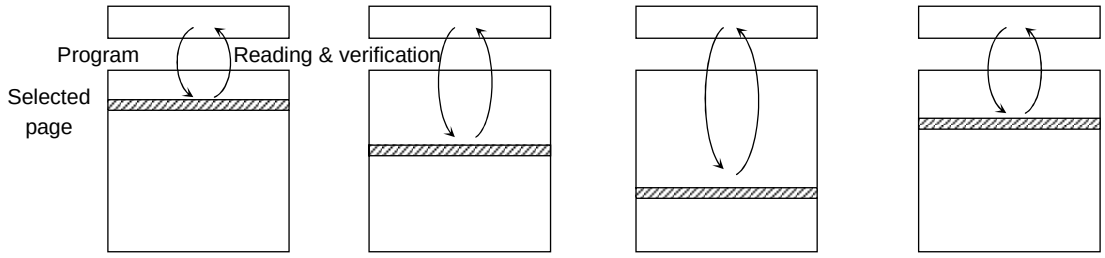
The device carries out an Multi Block Program operation when it receives a “15h” or “10h” Program command after some sets of the address and data have been input.

In the interval of the Multi District adress and the (512 + 16 byte) data input, “11h” Dummy Program command is used when it still continues the data input into another District.

The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)



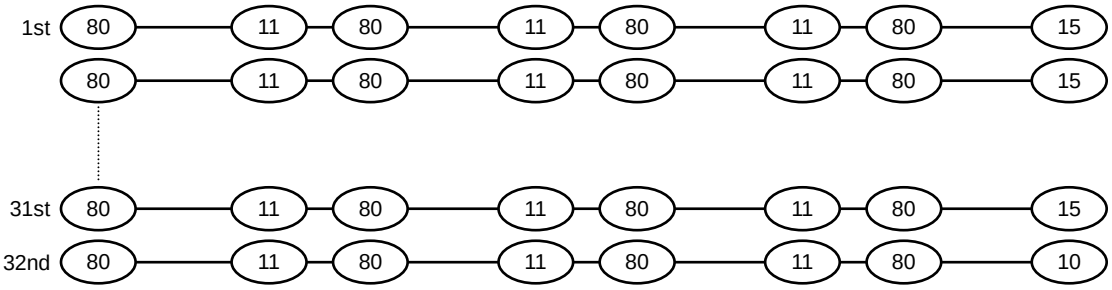
After “15h” Multi Block Program command, physical programing starts as follows.



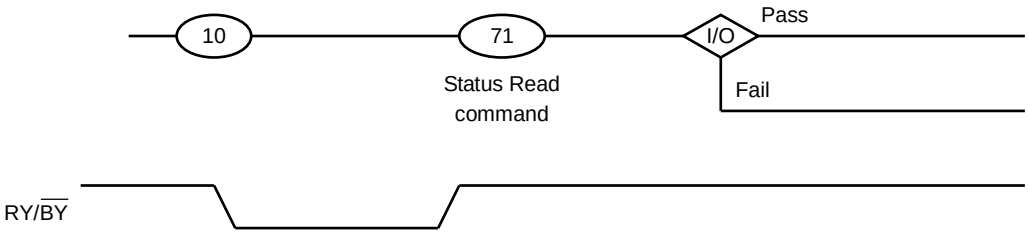
The data is transferred (programmed) from the register to the selected page on the rising edge of -WE following input of the “15h” command. After programming, the programmed data is transferred back to the register to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Starting the above operation from 1st page of the selected erase blocks, and then repeating the operation total 31 times with incrementing the page address in the blocks, and then input the last page data of the blocks, "10h" command executes final programming.

In this full sequence, the command sequence is following.



After the "10h" command, the total results of the above operation is shown through the Status Read command.



The Status discription of 71h command is following.

	STATUS	OUTPUT	
I/O1	Total Pass/Fail	Pass: 0	Fail: 1
I/O2	District 0 Pass/Fail	Pass: 0	Fail: 1
I/O3	District 1 Pass/Fail	Pass: 0	Fail: 1
I/O4	District 2 Pass/Fail	Pass: 0	Fail: 1
I/O5	District 3 Pass/Fail	Pass: 0	Fail: 1
I/O6	Not Used	Do not care	
I/O7	Ready/Busy	Ready: 1	Busy: 0
I/O8	Write Protect	Protect: 0	Not Protect: 1

I/O1 describes total Pass/Fail condition. If at least one fail occurred in 32 times × 4 (512 + 16 byte) page write operation, it shows "Fail" condition.

I/O2 describes Pass/Fail condition. If more than one fail occurred in 32 times (512 + 16 byte) page write operation in District 0 area, it shows "Fail" condition.

I/O3, I/O4 and I/O5 are as same manner as I/O2.

Internal addressing in relation with the Districts

To use Multi Block Program operation, the internal addressing should be conscious in relation with the District.

- The device consists of 4 Districts.
- Each District consists from 2048 erase blocks.
- The allocation rule is follows.

District 0: Block 0, Block 4, Block 8, Block 12, ….., Block 8188
District 1: Block 1, Block 5, Block 9, Block 13, ….., Block 8189
District 2: Block 2, Block 6, Block 10, Block 14, ….., Block 8190
District 3: Block 3, Block 7, Block 11, Block 15, ….., Block 8191

Address input restriction for the Multi Block Program operation

In selecting the blocks for the Multi Block Program operation, following is the restriction and acceptance.

(Restriction)
Maximum one block should be selected from each District.
The data input operation should be started from the same number page of the each selected block and then, the page number in the blocks should be same number at the same time programming.

(Acceptance)
There is no order limitation of the District for the address input.
Any number of the District can be select for the programming.
So, for example, following operations are in acceptance.
Example 1 : (80) [District 2] (11) (80) [District 0] (11) (80) [District 1] (15)
Example 2 : (80) [District 0] (11) (80) [District 1] (11) (80) [District 2] (11) (80) [District 3] (15)

It requires no mutual address relation between the selected blocks from each District.

Operating restriction during the Multi Block Program operation

(Restriction)
Starting from 1st page data input, until issuing “10h” command, any other command out of defined sequence can not be issued except Status Read command and Reset command.

(Acceptance)
The data input operation can be terminated with “10h” command instead of “15h” command in the middle of the page number in the block.
In this case the Status represents the reflected value accumulated from 1st page programming of this sequence and up to the last page programming terminated by “10h” command.

Status Read operation

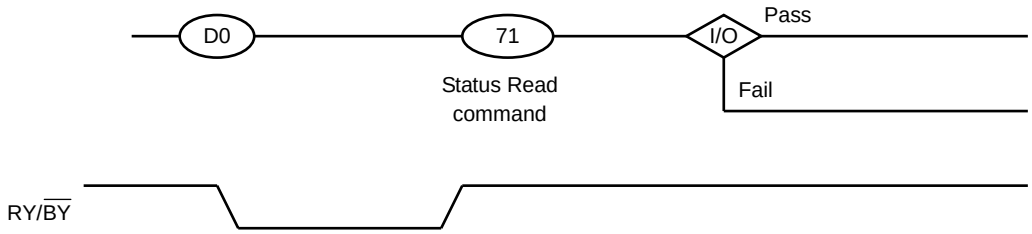
Untill the Ready condition after the programming terminated by “10h” command, effective bit in the Status data is limited on Ready/Busy bit.

In other words, Pass/Fail condition can be checked only in the Ready condition after “10h” command.

Multi Block Erase

The device carries out a Multi Block Erase operation when it receives a “D0h” command after some sets of the address have been input.

After the “D0h” command, the total results of Erase operation is shown through the Status Read command “71h”.



The Status discription of 71h command is following.

	STATUS	OUTPUT	
I/O1	Total Pass/Fail	Pass: 0	Fail: 1
I/O2	District 0 Pass/Fail	Pass: 0	Fail: 1
I/O3	District 1 Pass/Fail	Pass: 0	Fail: 1
I/O4	District 2 Pass/Fail	Pass: 0	Fail: 1
I/O5	District 3 Pass/Fail	Pass: 0	Fail: 1
I/O6	Not Used	Do not care	
I/O7	Ready/Busy	Ready: 1	Busy: 0
I/O8	Write Protect	Protect: 0	Not Protect: 1

I/O1 describes total Pass/Fail condition. If at least one fail occurred in Max 4 Blocks erase operation, it shows “Fail” condition.

I/O2 describes Pass/Fail condition. If fail occurred in District 0 area, it shows “Fail” condition.

I/O3, I/O4 and I/O5 are as same manner as I/O2.

Internal addressing in relation with the Districts

To use Multi Block Erase operation, the internal addressing should be conscious in relation with the Districts.

- The device consists of 4 Districts.
- Each District consists from 2048 erase blocks.
- The allocation rule is follows.

  District 0: Block 0, Block 4, Block 8, Block 12, ….., Block 8188
  District 1: Block 1, Block 5, Block 9, Block 13, ….., Block 8189
  District 2: Block 2, Block 6, Block 10, Block 14, ….., Block 8190
  District 3: Block 3, Block 7, Block 11, Block 15, ….., Block 8191

Address input restriction for the Multi Block Erase operation

In selecting the blocks for the Multi Block Erase operation, following is the restriction and acceptance.

(Restriction)
Maximum one block should be selected from each District.

(Acceptance)
There is no order limitation of the District for the address input.
Any number of the Districts can be select for the erase operation.
So, for example, following operation are in acceptance.
Example 1 : (60) [District 2] (60) [District 0] (60) [District 1] (D0)
Example 2 : (60) [District 0] (60) [District 1] (60) [District 2] (60) [District 3] (D0)

It requires no mutual address relation between the selected blocks from each District.

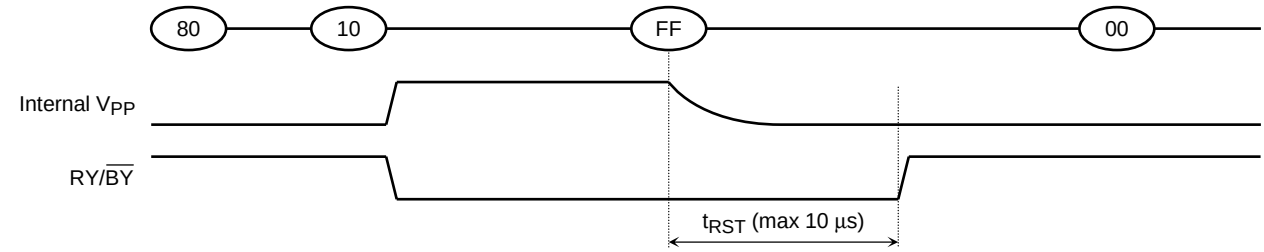
Reset

The Reset mode stops all operations. For example, in the case of a Program or Erase operation the internally generated voltage is discharged to 0 volts and the device enters Wait state.

The response to an "FFH" Reset command input during the various device operations is as follows:

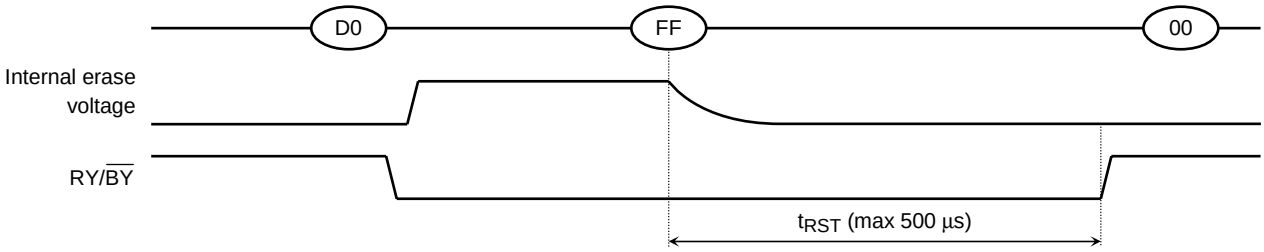
When a Reset (FFh) command is input during programming

Figure 8.



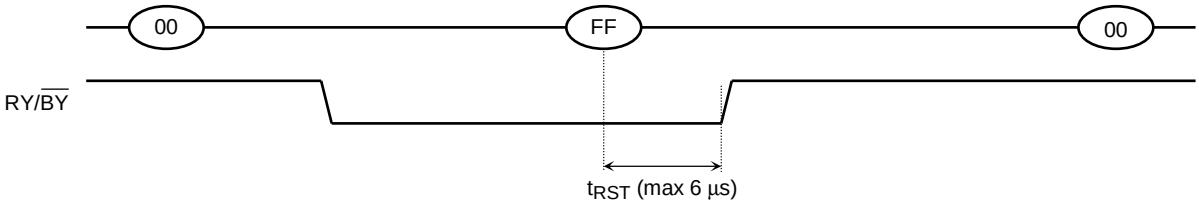
When a Reset (FFh) command is input during erasing

Figure 9.



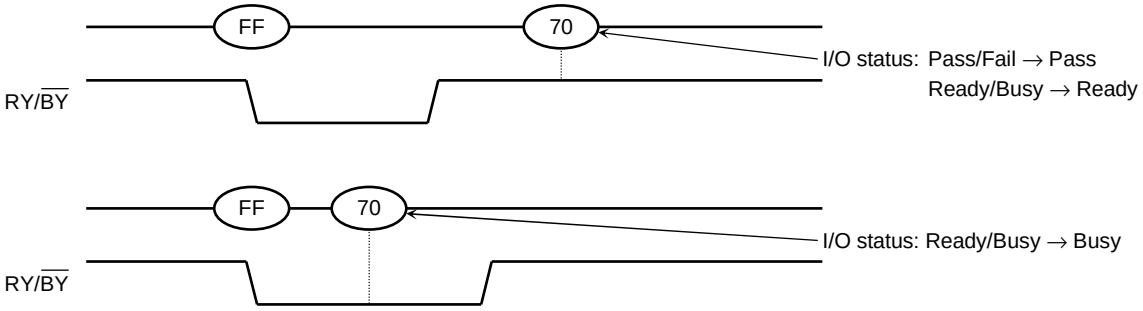
When a Reset (FFh) command is input during Read operation

Figure 10.



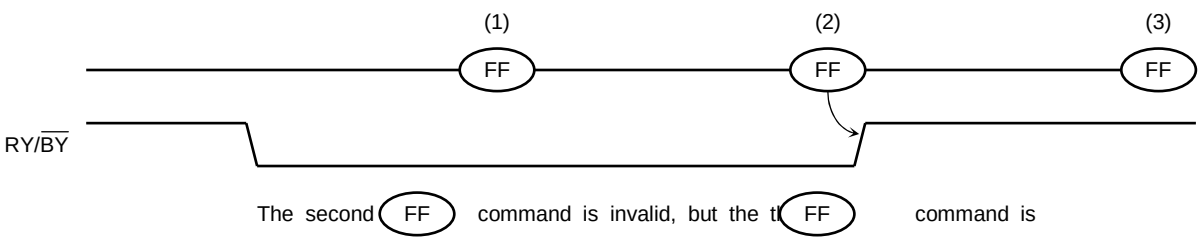
When a Status Read command (70h) is input after a Reset

Figure 11.



When two or more Reset commands are input in succession

Figure 12.



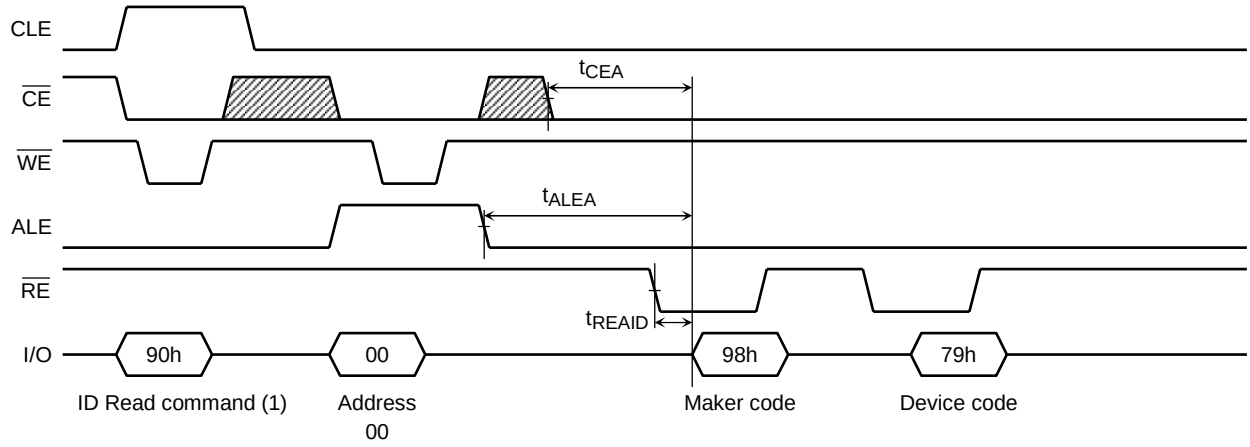
The second FF command is invalid, but the th FF command is

ID Read (1)

The device contains ID codes which identify the device type and the manufacturer.

The device has 2 types of ID read command, i.e. ID Read (1) command 90h and ID Read (2) command 91h.

ID Read (1) command 90h provides maker code and device code. The ID codes can be read out under the following timing conditions:



For the specifications of the access times t_{REAID}, t_{CEA} and t_{ALEA} refer to the AC Characteristics.

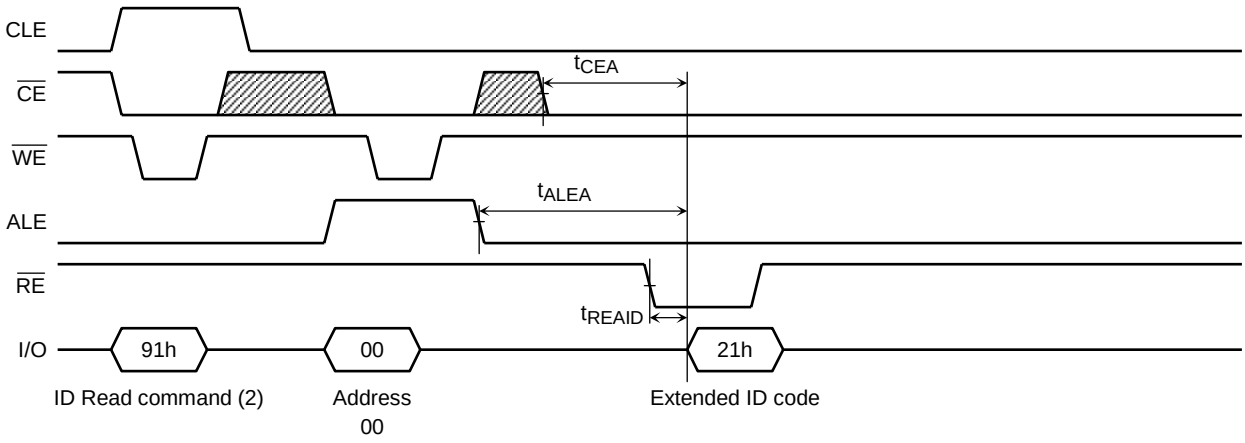
Figure 13. ID Read timing

Table 6. ID Codes read out by ID read command (1) 90h

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
Maker code	1	0	0	1	1	0	0	0	98h
Device code	0	1	1	1	1	0	0	1	79h

ID Read (2)

ID Read (2) command 91h provides ×4-block mode availability. If ID code read out by 91h is 21h, it indicates the device has ×4-block mode.



For the specifications of the access times t_{REAID}, t_{CEA} and t_{ALEA} refer to the AC Characteristics.

Figure 14. ID Read timing

Table 7. ID Codes read out by command 91h

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
Extended ID code	0	0	1	0	0	0	0	1	21h

APPLICATION NOTES AND COMMENTS

(1) Power-on/off sequence:

The $\overline{WP}$ signal is useful for protecting against data corruption at power-on/off. The following timing sequence is necessary.

The $\overline{WP}$ signal may be negated any time after the V_{CC} reaches 2.5 V and $\overline{CE}$ signal is kept high in power up sequence.

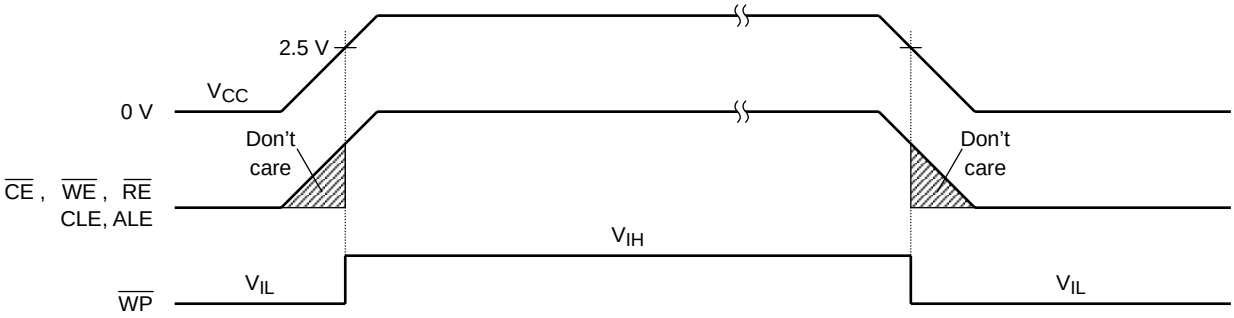


Figure 15. Power-on/off Sequence

In order to operate this device stably, after V_{CC} becomes 2.5 V, it recommends starting access after about 200 μs.

(2) Status after power-on

The following sequence is necessary because some input signals may not be stable at power-on.

Reset

Figure

(3) Prohibition of unspecified commands

The operation commands are listed in Table 3. Input of a command other than those specified in Table 3 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

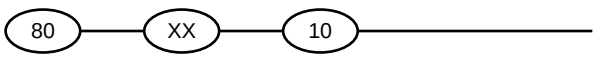
(4) Restriction of command while Busy state

During Busy state, do not input any command except 70h, 71h and FFH.

(5) Acceptable commands after Serial Input command "80h"

Once the Serial Input command "80h" has been input, do not input any command other than the Program Execution command "10h", "11h" or "15h" or the Reset command "FFH".

If a command other than "10h", "11h", "15h" or "FFH" is input, the Program operation is not performed.



Command other than "10h", "11h", "15h" or "FFH"

Programming cannot be

For this operation the "FFH" command is

(6) Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.

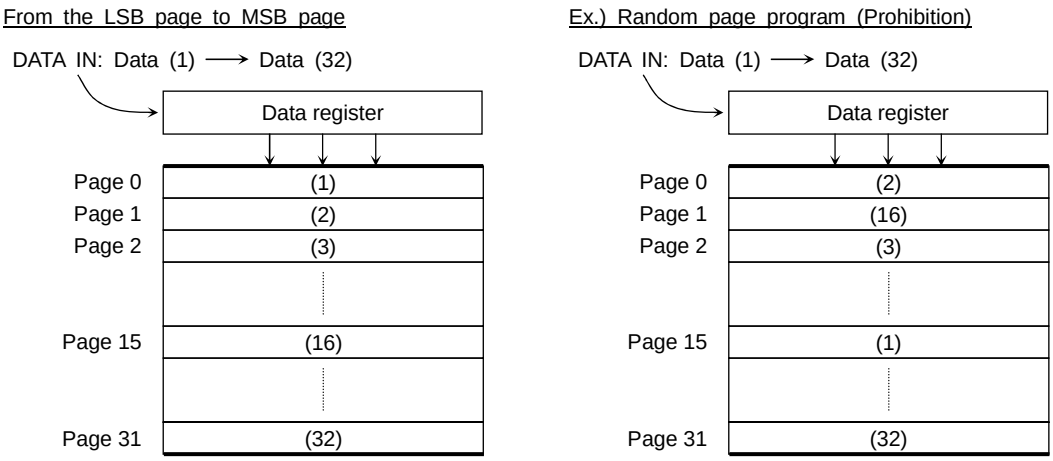


Figure 17. page programming within a block

(7) Status Read during a Read operation

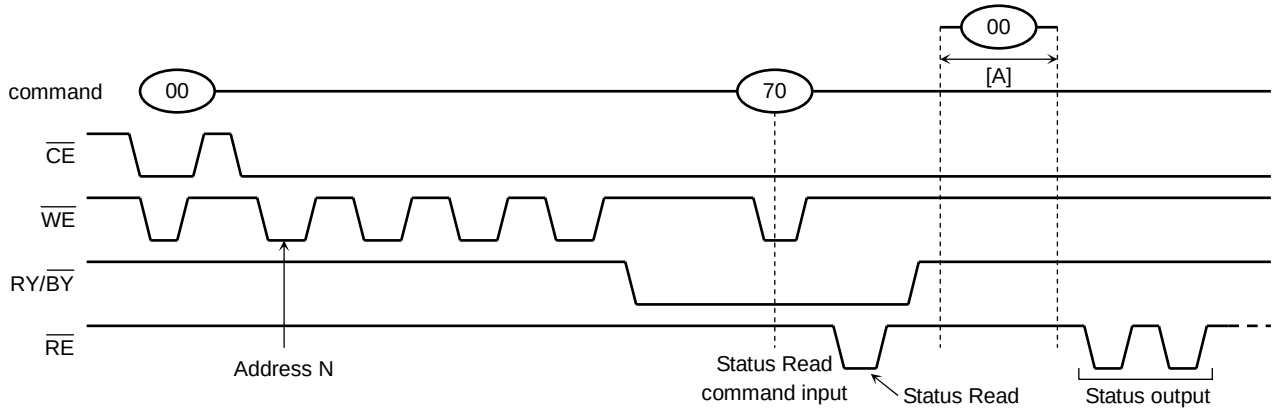


Figure 18.

The device status can be read out by inputting the Status Read command “70h” in Read mode.

Once the device has been set to Status Read mode by a “70h” command, the device will not return to Read mode.

Therefore, a Status Read during a Read operation is prohibited.

However, when the Read command “00h” is input during [A], Status mode is reset and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary

(8) Pointer control for “00h”, “01h” and “50h”

The device has three Read modes which set the destination of the pointer. Table 7 shows the destination of the pointer, and Figure 14 is a block diagram of their operations.

Table 8. Pointer Destination

Read Mode	Command	Pointer
(1)	00h	0 to 255
(2)	01h	256 to 511
(3)	50h	512 to 527

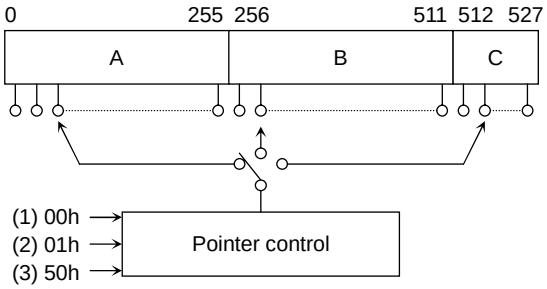
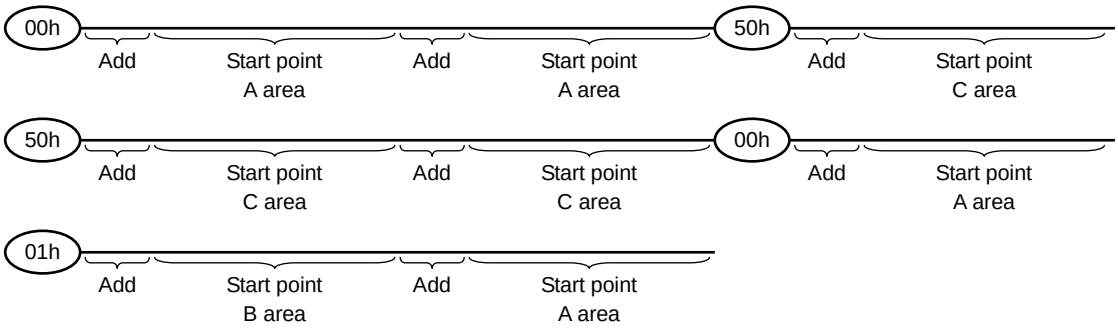


Figure 19. Pointer control

The pointer is set to region A by the “00h” command, to region B by the “01h” command, and to region C by the “50h” command.

(Example)

The “00h” command must be input to set the pointer back to region A when the pointer is pointing to region C.



To program region C only, set the start point to region C using the 50h command.

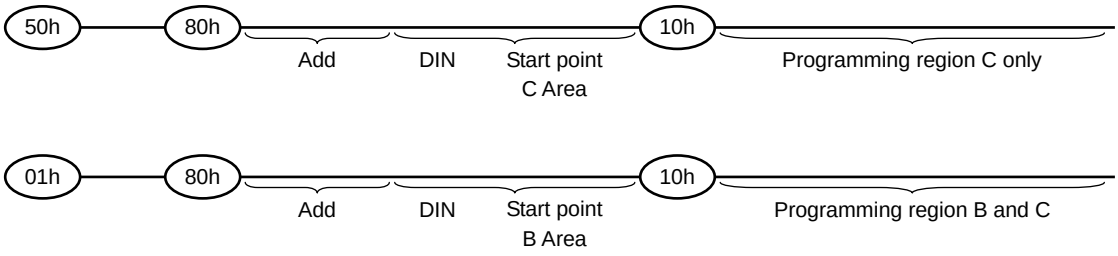


Figure 20. Example of How to Set the Pointer

(9) RY/$\overline{BY}$: termination for the Ready/Busy pin (RY/$\overline{BY}$)

A pull-up resistor needs to be used for termination because the RY/$\overline{BY}$ buffer consists of an open drain circuit.

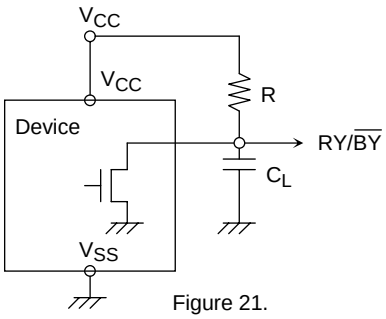
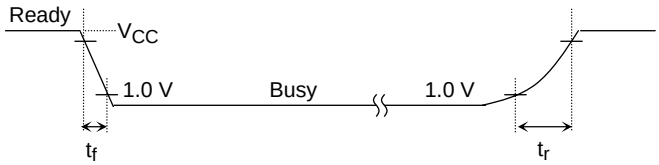
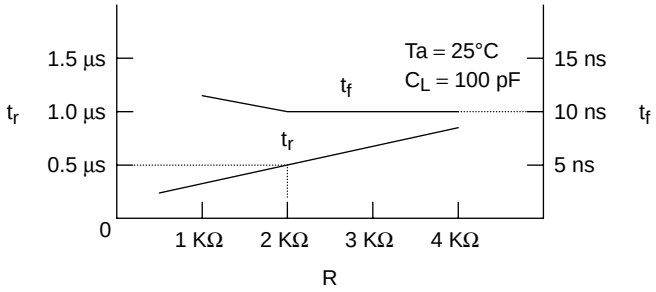


Figure 21.



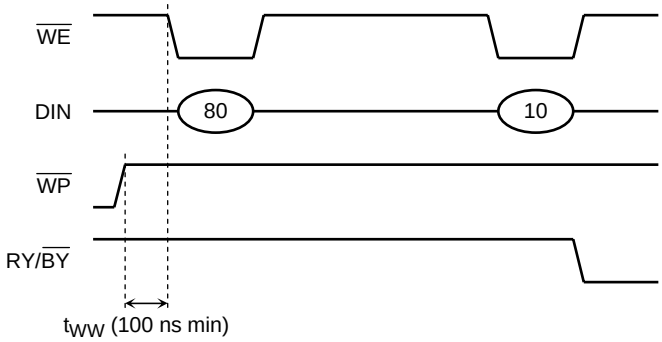


This data may vary from device to device.
We recommend that you use this data as a reference when selecting a resistor value.

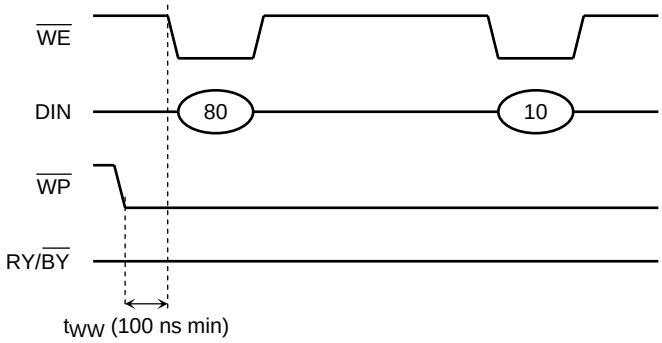
(10) Note regarding the $\overline{WP}$ signal

The Erase and Program operations are automatically reset when $\overline{WP}$ goes Low. The operations are enabled and disabled as follows:

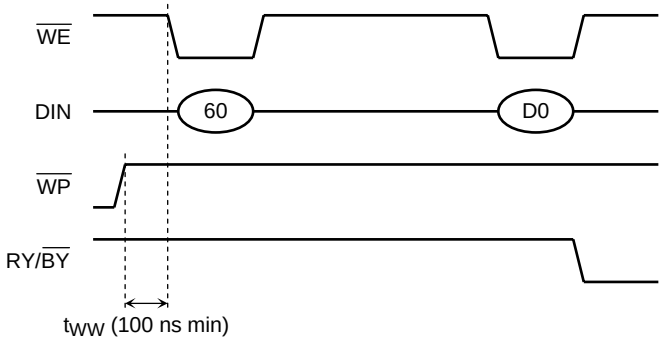
Enable Programming



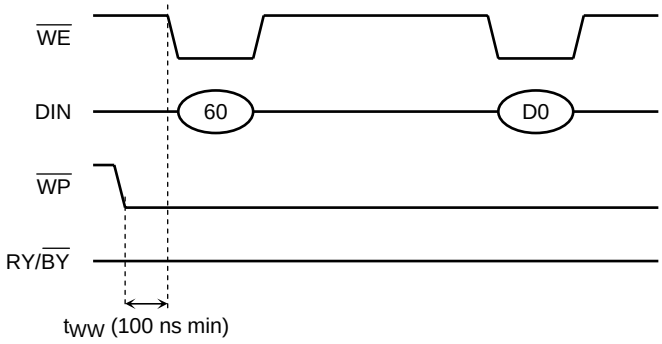
Disable Programming



Enable Erasing



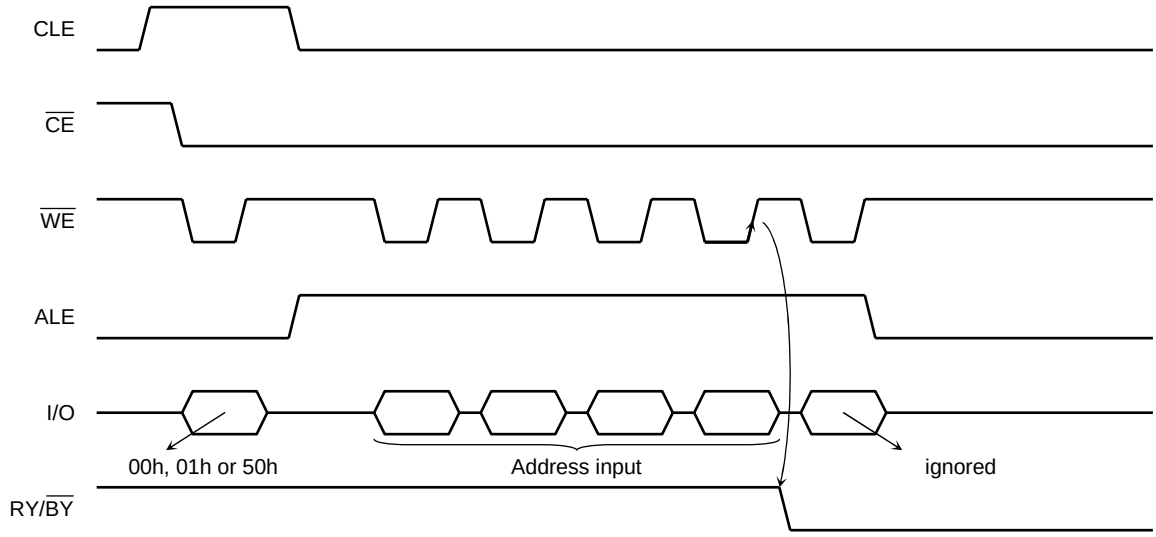
Disable Erasing



(11) When five address cycles are input

Although the device may read in a fifth address, it is ignored inside the chip.

Read operation



WE Internal read operation starts when WE goes High in the fourth cycle.

Figure 22.

Program operation

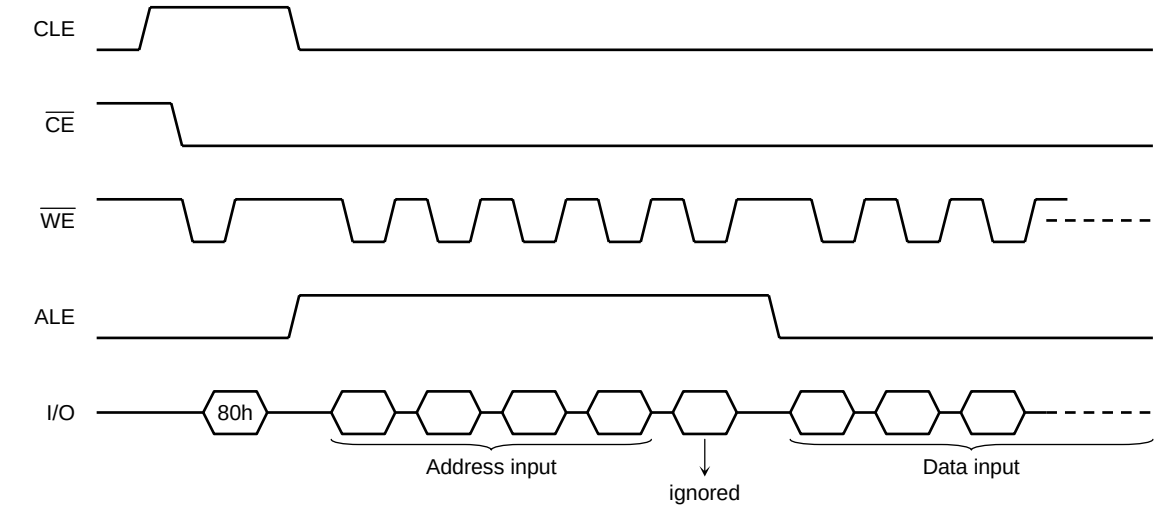


Figure 23.

(12) Several programming cycles on the same page (Partial Page Program)

A page can be divided into up to 3 segments. Each segment can be programmed individually as follows:

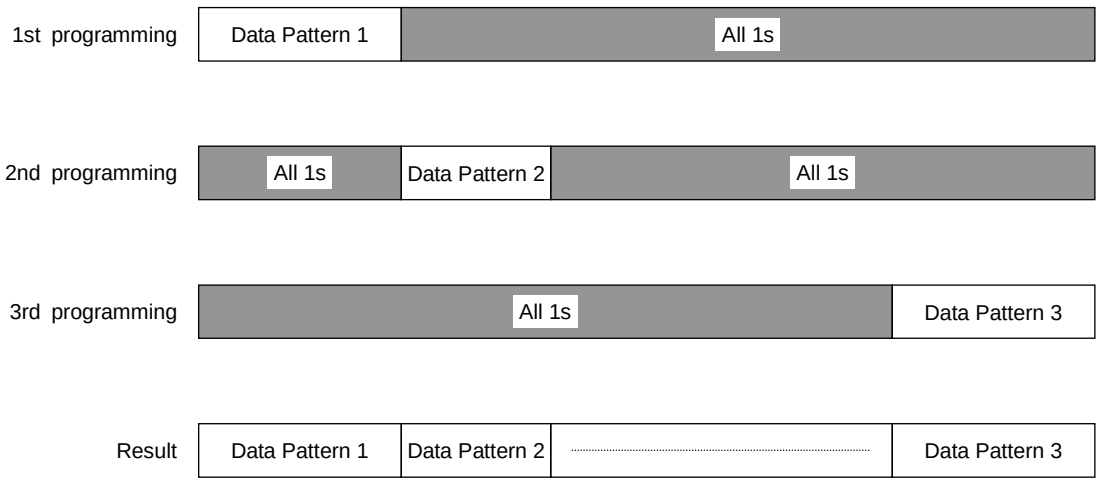


Figure 24.

Note: The input data for unprogrammed or previously programmed page segments must be “1”
(i.e. the inputs for all page bytes outside the segment which is to be programmed should be set to all “1”).

(13) Note regarding the $\overline{RE}$ signal

$\overline{RE}$ The internal column address counter is incremented synchronously with the $\overline{RE}$ clock in Read mode. Therefore, once the device has been set to Read mode by a “00h”, “01h” or “50h” command, the internal column address counter is incremented by the $\overline{RE}$ clock independently of the address input timing, If the $\overline{RE}$ clock input pulses start before the address input, and the pointer reaches the last column address, an internal read operation (array to register) will occur and the device will enter Busy state. (Refer to Figure 25.)

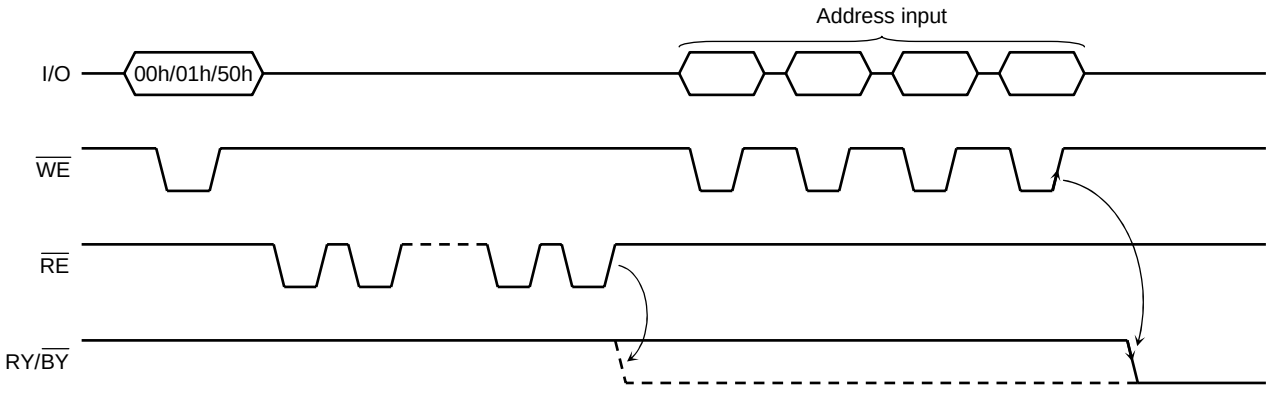


Figure 25.

Hence the $\overline{RE}$ clock input must start after the address input.

(14) Invalid blocks (bad blocks)

The device contains unusable blocks. Therefore, at the time of use, please check whether a block is bad and do not use these bad blocks.

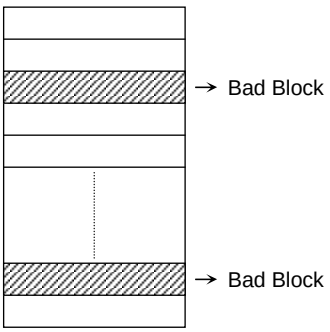


Figure 26.

At the time of shipment, all data bytes in a Valid Block are FFh. For Bad Block, all bytes are not in the FFh state. Please don't perform erase operation to Bad Block.

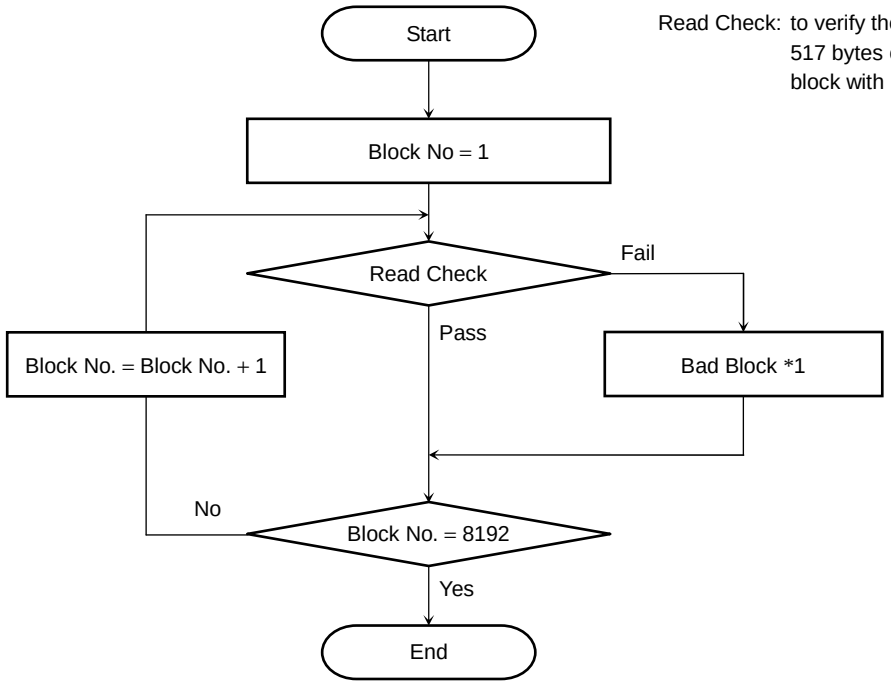
Check if the device has any bad blocks after installation into the system. Figure 27 shows the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

A bad block does not affect the performance of good blocks because it is isolated from the Bit line by the Select gate

The number of valid blocks at the time of shipment is as follows:

	MIN	TYP.	MAX	UNIT
Valid (Good) Block Number	8032	—	8192	Block

Bad Block Test Flow



Read Check: to verify the column address of 517 bytes of the first page in the block with FF (Hex)

*1: No erase operation is allowed to detected bad blocks

Figure 27

(15) Failure phenomena for Program and Erase operations

The device may fail during a Program or Erase operation.
The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Single Bit	Programming Failure 1 → 0	(1) Block Verify after Program → Retry
		(2) ECC

- ECC: Error Correction Code
- Block Replacement

Program

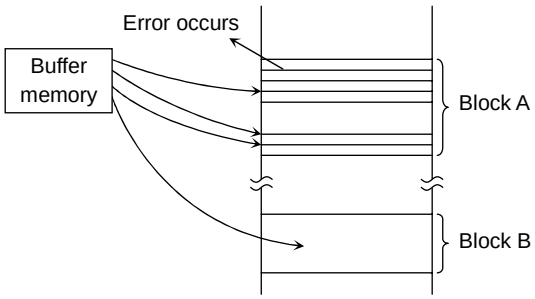


Figure 28.

When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using an another appropriate scheme).

Erase

When an error occurs in an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

(16) Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.