OV2610 Color CMOS UXGA (2.0 MPixel) CAMERACHIP™

General Description

The OV2610 CAMERACHIP™ is a high performance CMOS image sensor for digital still image and video/still camera products.

The device incorporates a 1600 x 1200 (UXGA) image array and an on-chip 10-bit A/D converter capable of operating at up to 10 frames per second (fps) with full resolution and 40 fps at SVGA (800 x 600) resolution. Proprietary sensor technology utilizes advanced algorithms to cancel Fixed Pattern Noise (FPN), and provides superior black level calibration for optimal color performance. The control registers allow for flexible control of timing, polarity, and CameraChip operation, which in turn allows the engineer a great deal of freedom in product design.

Features

- Optical black level calibration
- Video or snapshot operations
- Programmable/Auto Exposure and Gain Control
- Programmable/Auto White Balance Control
- Horizontal and vertical sub-sampling (4:2 and 4:2)
- Programmable image windowing
- Variable frame rate control
- On-chip R/G/B Channel and Luminance Average Counter
- Internal/External frame synchronization
- SCCB slave interface
- Power on reset and power down mode

Ordering Information

Product	Package
OV2610 (Color, UXGA, SVGA)	CLCC-48

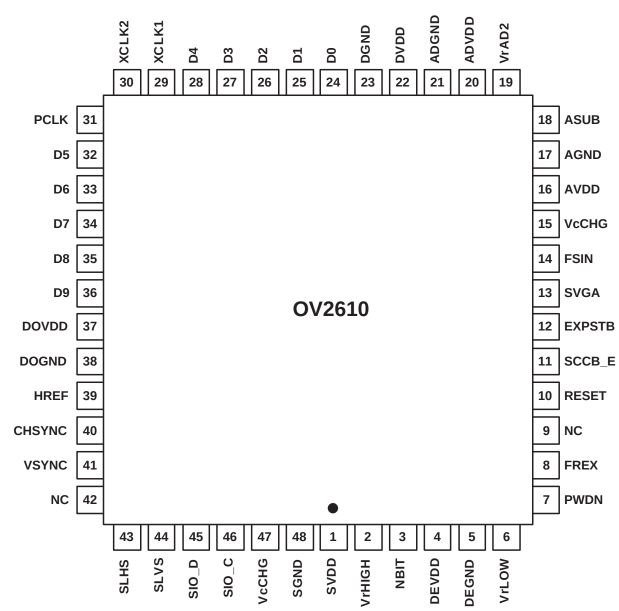
Applications

- Digital still cameras
- Video/Still camcorders

Key Specifications

Array Size	**UXGA**	1600 x 1200
	SVGA	800 x 600
Power Supply	**Core**	2.5 VDC ± 10%
	Analog	3.3 VDC ± 10%
	I/O	3.3 VDC ± 10%
Power Requirements	**Active**	< 50 mA
	Standby	< 10 µA
Electronics Exposure	**UXGA**	Up to 1230:1
	SVGA	Up to 614:1
Output Format		10-bit digital raw RGB data
Lens Size		1/2"
Maximum Image Transfer Rate	**UXGA**	10 fps
	SVGA	40 fps
Sensitivity		1.0 V/Lux-sec
S/N Ratio		54 dB
Dynamic Range		60 dB (due to ADC limitations)
Scan Mode		Progressive
Maximum Exposure Interval		1048 x t_{ROW}
Pixel Size		4.2 µm x 4.2 µm
Dark Current		28 mV/s
Fixed Pattern Noise		< 0.03% of $V_{PEAK-TO-PEAK}$
Image Area		6.72 mm x 5.04 mm
Package Dimensions		.560 in. x .560 in.

Figure 1 OV2610 Pin Diagram



Functional Description

Figure 2 shows the functional block diagram of the OV2610 image sensor. The OV2610 includes:

- Image Sensor Array (1632 x 1216 resolution)
- Analog Amplifier
  - Gain Control
- Channel Balance
  - Balance Control
- 10-Bit A/D Converter
- Black Level Compensation
- Timing Generator and Control Logic
  - Frame Exposure Mode Timing
  - Frame Rate Timing
  - Frame Rate Adjust
- SCCB Interface
- Channel Average Calculator

Figure 2 Functional Block Diagram

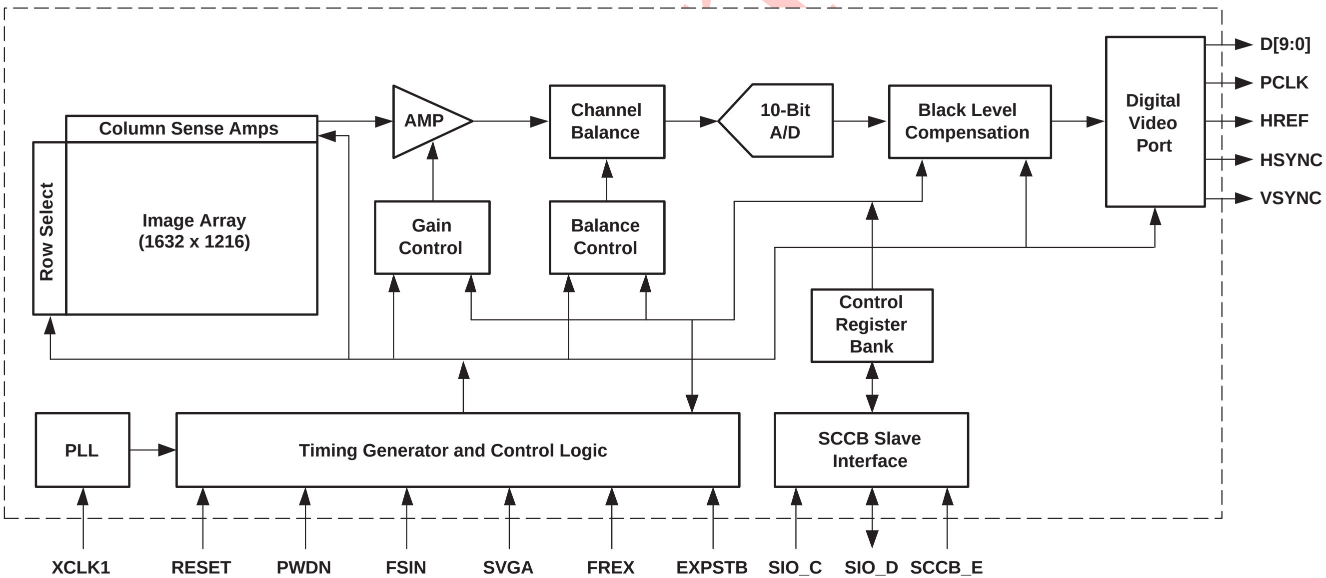
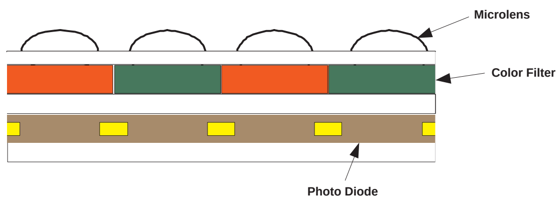


Image Sensor Array

The OV2610 sensor is a 1/2-inch CMOS imaging device. The sensor contains 1,984,512 pixels. However, the maximum output window size is 1618 columns by 1204 rows.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme. Figure 3 shows a cross-section of the image sensor array.

Figure 3 Image Sensor Array



Analog Amplifier

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier.

Gain Control

The amplifier gain can either be programmed by the user or controlled by the internal automatic gain control circuit (AGC).

Channel Balance

The amplified signals are then balanced with a channel balance block. In this block, the Red/Blue channel gain is increased or decreased to match Green channel luminance level. The adjustment range is ±54 dB.

Balance Control

Channel Balance can be done manually by the user or by the internal automatic white balance (AWB) controller.

10-Bit A/D Converter

The balanced signal is then digitized by the on-chip 10-bit ADC. It can operate at 12 MHz and is fully synchronous to the pixel clock. The actual conversion rate is determined by the frame rate.

Black Level Compensation

After the pixel data has been digitized, black level calibration can be applied before the data is output. The black level calibration block subtracts the average signal level of optical black pixels to compensate for the temperature and exposure time generated dark current in the pixel output. The user can disable black level calibration.

Timing Generator and Control Logic

In general, the timing generator controls the following:

- Frame Exposure Mode Timing
- Frame Rate Timing
- Frame Rate Adjust

Frame Exposure Mode Timing

The OV2610 supports frame exposure mode. Typically, the frame exposure mode must work with the aid of an external shutter.

The frame exposure pin, FREX (pin 8), is the frame exposure mode enable pin and the EXPSTB pin (pin 12) serves as the sensor's exposure start trigger. There are two ways to set Frame Exposure mode:

- Control both FREX and EXPSTB pins - Frame Exposure mode can be set by pulling both FREX and EXPSTB pins high at the same time (see Figure 13).
- Control FREX only and keep EXPSTB low - In this case, the pre-charge time is tline and sensor exposure time is the period after pre-charge until the shutter closes (see Figure 12).

When the external master device asserts the FREX pin high, the sensor array is quickly pre-charged and stays in reset mode until the EXPSTB pin is pulled low by the external master (sensor exposure time can be defined as the period between EXPSTB low to shutter close). After the FREX pin is pulled low, the video data stream is then clocked to the output port in a line-by-line manner. After completing one frame of data output, the OV2610 will output continuous live video data unless in single frame transfer mode. Figure 12, Figure 13, Figure 14, and Figure 15 show detailed timing of the Frame Exposure mode.

For frame exposure, register AEC (0x10) must be set to 0xFF and register GAIN (0x00) should be no larger than 0x10 (maximum 2x gain).

Frame Rate Timing

Default frame timing is illustrated in Figure 10 and Figure 11. Refer to Table 1 for the actual pixel rate at different frame rates.

Table 1 Frame and Pixel Rates

Frame Rate (fps)	10	5	2.5	1.25
PCLK (MHz)	24	12	6	3
NOTE: Based on 24 MHz external clock and internal PLL on, frame rate is adjusted by the main clock divide method.				

Frame Rate Adjust

The OV2610 offers three methods for frame rate adjustment:

- Clock prescaler:
  By changing the system clock divide ratio, the frame rate and pixel rate will change together.
- Line adjustment:
  By adding a dummy pixel timing in each line, the frame rate can be changed while leaving the pixel rate as is.
- Vertical sync adjustment:
  By adding dummy line periods to the vertical sync period, the frame rate can be altered while the pixel rate remains the same.

After changing registers COML (0x2A) and FRARL (0x2B) to adjust the dummy pixels, it is necessary to write to register COMH (0x12) or CLKRC (0x11) to reset the counter. Generally, OmniVision suggests users write to register COMH (0x12) (to change the sensor mode) as the last one. However, if you want to adjust the cropping window, it is necessary to write to those registers after changing register COMH (0x12). To use COMH to reset the counter, it is necessary to generate a pulse on resolution control register bit COMH[6].

SCCB Interface

The OV2610 provides an on-chip SCCB serial control port that allows access to all internal registers, for complete control and monitoring of OV2610 operation. Refer to *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

Slave Operation Mode

The OV2610 can be programmed to operate in slave mode (default is master mode).

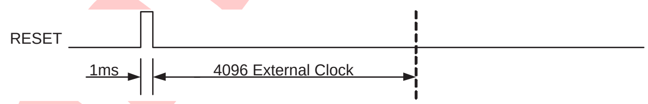
Channel Average Calculator

The OV2610 provides average output level data for the R/G/B channels along with frame-averaged luminance level. Access to the data is provided via the serial control port. Average values are calculated from 128 pixels per line (64 pixels per line in SVGA).

Reset

The RESET pin (pin 10) is active high. There is an internal pull-down (weak) resistor in the sensor so the default status of the RESET pin is low.

Figure 4 RESET Timing Diagram



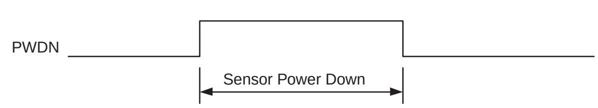
There are two ways for a sensor reset:

1. Hardware reset - Pulling the RESET pin high and keeping it high for at least 1 ms. As shown in Figure 4, after a reset has been initiated, the sensor will be most stable after the period shown as 4096 External Clock.
2. Software reset - Writing 0x80 to register 0x12 (see "COMH" on page 19) for a software reset. If a software reset is used, a reset operation done twice is recommended to make sure the sensor is stable and ready to access registers. When performing a software reset twice, the second reset should be initiated after the 4096 External Clock period as shown in Figure 4.

Power Down Mode

The PWDN pin (pin 7) is active high. There is an internal pull-down (weak) resistor in the sensor so the default status of the PWDN pin is low.

Figure 5 PWDN Timing Diagram



Two methods of power-down or standby operation are available with the OV2610.

- Hardware power-down may be selected by pulling the PWDN pin high (+3.3VDC). When this occurs, the OV2610 internal device clock is halted and all internal counters are reset. The current draw is less than 10 μA in this standby mode.

- Software power-down can be effected by setting the COMC[4] register bit high (see “COMC” on page 18). Standby current will be less then 1 mA when in software power-down.

Video Output

RGB Raw Data Output

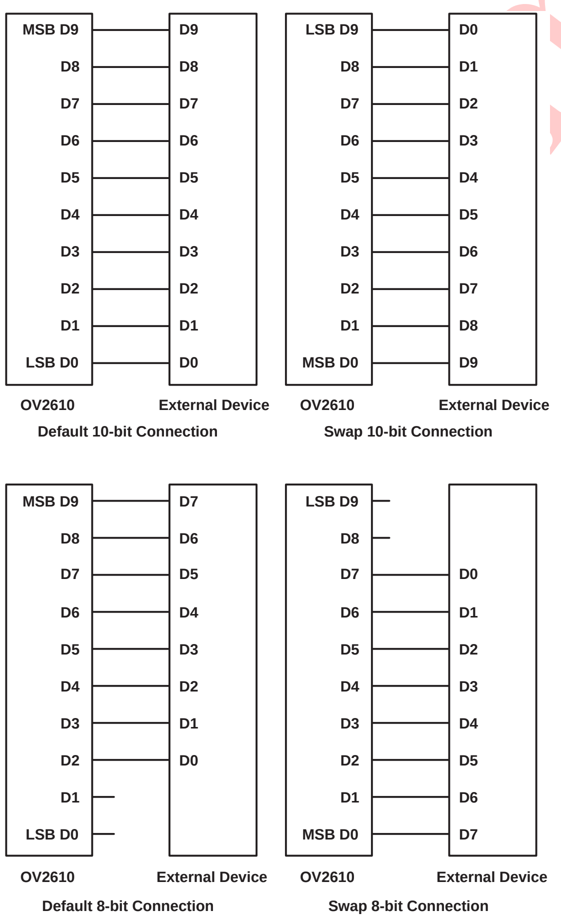
The OV2610 CAMERACHIP offers 10-bit RGB raw data output.

Digital Video Port

MSB/LSB Swap

OV2610 has a 10-bit digital video port. The MSB and LSB can be swapped with the control registers. Figure 6 shows some examples of connections with external devices.

Figure 6 Connection Examples



Line/Pixel Timing

The OV2610 digital video port can be programmed to work in either master or slave mode.

Pixel Output Pattern

Table 2 shows the output data order from the OV2610. The data output sequence following the first HREF and after VSYNC is: $B_{0,0}$ $G_{0,1}$ $B_{0,2}$ $G_{0,3}$… $B_{0,1598}$ $G_{0,1599}$. After the second HREF, the output is $G_{1,0}$ $R_{1,1}$ $G_{1,2}$ $R_{1,3}$… $G_{1,1598}$ $R_{1,1599}$…, etc. If the OV2610 is programmed to output SVGA resolution data, horizontal and vertical sub-sampling will occur. The default output sequence for the first line of output will be: $B_{0,0}$ $G_{0,1}$ $B_{0,4}$ $G_{0,5}$… $B_{0,1596}$ $G_{0,1597}$. The second line of output will be: $G_{1,0}$ $R_{1,1}$ $G_{1,4}$ $R_{1,5}$… $G_{1,1596}$ $R_{1,1597}$.

Table 2 Data Pattern

R/C	0	1	2	3	. . .	1598	1599
0	$B_{0,0}$	$G_{0,1}$	$B_{0,2}$	$G_{0,3}$	. . .	$B_{0,1598}$	$G_{0,1599}$
1	$G_{1,0}$	$R_{1,1}$	$G_{1,2}$	$R_{1,3}$	. . .	$G_{1,1598}$	$R_{1,1599}$
2	$B_{2,0}$	G_2	$B_{2,2}$	$G_{2,3}$	. . .	$B_{2,1598}$	$G_{2,1599}$
3	$G_{3,0}$	$R_{3,1}$	$G_{3,2}$	$R_{3,3}$	. . .	$G_{3,1598}$	$R_{3,1599}$
. .					. .		
1198	$B_{1198,0}$	$G_{1198,1}$	$B_{1198,2}$	$G_{1198,3}$		$B_{1198,1598}$	$G_{1198,1599}$
1199	$G_{1199,0}$	$R_{1199,1}$	$G_{1199,2}$	$R_{1199,3}$		$G_{1199,1598}$	$R_{1199,1599}$

Note that after writing to register COMH (0x12) to change the sensor mode, registers related to the sensor’s cropping window will be reset back to its default value.

Pin Description

Table 3 Pin Description

Pin Number	Name	Pin Type	Function/Description
01	SVDD	Power	3.3 V supply for the pixel array
02	VrHIGH	Analog	Sensor reference 1 - connect to ground using a 0.1 µF capacitor
03	NBIT	Analog	Sensor reference 2 - connect to ground using a 0.1 µF capacitor
04	DEVDD	Power	3.3 V supply for the sensor array decoder
05	DEGND	Power	Ground for sensor array decoder
06	VrLOW	Analog	Sensor reference 3 - connect to ground using a 0.1 µF capacitor
07	PWDN	Input (0)[a]	Power down mode enable, active high
08	FREX	Input (0)	Snapshot trigger - use to activate a snapshot sequence
09	NC	—	No connection
10	RESET	Input (0)	Chip reset, active high
11	SCCB_E	Input (0)	SCCB interface enable signal, active low
12	EXPSTB	Input (0)	Snapshot Exposure Start Trigger 0: Sensor starts exposure (only effective in snapshot mode) 1: Sensor stays in reset mode
13	SVGA	Input (0)	Sensor Resolution Selection 0: UXGA resolution (1600 x 1200) 1: SVGA resolution (800 x 600)
14	FSIN	Input (0)	Frame synchronization input
15	VcCHG	Analog	Sensor reference 4 - bypass to ground using a 0.1 µF capacitor (short internally with pin 47, see “VcCHG” on page 7)
16	AVDD	Power	3.3 V supply for analog circuits
17	AGND	Power	Analog ground
18	ASUB	Power	Analog ground (substrate)
19	VrAD2	Analog	A/D converter reference - bypass to ground using a 0.1 µF capacitor
20	ADVDD	Power	3.3 V supply for A/D converter
21	ADGND	Power	A/D converter ground
22	DVDD	Power	2.5 V supply for digital circuits
23	DGND	Power	Digital ground
24	D0	Output	Video port output bit[0]
25	D1	Output	Video port output bit[1]
26	D2	Output	Video port output bit[2]
27	D3	Output	Video port output bit[3]
28	D4	Output	Video port output bit[4]

Table 3 Pin Description (Continued)

Pin Number	Name	Pin Type	Function/Description
29	XCLK1	Input	Crystal clock input
30	XCLK2	Output	Crystal clock output
31	PCLK	Output	Pixel clock output
32	D5	Output	Video port output bit[5]
33	D6	Output	Video port output bit[6]
34	D7	Output	Video port output bit[7]
35	D8	Output	Video port output bit[8]
36	D9	Output	Video port output bit[9]
37	DOVDD	Power	3.3 V supply for digital video port
38	DOGND	Power	Digital video port ground
39	HREF	Output	Horizontal reference output
40	CHSYNC	Output	Horizontal synchronization output when chip is in master mode.
41	VSYNC	Output	Vertical synchronization output when chip is in master mode.
42	NC	—	No connection
43	SLHS	Input (0)	Slave mode horizontal synchronization input, active high
44	SLVS	Input (0)	Slave mode vertical synchronization input, active high
45	SIO_D	I/O	SCCB serial interface data I/O
46	SIO_C	Input	SCCB serial interface clock input
47	VcCHG	Analog	Sensor reference 4 - bypass to ground using a 0.1 µF capacitor (short internally with pin 15, see "VcCHG" on page 6)
48	SGND	Power	Pixel array ground

a. Input (0) represents an internal pull-down low resistor.

Electrical Characteristics

Table 4 Operating Conditions

Parameter	Min	Max	Unit
Operating temperature	0	40	°C
Storage temperature	-40	125	°C
Operating humidity	TBD	TBD	
Storage humidity	TBD	TBD	

Table 5 DC Characteristics (0°C < T_A < 85°C, Voltages referenced to GND)

Symbol	Parameter	Min	Typ	Max	Unit
Supply					
V_{DD-A}	Supply voltage (DEVDD, ADVDD, AVDD, SVDD)	3.0	3.3	3.6	V
V_{DD-IO}	Supply voltage (DOVDD)	3.0	3.3	3.6	V
V_{DD-C}	Supply voltage (DVDD)	2.25	2.5	2.75	V
I_{DD1}	Supply current (UXGA at 10 Hz frame rate and 3.3 V digital I/O with 25 pF plus 1 TTL loading on 10-bit data bus)			60	mA
I_{DD2}	Supply current (V_{DD} = 3 V at 15 Hz frame rate without digital I/O loading)		40		mA
Digital Inputs					
V_{IL}	Input voltage LOW			0.8	V
V_{IH}	Input voltage HIGH	2			V
C_{IN}	Input capacitor			10	pF
Digital Outputs (standard loading 25 pF, 1.2 KΩ to 3 V)					
V_{OH}	Output voltage HIGH	2.4			V
V_{OL}	Output voltage LOW			0.6	V
SCCB Inputs					
V_{IL}	SIO_C and SIO_D	-0.5	0	1	V
V_{IH}	SIO_C and SIO_D	2.5	3.3	V_{DD} + 0.5	V

Table 6 AC Characteristics (T_A = 25°C, V_{DD} = 3V)

Symbol	Parameter	Min	Typ	Max	Unit
ADC Parameters					
B	Analog bandwidth		12		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	Settling time for hardware reset			<1	ms
	Settling time for software reset			<1	ms
	Settling time for SVGA/UXGA mode change			<1	ms
	Settling time for register setting			<300	ms

Table 7 Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Oscillator and Clock Input					
f_{OSC}	Frequency (XCLK1, XCLK2)	8	24	48	MHz
t_r, t_f	Clock input rise/fall time			2	ns
	Clock input duty cycle	45	50	55	%

Timing Specifications

Figure 7 SCCB Timing Diagram

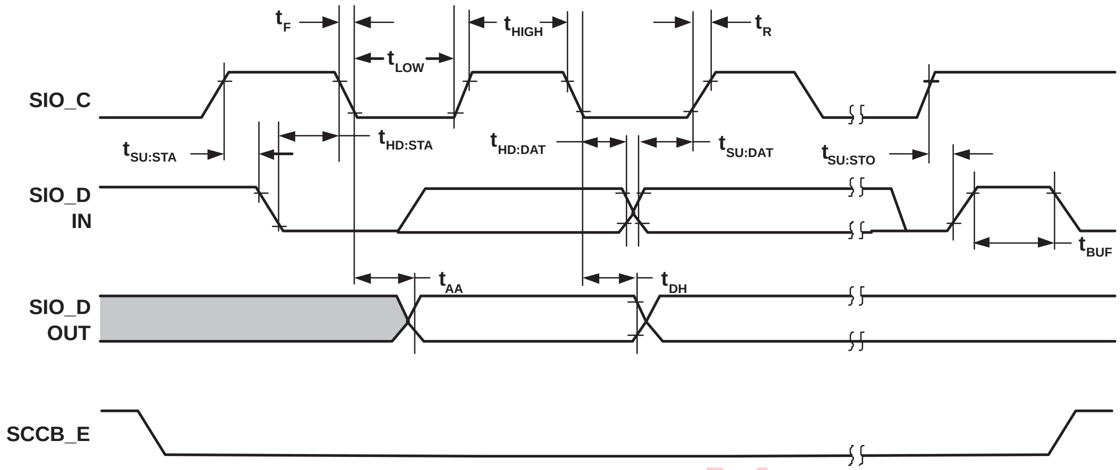


Table 8 SCCB Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{SIO_C}	Clock Frequency			400	KHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_{AA}	SIO_C low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			µs
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
t_R, t_F	SCCB Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns

Figure 8 UXGA Line/Pixel Output Timing

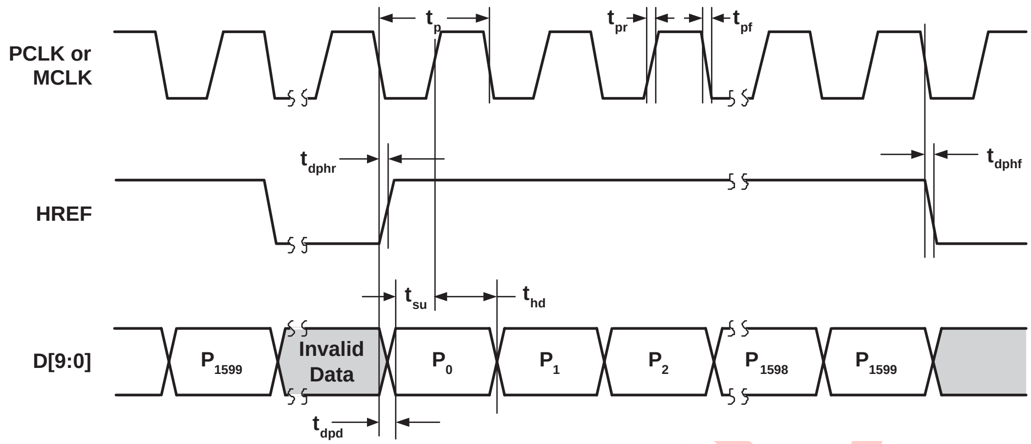


Figure 9 SVGA Line/Pixel Output Timing

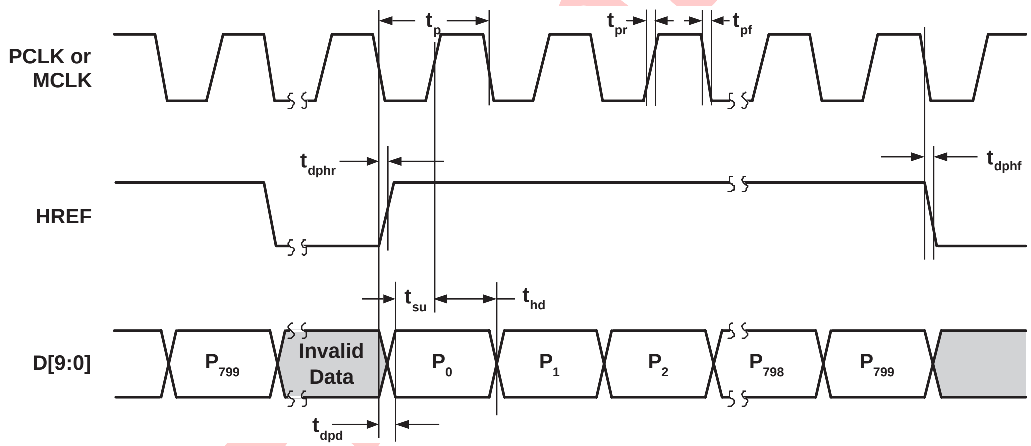


Figure 10 UXGA Frame Timing

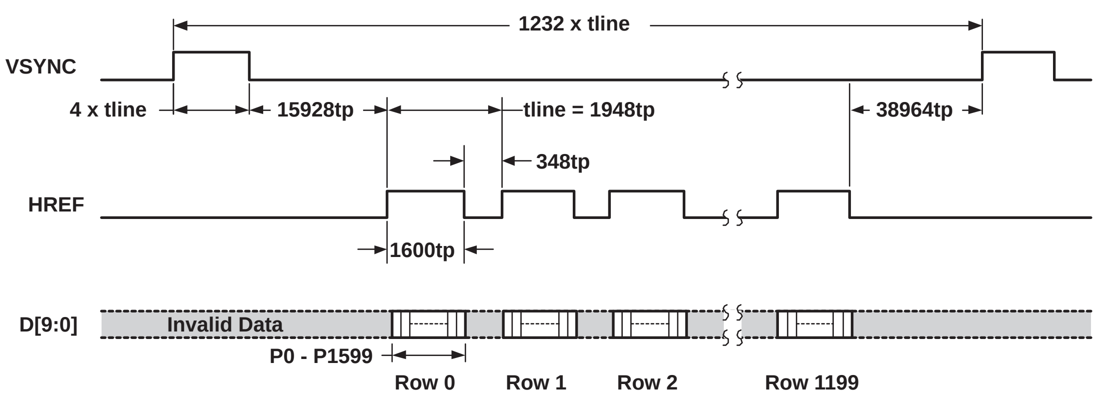


Figure 11 SVGA Frame Timing

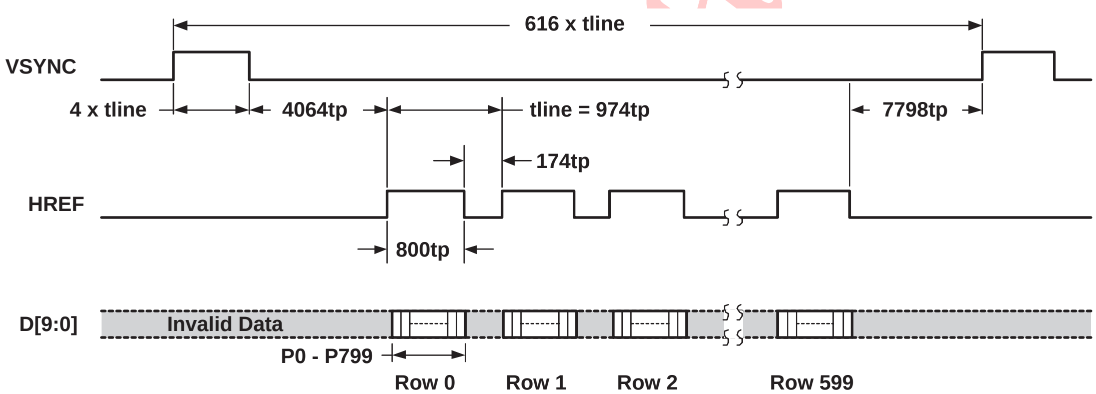


Table 9 Pixel Timing Specification

Symbol	Parameter	Min	Typ	Max	Unit
t_p	PCLK period		41.67		ns
t_{pr}	PCLK rising time		10		ns
t_{pf}	PCLK falling time		5		ns
t_{dphr}	PCLK negative edge to HREF rising edge	0		5	ns
t_{dphf}	PCLK negative edge to HREF negative edge	0		5	ns
t_{dpd}	PCLK negative edge to data output delay	0		5	ns
t_{su}	Data bus setup time	15			ns
t_{hd}	Data bus hold time	8			ns

Figure 12 Frame Exposure Mode Timing with EXPSTB Staying Low

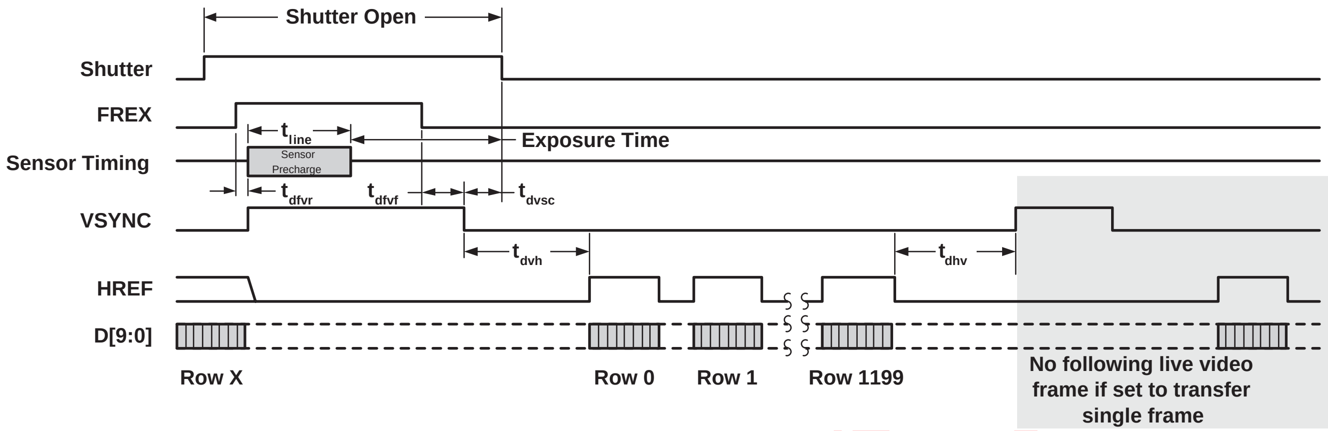


Figure 13 Frame Exposure Mode Timing with EXPSTB Asserted

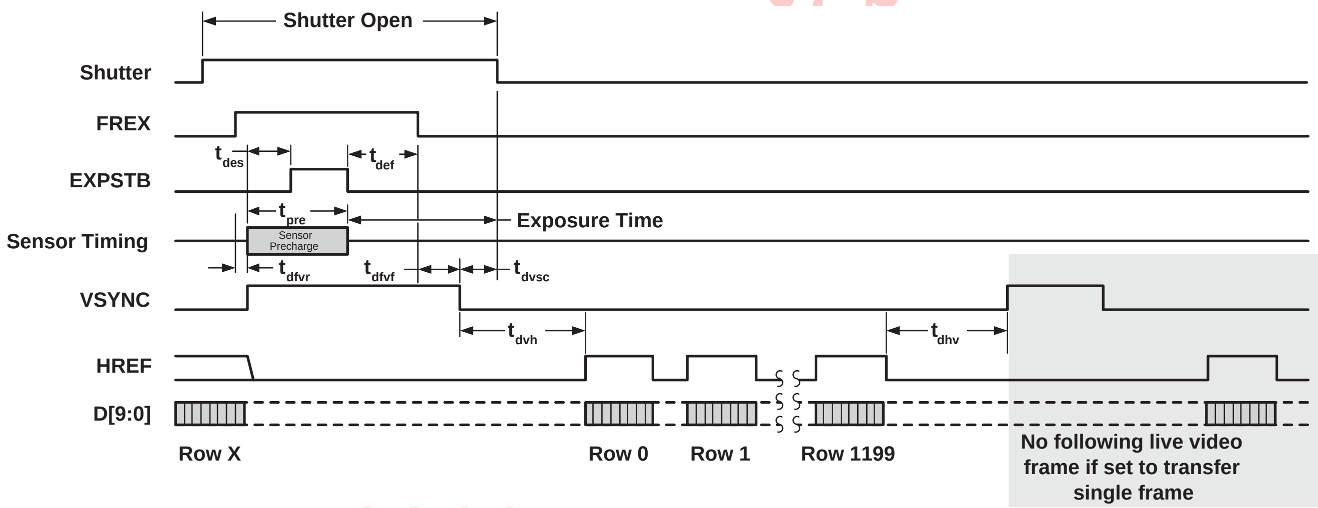


Table 10 Frame Exposure Timing Specifications

Symbol	Min	Typ	Max	Unit
tline		1948 (UXGA)		tp
		974 (SVGA)		tp
tvs		4		tline
tdfvr	8		9	tp
tdfvf			4	tline
tdvsc			2	tline
tdhv		38964 (UXGA)		tp
		7798 (SVGA)		tp
tdvh		15928 (UXGA)		tp
		4064 (SVGA)		tp
tdhso	0			ns
tdef	20			tp
tdes			1900 (UXGA)	tp
			900 (SVGA)	tp

NOTE 1) FREX must stay high long enough to ensure the entire sensor has been reset.
2) Shutter must be closed no later then 3896 tp (1948 tp for SVGA) after VSYNC falling edge.

Figure 14 Frame Exposure Mode Control Timing (UXGA Mode)

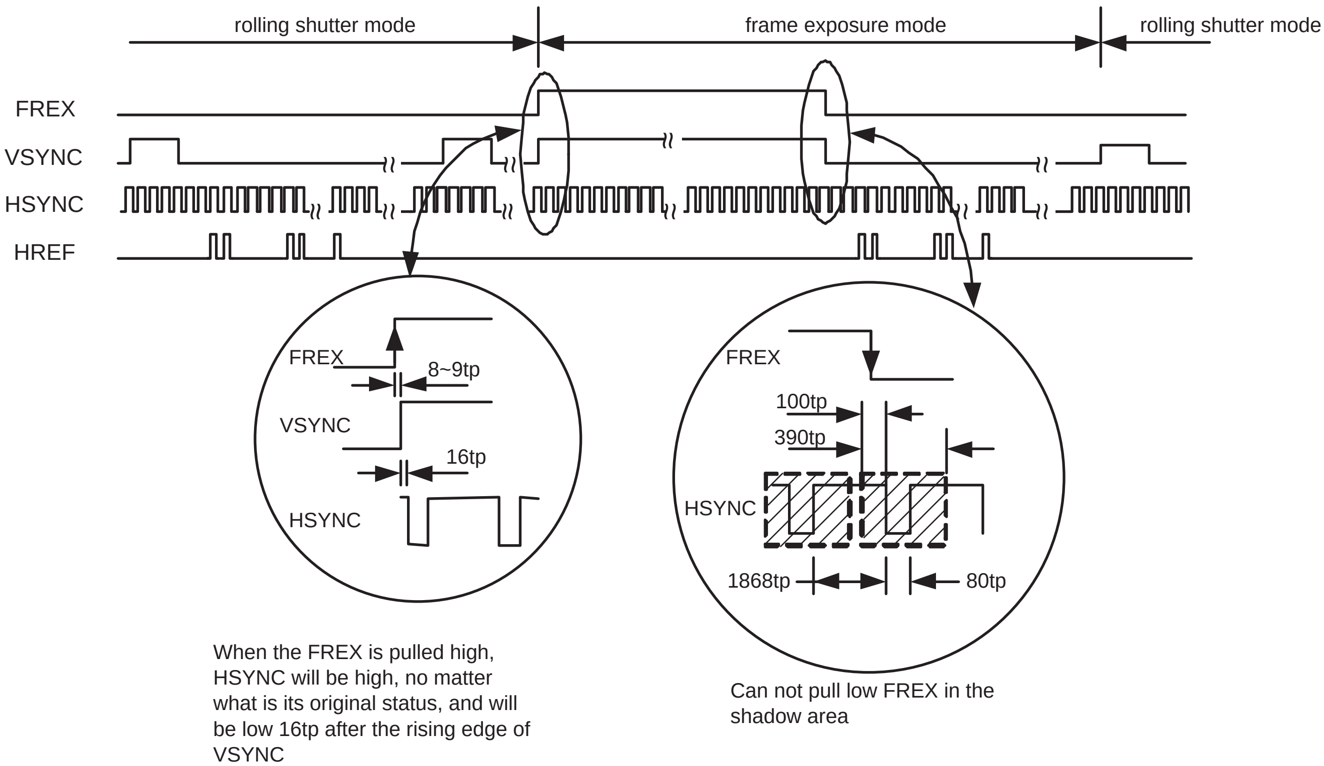
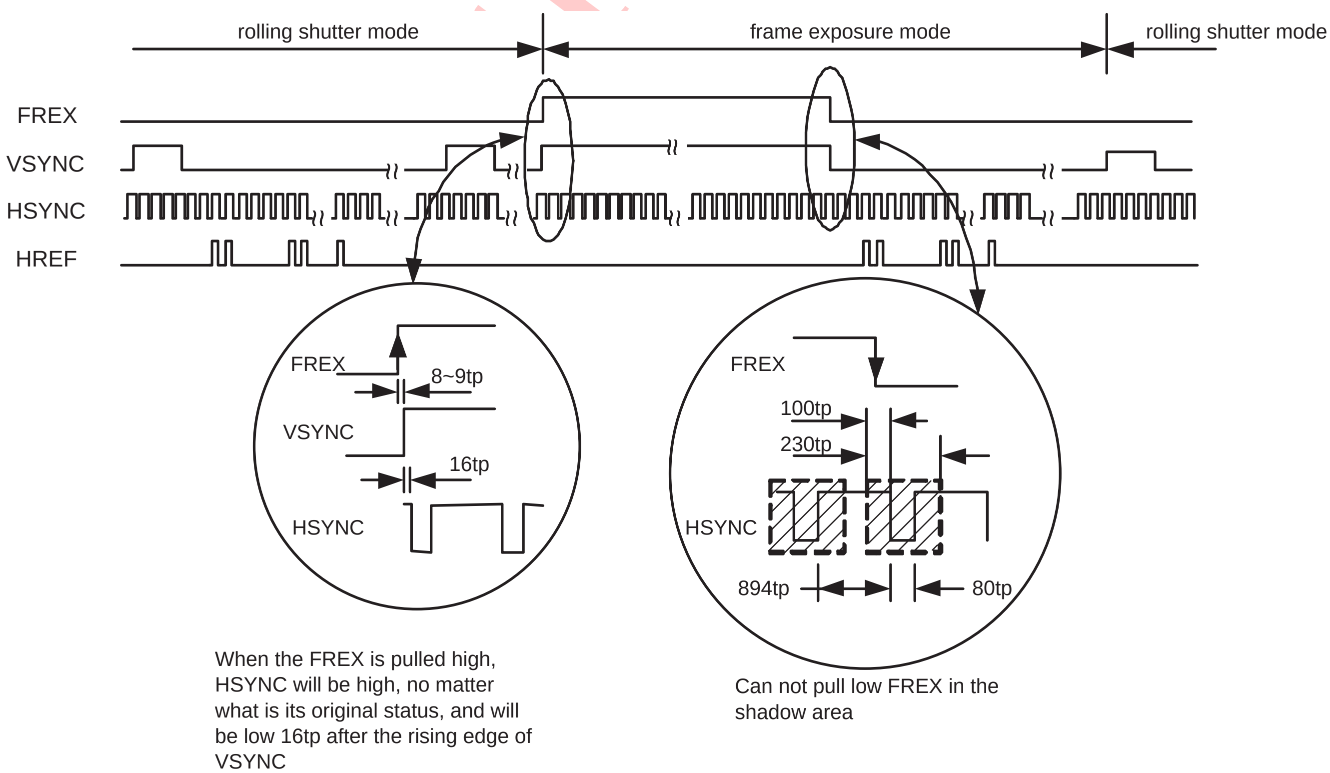
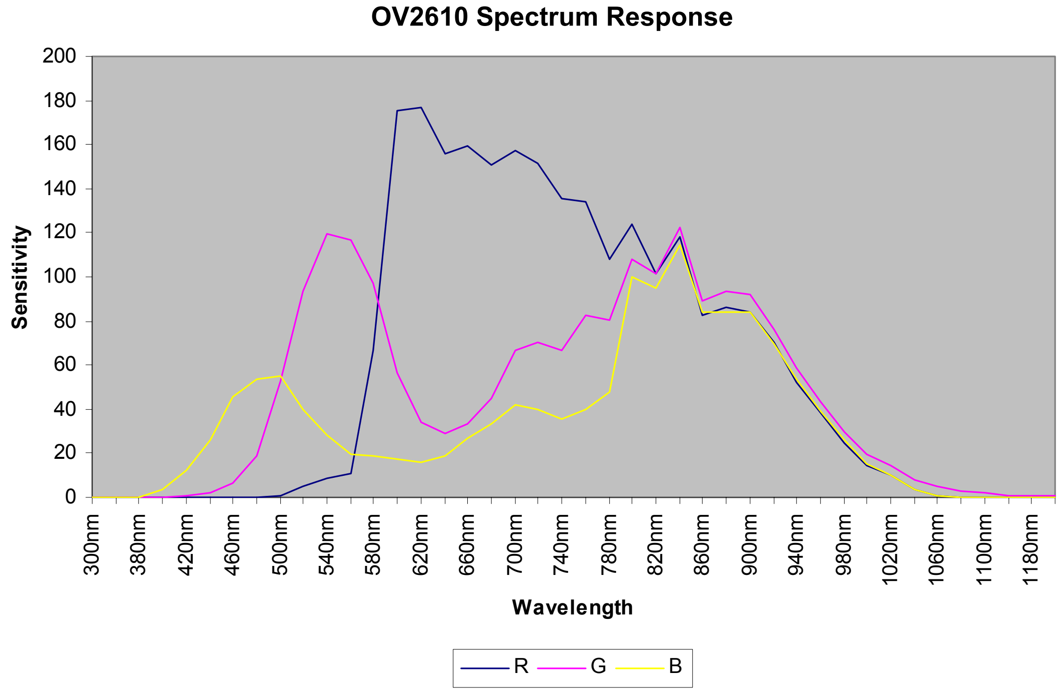


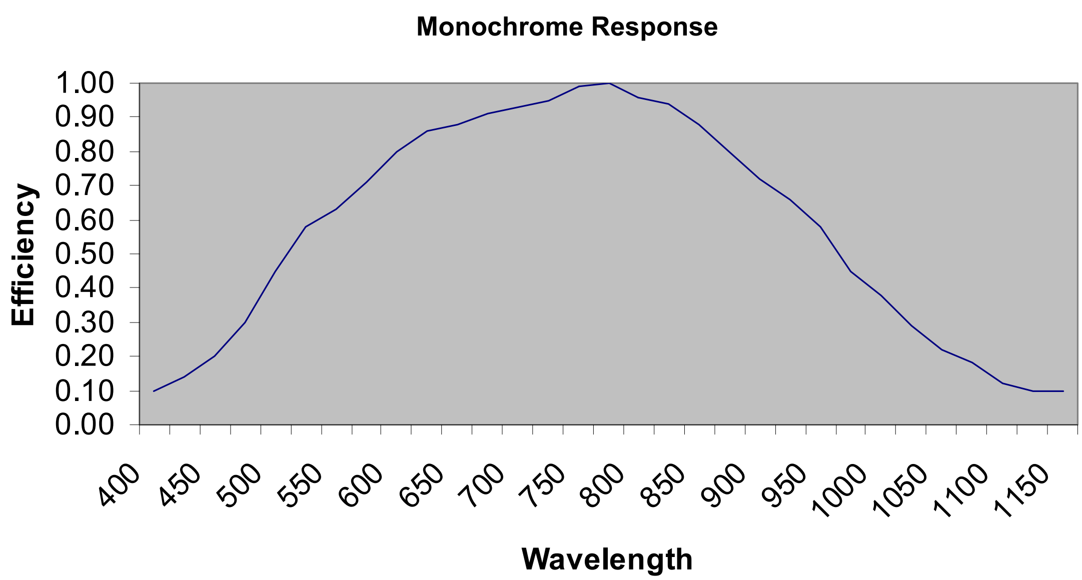
Figure 15 Frame Exposure Mode Control Timing (SVGA Mode)



OV2610 Light Response

Figure 16 OV2610 Light Response





Register Set

Table 11 provides a list and description of the Device Control registers contained in the OV2610. The device slave addresses for the OV2610 are 60 for write and 61 for read.

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC Gain control setting Bit[7:6]: Reserved Bit[5:0]: Gain control gain setting • Range: 1x to 8x Gain = (Bit[5]+1) x (Bit[4]+1) x (1+Bit[3:0]/16) ***Note:** Set COMI[0] = 0 to disable AGC.*
01	BLUE	80	RW	Blue gain control MSB, 8 bits (LSB 2 bits in COMA[3:2] - see "COMA" on page 17). • Range: 1/5x to 5x If BLUE[9] = 1, then Blue gain = 1 + BLUE[8:0]/128 If BLUE[9] = 0, then Blue gain = 1/(1 + BLUE_B[8:0]/128), where BLUE_B[8:0] is the bit reverse of BLUE[8:0].
02	RED	80	RW	Red gain control MSB, 8 bits (LSB 2 bits in COMA[1:0] - see "COMA" on page 17). • Range: 1/5x to 5x If RED[9] = 1, then Red gain = 1 + RED[8:0]/128 If RED[9] = 0, then Red gain = 1/(1 + RED_B[8:0]/128), where RED_B[8:0] is the bit reverse of RED[8:0].
03	COMA	40	RW	Common Control A Bit[7:4]: AWB update threshold Bit[3:2]: BLUE channel lower 2 bits of Blue gain control Bit[1:0]: RED channel lower 2 bits of Blue gain control
04	COMB	00	RW	Common Control B Bit[7:6]: AWB Step Selection 00: 1023 steps 01: 255 steps 10: 511 steps 11: 255 steps Bit[5:4]: AWB Update Speed Selection 00: Slow 01: Slowest 10: Fast 11: Fast Bit[3]: Reserved Bit[2:0]: AEC lower 3 bits – AEC[2:0]
05	BAVG	00	RW	B Channel Average
06	GbAVG	00	RW	G Channel Average - Picked G pixels in the same line with B pixels.
07	GrAVG	00	RW	G Channel Average - Picked G pixels in the same line with R pixels.

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
08	RAVG	00	RW	R Channel Average
09	COMC	0C	RW	Common Control C Bit[7:5]: Reserved Bit[4]: Sleep Mode Enable 0: Normal mode 1: Sleep mode Bit[3:2]: Sensor Sampling Reset Timing Selection 00: Normal reset time 01: Long reset time 10: Longer reset time 11: Longest reset time Bit[1:0]: Output Drive Select 00: Weakest 01: Double capability 10: Double capability 11: Triple drive current
0A	PIDH	96	R	Product ID Number MSB (Read only)
0B	PIDL	40	R	Product ID Number LSB (Read only)
0C	COMD	28	RW	Common Control D Bit[7]: Reserved Bit[6]: Swap MSB and LSB at the output port Bit[5:2]: Reserved Bit[1]: Sensor precharge voltage selection 0: Selects internal reference as precharge voltage 1: Selects SVDD as precharge voltage Bit[0]: Snapshot option 0: Enable live video output after snapshot sequence 1: Output single frame only
0D-0F	RSVD	XX	–	Reserved
10	AEC	43	RW	Automatic Exposure Control Most Significant 8 bits for AEC[10:3] (least significant 3 bits in register COMB[2:0] - see "COMB" on page 17). Bit[10:0]: Exposure time $T_{EX} = t_{LINE} \times AEC[10:0]$ ***Note:*** *Set COMI[2] to 0 to disable the AEC.*

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
11	CLKRC	00	RW	Clock Rate Control Bit[7]: Internal PLL ON/OFF selection 0: PLL disabled 1: PLL enabled Bit[6]: Digital video port master/slave selection 0: Master mode, sensor provides PCLK 1: Slave mode, external PCLK input from XCLK1 pin Bit[5:0]: Clock divider CLK = XCLK1/(decimal value of CLKRC[5:0] + 1)
12	COMH	20	RW	Common Control H Bit[7]: SRST 1: Initiates soft reset. All register are set to factory default values after which the chip resumes normal operation Bit[6]: Resolution selection 0: UXGA 1: SVGA Bit[5]: Average luminance value pixel counter ON/OFF 0: OFF 1: ON Bit[4]: Reserved Bit[3]: Master/slave selection 0: Master mode 1: Slave mode Bit[2]: Window output selection 0: Output only pixels defined by window registers 1: Output all pixels Bit[1]: Color bar test pattern 0: OFF 1: ON Bit[0]: ADC mode selection 0: 2 channel ADC 1: 4 channel ADC

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
13	COMI	C7	RW	Common Control I Bit[7]: AEC speed selection 0: Normal 1: Faster AEC correction Bit[6]: AEC speed/step selection 0: Small steps, slow 1: Big steps, fast Bit[5]: Banding filter ON/OFF 0: OFF 1: ON, set minimum exposure to 1/120s Bit[4]: Banding filter option 0: Set to 0, if system clock is 48 MHz and the PLL is ON. 1: Set to 1, if system clock is 24 MHz and the PLL is ON or if the system clock is 48 MHz and the PLL is OFF. Bit[3]: Reserved Bit[2]: AGC auto/manual control selection 0: Manual 1: Auto Bit[1]: AWB auto/manual control selection 0: Manual 1: Auto Bit[0]: Exposure control 0: Manual 1: Auto
14-18	RSVD	XX	–	Reserved
19	VSTRT	01	RW	Vertical Window line start most significant 8 bits, LSB in COMM register (see “COMM” on page 21). Bit[8:0]: Selects the start of the vertical window, each LSB represents four scan lines in UXGA or two scan lines in SVGA. ***Note:*** *VSTRT[8:0] should be less than VEND[8:0].*
1A	VEND	97	RW	Vertical Window line end most significant 8 bits, LSB in COMM register (see “COMM” on page 21). Bit[8:0]: Selects the end of the vertical window, each LSB represents four scan lines in UXGA and two scan lines in SVGA. ***Note:*** *VEND[8:0] should be larger than VSTRT[8:0]. The adjustment range for the vertical window size is from [01] to [12F].*
1B-29	RSVD	XX	–	Reserved

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
2A	COML	00	RW	Common Control L Bit[7]: Line interval adjustment. Interval adjustment value is in COML[6:5] and FRARL[7:0] (see "FRARL" on page 21). 0: Disabled 1: Enabled Bit[6:5]: Line interval adjust value MSB 2 bits Bit[4]: Reserved Bit[3:2]: HSYNC timing end point adjustment MSB 2 bits Bit[1:0]: HSYNC timing start point adjustment MSB 2 bits
2B	FRARL	00	RW	Line Interval Adjustment Value LSB 8 bits The frame rate will be adjusted by changing the line interval. Each LSB will add 2/1948 T_{frame} in UXGA and 2/974 T_{frame} in SVGA mode to the frame period.
2C	RSVD	XX	–	Reserved
2D	ADDVSL	00	RW	VSYNC Pulse Width LSB 8 bits Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x t_{line}. Each LSB count will add 1 x t_{line} to the VSYNC active period.
2E	ADDVSH	00	RW	VSYNC Pulse width MSB 8 bits Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x t_{line}. Each MSB count will add 256 x t_{line} to the VSYNC active period.
2F	YAVG	00	RW	Luminance Average This register will auto update when COMH[5] = 1 (see "COMH" on page 19). Average Luminance is calculated from the B/Gb/Gr/R channel average as follows: B/Gb/Gr/R channel average = (BAVG[7:0] + GbAVG[7:0] + GrAVG[7:0] +RAVG[7:0])/4
30-31	RSVD	XX	–	Reserved
32	COMM	00 (0Fin SVGA)	RW	Common Control M Bit[7]: Pixel blanking period 1: Set pixel blanking to 040 to each side of HREF Bit[6]: Blank pixel value setting 1: Set pixel blanking to 010 periods to each side of HREF. Default pixel blanking is 0. Bit[5]: Vertical window end position LSB Bit[4]: Vertical window start position LSB Bit[3:2]: Horizontal window end position LSBs Bit[1:0]: Horizontal window start position LSBs
33-3D	RSVD	XX	–	Reserved

NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.

Package Specifications

The OV2610 uses a 48-pin ceramic package. Refer to Figure 17 for package information and Figure 18 for the array center on the chip.

Figure 17 OV2610 Package Specifications

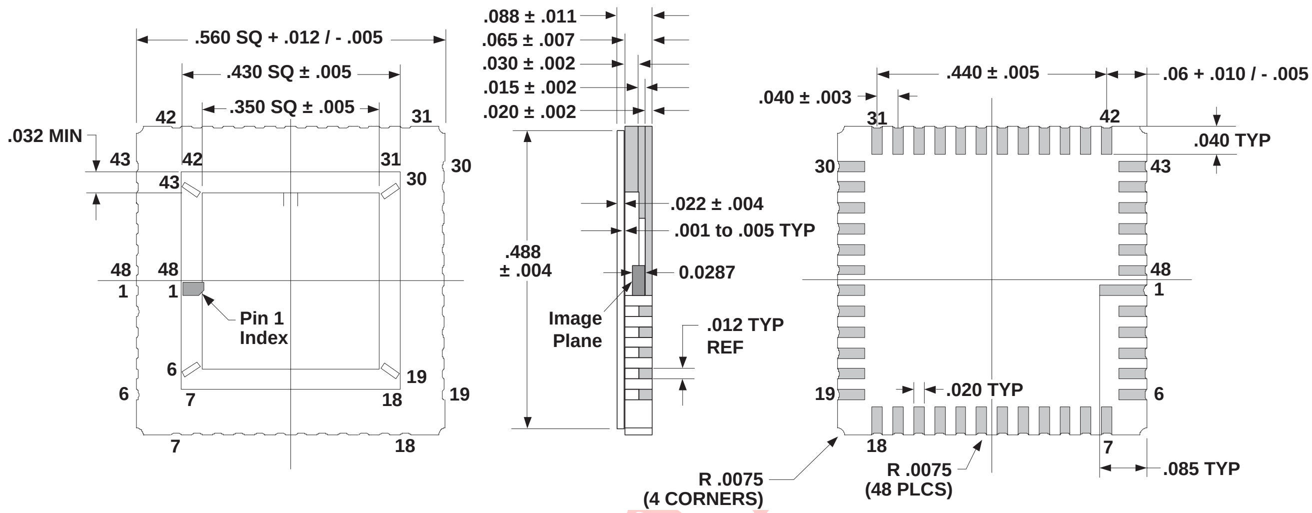
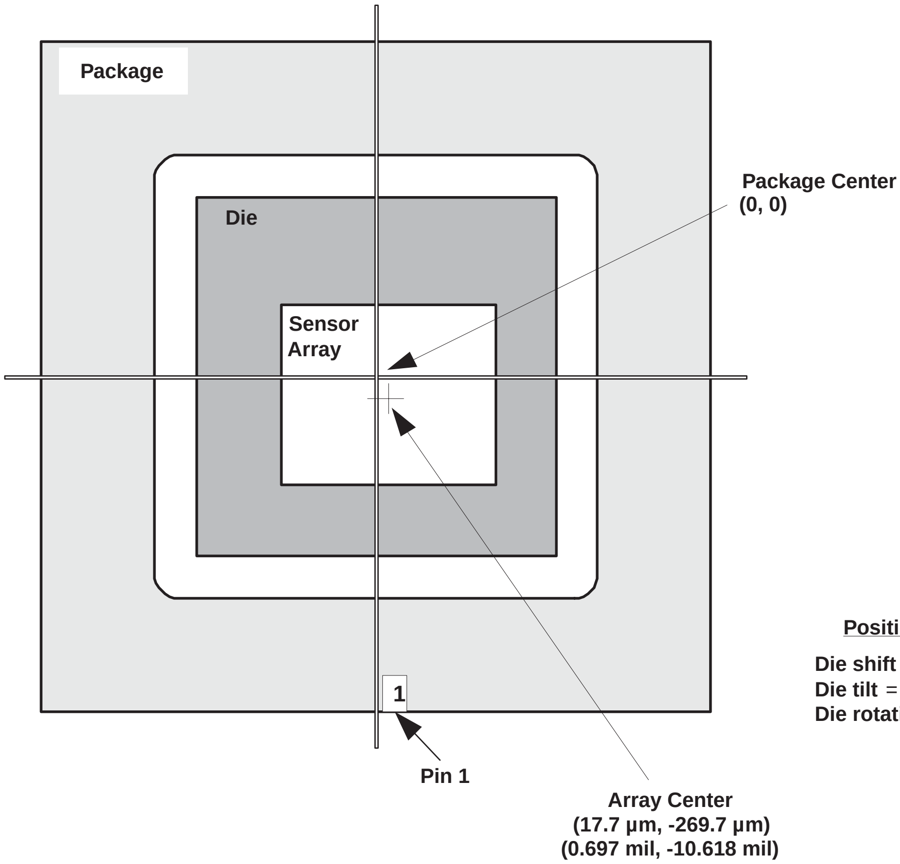


Table 12 OV2610 Package Dimensions

Dimensions	Millimeters (mm)	Inches (in.)
Package Size	14.22 + 0.30 / -0.13 SQ	.560 + .012 / - .005 SQ
Package Height	2.23 ± 0.28	.088 ± .011
Substrate Height	0.51 ± 0.05	.020 ± .002
Cavity Size	8.89 ± 0.13 SQ	.350 ± .005 SQ
Castellation Height	1.14 ± 0.13	.045 ± .005
Pin #1 Pad Size	0.51 x 2.16	.020 x .085
Pad Size	0.51 x 1.02	.020 x .040
Pad Pitch	1.02 ± 0.08	.040 ± .003
Package Edge to First Lead Center	1.524 + 0.25 / -0.13	.06 + .010 / - .005
End-to-End Pad Center-Center	11.18 ± 0.13	.440 ± .005
Glass Size	12.40 ± 0.10 SQ / 13.00 ± 0.10 SQ	.488 ± .004 SQ / .512 ± .004 SQ
Glass Height	0.55 ± 0.05	.022 ± .002

Sensor Array Center

Figure 18 OV2610 Sensor Array Center



<u>Positional Tolerances</u>

Die shift (x,y) = 0.15 mm (6 mils) max.
Die tilt = 1 degrees max.
Die rotation = 3 degrees max.

Important: Most optical systems invert and mirror the image so the chip is usually mounted on the board with pin 1 (SVDD) down as shown.

NOTE: Picture is for reference only, not to scale.

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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