A GPS Radio for Indoor Wireless Communication

Paul Paddan, Paul Naish and Marino Phocas
ParthusCeva(UK) Ltd

BIOGRAPHIES

Paul Paddan has been designing RF and mixed signal circuits for over 25 years in CCD, CMOS and bipolar (including SiGe) technologies for a variety of applications. He is the project manager for the design and development of the RF3000 and co-holds a patent for signal processing in GPS.

Paul Naish has over 20 years experience in mixed signal IC design in CMOS, bipolar, BiCMOS and SiGe circuits. He was the chief designer for a design consultancy and is now the lead designer of the RF3000. Paul is a co-owner of a patent for signal processing in GPS.

Marino Phocas has over 5 years experience in GPS receivers, LNA and antenna design. He holds a BSc and MSc in Radio and High Frequency Engineering. He has worked on CMOS and bipolar circuits, specialising in the modelling of circuit blocks in ADS and Matlab

ABSTRACT

GPS is poised to play a critical role offering commercial opportunities in wireless communications through the E911 directive and 'location-based m-commerce' services. The NavStream 3000 platform provides solutions for the critical areas for implementing GPS in mobile phones - low cost, low power consumption, accuracy, sensitivity and noise immunity.

This paper presents the development of a SiGe BiCMOS GPS rf receiver designed specifically for mobile communication and automotive applications. Key technical drivers are discussed and design options overviewed. Finally important evaluation results will be presented.

INTRODUCTION

The GPS receiver typically comprises two functions: the radio front end and the baseband digital processor. CMOS digital technology improvements now readily (almost) permit the design of the baseband to be portable across silicon vendors and to be incorporated in a system level realisation. The challenge is now for the radio to deliver a GPS solution optimised for indoor tracking in cellular handsets.

Key technical requirements on the RF subsystem are to achieve the usual demanding GPS requirements of high sensitivity, image rejection and blocking immunity simultaneously with the ability of co-operational functioning within a mobile phone handset, both in a hostile RF sense and also to utilise the scarce resources available, of power, space, bandwidth and MIPS (clock-cycles).

These demanding noise, linearity and cost requirements have driven a SiGe BiCMOS solution with minimum external components and a programmable synthesiser that accepts multiple reference frequency inputs. RF3000 downconverts the L1 band carrier at 1575.42MHz to a frequency and format suitable for subsequent digital processing by the baseband processor. The radio is designed for easy interface to most industry standard baseband processors.

We have developed GPS RF models at multiple abstraction levels using Agilent's ADS tool including the baseband correlators and code/carrier mixers. With this approach we are able to define, optimise and specify the performance of each block for silicon implementation. This has an additional benefit in that it expedites the process of translating the design to another process, as the overall performance of the system becomes the target rather than the result of the design process.

It has been to necessary to design RF3000 with the ability to operate from the same reference clock as the host protocol thereby permitting a common clock strategy to be used. An on-chip phase locked loop synthesises suitable local oscillator frequencies for the complex mixers.

This paper will describe our developmental process and our approaches to exploring compromises using modelling techniques, key design decisions and some of the novel architectures and solutions that were needed. Performance results from the evaluation of the chip will be presented.

RF Design/Porting Challenges

The design of a GPS RF chip is relatively straightforward; the challenge lies in getting the best performance at minimum cost. Good chip design will ensure that gain and frequency planning is carried out in the early phases so that the system tradeoffs can be optimised.

The design of the radio normally breaks down into two aspects; the top or system level requirements such as chip gain and frequency planning and the individual circuit block performance. Traditional design approaches use separate tools for system, DSP, and RF design. RFIC designers are thus faced with the unenviable task of reconciling the different modelling results of analogue, digital and RF signals in very high-density circuits. For example, integrating bipolar transistors alongside passive components and high-speed CMOS logic introduces significant uncertainty in the operational behaviour of the circuits.

The initial design and development of a radio requires a careful design process that is focussed on the particular and specific attributes of the process technology being used. Converting this as IP for porting to other processes requires an approach that will reduce the development time and cost significantly below the original. Indeed most customers have very short development times that less than half of the time taken for the first demonstrator design.

What is needed is a methodology that will provide for frequency-domain and mixed-domain simulation technologies; optimisation and statistical design tools; additional device, system and behavioural models. This would allow both a top down and bottom up approach so that transistor level changes due to the different process models can be quickly transported to the system level. Agilent's ADS simulator provides this co-simulation capability.

RF3000 Radio Overview

RF3000 provides the radio front end for the NS3000 GPS receiver developed for use in mobile communications, such as handsets and personal digital assistants (PDAs) as shown in the block diagram in Figure 1.

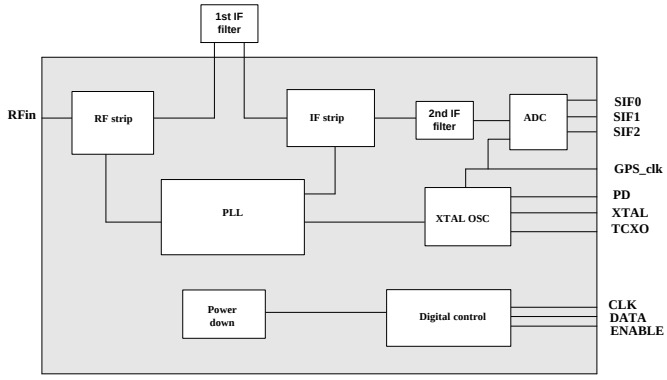


Figure 1: Block Diagram of RF3000A

It is designed on an advanced SiGe BiCMOS process to achieve a very low RF noise figure of <1.5dB, high level of integration, low power consumption and low system implementation cost. The process features SiGe transistors with ft>50GHz, Si bipolar and CMOS transistors, high accuracy passives, including high Q inductors and 4 level of gold metallisation. RF3000 downconverts the L1 band GPS signal at 1575.42 MHz and performs a 2½ bit or 1bit sign/magnitude analogue to digital conversion to produce a signal at 3.78MHz suitable for the baseband processor.

A variable frequency plan provides the necessary local oscillator and baseband clock frequencies from an external TCXO allowing a single board design to be used for different reference clocks from 10 MHz to 26 MHz. Alternatively, a single crystal may be connected to the device using the built in oscillator circuitry for applications permitting higher reference phase noise.

Design Methodology for RF IP

Key challenges on the RF subsystem are to achieve the usual demanding GPS requirements of image rejection and blocking immunity simultaneously with the ability to co-operational function within a mobile phone handset, both in a hostile RF sense and also to utilise the scarce resources available, of power, space, bandwidth and MIPS (clock-cycles) to the interferers generated by the mobile telephone protocols.

We have developed GPS RF models at multiple abstraction levels using Agilent's ADS tool including GPS signal generation through to a single channel baseband correlator for demodulation. With this approach we are able to define, optimise and specify the performance of each block for silicon implementation. This makes the process of translating the design to another process much easier as the overall performance of the system becomes the target rather than the result of the design process.

In addition, this approach allows the RF3000 IP to be used as Parthus supplied block in a customer's test bench thereby reducing the time taken to simulate and derive probable performance in a given system environment. Figure 2 shows the top level schematic of the RF3000 IP in an ADS window.

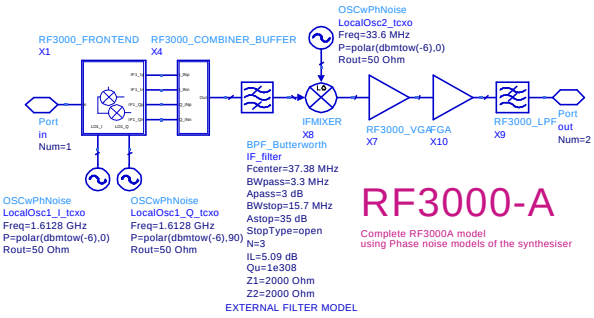


Figure 2 RF3000 ADS model

The typical spectrum of the GPS signal is shown in Figure 3 where the upper trace is the thermal noise power and the lower trace is the GPS power level. The RF3000 has to process a signal that is about 20dB below the noise level.

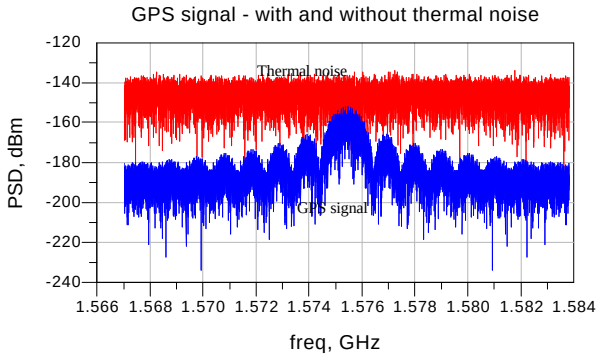


Figure 3 GPS signal spectrum

The various simulators provided by ADS allow for a large variety of test scenarios to be carried out. The use of the harmonic balance simulator is mainly used to provide and test RF block specifications. The complete system is then co-simulated using HP Ptolemy and the circuit envelope simulator. This is an efficient technique where the time step is chosen from the modulation bandwidth rather than the highest frequency of the system.

The following plots and tables are some of the results gathered from simulations carried out in ADS on the RF3000 GPS receiver.

RF3000 Noise performance

One of the key parameters for the front end is the total noise figure referred to the input. ADS can model this parameter efficiently and is summarised in figure 4.

RF3000A Conversion gain and NF no frontend filter

noisefreq	NF_noFilter	PowerGain	VoltageGain
3.780MHz	1.411	67.383	94.328

RF3000A Conversion gain, NF with frontend filter

noisefreq	nf(2)	PGain[0]	VGain[0]
3.780MHz	2.986	65.082	94.028

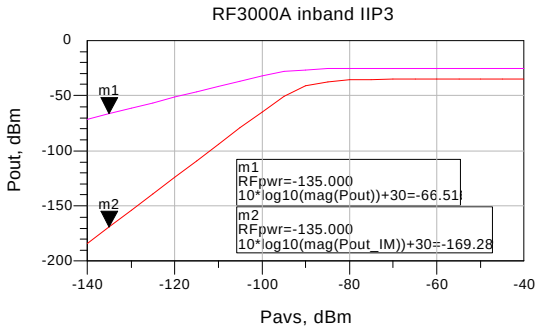
Figure 4 Results of NF and Conversion Gain Simulation

RF3000 jamming performance

The plots below shows the in-band non-linearity of the RF3000 and the voltage conversion gain as a function of the jamming frequency. The incorporation of the RF3000 in a cellular handset means that there will be a jammer at the cellular frequency, about 1800MHz in GSM systems.

A high jammer power level can cause the generation of spurs if the level exceeds the linear range of the circuit blocks. For the scenario below, an output level of +33dBm was used to simulate the incident jammer power level transmitted by the GSM antenna.

A front-end filter model was used in this simulation.



Piip3	IP3in1[0]	PGain[0]	VGain[0]
-83.613	-85.624	67.410	94.356

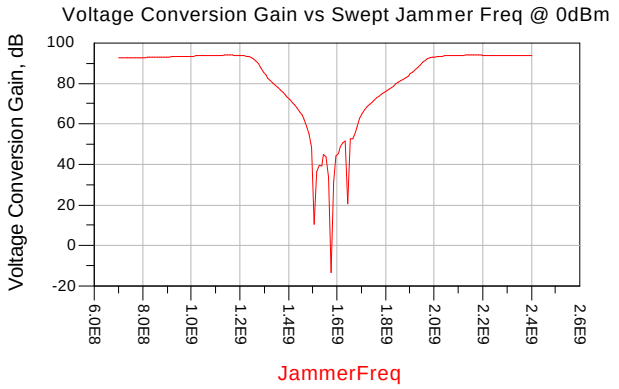


Figure 5 Jamming performance of RF3000

RF3000 Complete GPS Simulations

For complete GPS system simulations, the HP Ptolemy and circuit envelope co-simulation environment is used. Figure 6 shows a typical schematic of an RF3000A co-simulation test bench. It is possible to provide parameter sweeps such as interferer power levels and observe the effects on CNO.

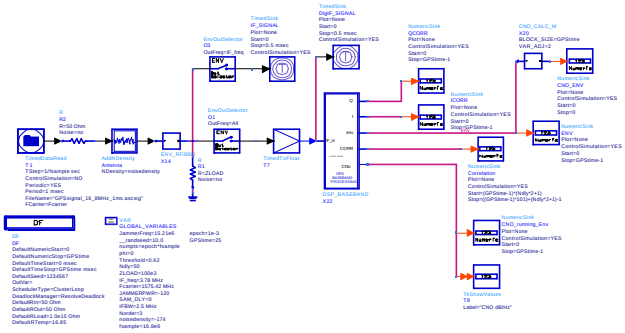
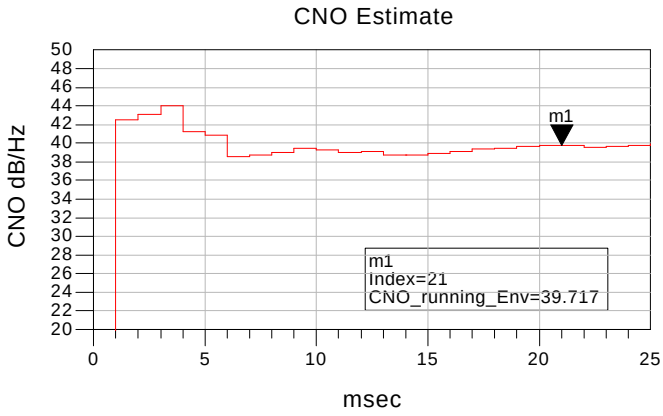


Figure 6 RF3000 HP Ptolemy Co-simulation Schematics

Co-simulation results on RF3000 with input thermal noise, phase noise & receiver noise figure are included below.

CNO	CNOloss	AveSigPhase	AveSigLevel
39.748	4.252	-14.945	745.358



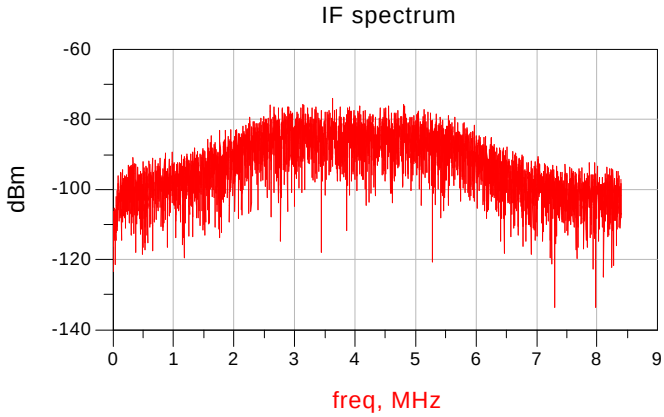


Figure 7 HP Ptolemy Co-simulation results with all noise contributions

The following plots shows an I,Q polar plot of the demodulated GPS signal. In this case there is no data on the GPS signal and therefore one symbol is shown.

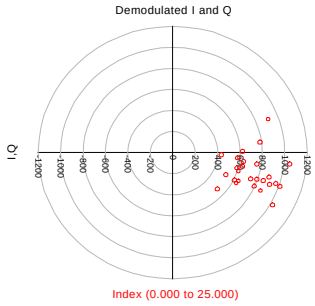


Figure 8 HP Ptolemy Co-simulation results showing I,Q polar plot

?? Co-simulation repeated without phase noise modelled, only input thermal noise and receiver noise figure is included.

CNO	CNOloss	AveSigPhase	AveSigLevel
42.504	1.496	-12.838	785.187

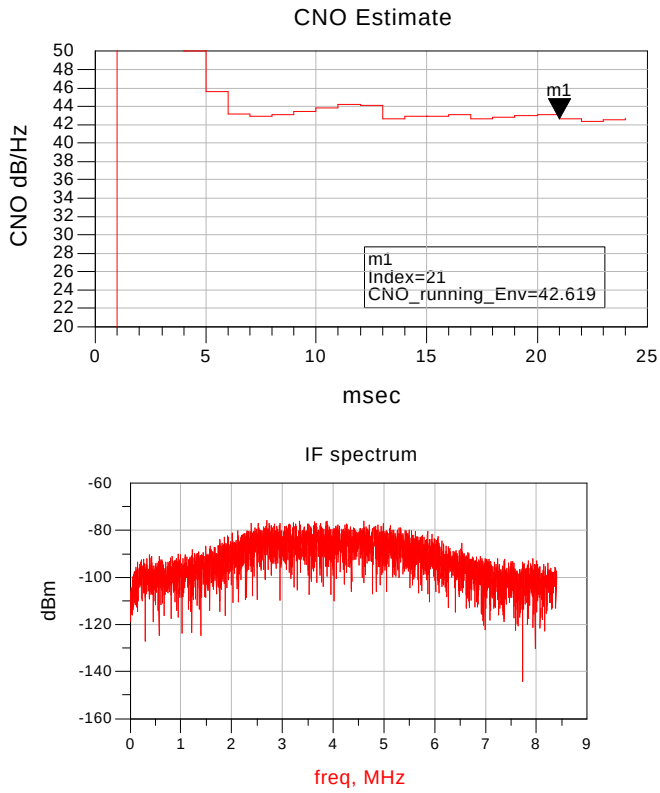


Figure 9 HP Ptolemy Co-simulation results with no phase noise contributions

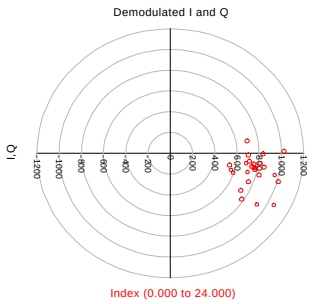


Figure 10 HP Ptolemy Co-simulation results showing I,Q polar plot

?? Co-simulation of noiseless RF3000, only input noise is added.

CNO	CNOloss	AveSigPhase	AveSigLevel
43.436	0.564	-13.798	1059.717

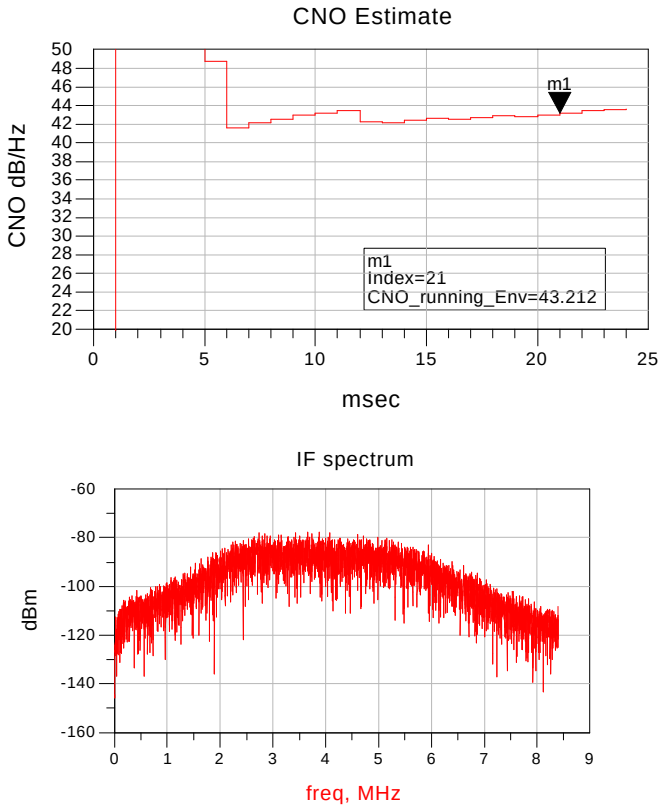


Figure 11 HP Ptolemy Co-simulation results of noiseless receiver

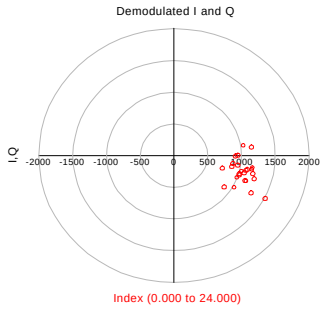


Figure 12 HP Ptolemy Co-simulation results showing I,Q polar plot

RF3000 filter development

One of the key attributes of the GPS radio is to examine the tradeoff filter between providing rejection of the jamming frequencies but at the same time be low cost and low current. We want to be able to determine the lowest order filter that will meet the jamming frequency rejection requirements.

The plot below in Figure 13 shows the results of a simulation evaluating the CNO degradation as a function of filter bandwidth and order.

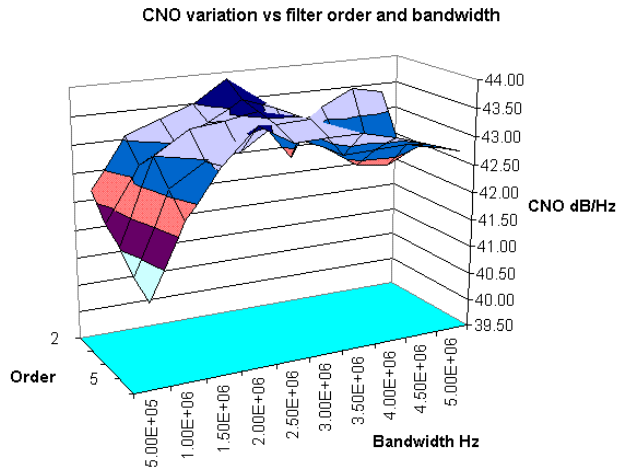


Figure 13 Simulation of optimum filter requirements

Conclusions

To conclude we have found ADS to be a powerful tool in the analysis and design of the RF3000 IP, helping to define and verify our next generation of GPS radio at a number of levels, from sub-system block level simulation up to system simulations. These include the code recovery/correlation in the baseband. ADS has allowed us to identify and explore the key parameter tradeoffs in GPS receiver design.

The main benefit to potential customers is that, in addition to having a better design process, our development methodology can give customers added reassurance by making our design techniques and methods visible to them. Pre-sales, or potential customers can also verify the suitability of our designs and IP to their needs.

We believe that this ADS modelling approach will allow to port the RF3000 IP to other processes with minimum risk and greater confidence, improving the customer's time and cost to market.

ACKNOWLEDGEMENTS

The authors would like to acknowledge that assistance of their colleagues at ParthusCeva during the design of the device.