R5C551

PCI-CARDBUS / 1394 OHCI-LINK

/ 1394 PHY DATA SHEET

REV. 1.22

RICOH

REVISION HISTORY

REVISION	DATE	COMMENTS
0.90	3/19/2001	First Draft for internal use
0.95	4/20/01	Designer′s second check
0.99	6/6/01	Designer′s third check
1.00	8/31/01	Setting is changed in Serial ROM interface. (ch.,4.17.2) 1394 Cable Interface is supported.(ch.,4.19) Vaule of Iccstd, Iccsusp and Icc are added.
1.10	9/18/01	Definitions concern to AVCC_PHY is added. (ch.3.2.11,ch4.11,ch4.15,ch.10.3.6) GPIO is shown in some detail.(ch.4.12)
1.20	2/18/02	Names for power supply pins are changed as follows. VCC_CORE → VCC_CORE18V VCC_PCI → VCC_PCI3V VCC_SLOT → VCC_3V VCC_3V(AUX) → VCC_3V AVCC_PHY → AVCC_PHY3V The description of Power Management Capabilities register is added more. Mistakes in writing are corrected.
1.21	11/11/02	Mistakes in writing are corrected.
1.22	4/22/04	Changes in the chart of Global Reset Timing (ch.10.3.6)

1 OVERVIEW

The R5C551 is the single chip solution offering PCI bus-PC Card bridges and PCI bus-IEEE 1394 OHCI bridge with integrated PHY. The R5C551 is compliant with the latest specification in both PC card and IEEE 1394.
The R5C551 has two PCI functions compliant, the PC Card interface and the IEEE1394 interface.
The PC Card controller of the R5C551 is compliant with PC Card Standard Release 8.0. The R5C551 provides features that make it the best choice for bridging between the PCI bus and PC Cards, and supports any combination of 16-bit (Card-16) and CardBus (Card-32) PC Cards in one socket, powered at 5V or 3.3V, as required.
The R5C551's 16-bit card control register is compatible with the Intel 82365SL and Ricoh's RF5C396/366 in order to maintain backward compatibility with the existing 16-bit PC Card compliant with PCMCIA2.1/JEIDA4.2. All PC card interface signals are individually buffered to allow direct connection to CardBus and Hot Insertion/Removal without external buffers. The R5C551 also allows direct connection to PCI bus.
The R5C551 provides the IEEE1394 OHCI-Link and two ports the IEEE1394 PHY that are compliant with the IEEE1394-1995, IEEE1394a-2000 and the latest 1394 OHCI specifications (Release 1.1/1.0). The R5C551 data rate is capable of 100, 200, and 400 Mbits per second. The R5C551 has the large FIFO buffer and the DMA engine, which work independently to achieve the high-speed transmission rate.
The R5C551 is compliant with the latest PCI Bus Power Management Specification, and provides several low-power modes that enable the host power system to further reduce power consumption.

- PC98/99/2001 compliant
  - Compliant with PC99 Design Guide (Subsystem ID, Subsystem Vendor ID)
  - Compliant with ACPI 1.0 and PCI Bus Power Management 1.1
  - Supports Global Reset

- Low Power consumption
  - Power decreased by the improvement of Power Management supply on the operation
  - Software Suspend mode compliant with ACPI
  - Hardware Suspend
  - Supports CLKRUN# and CCLKRUN#
  - Programmable PHY block sleep mode
  - Powered at 1.8V/2.5V for core logic.

- High-performance

- Single Chip PCI-CardBus/1394 Bridge
  - Bridge function between PCI bus and CardBus
  - Bridge function between PCI bus and 1394 OHCI-LINK

- PCI Bus Interface
  - Compliant with PCI Local Bus Specification2.2
  - the maximum frequency 33MHz
  - Supports PCI Master/Target protocol
  - Separated PCI configuration space
  - Direct connection to PCI bus

- CardBus PC card Bridge
  - Compliant with PC Card Standard Release 8.0 Specification
  - the maximum frequency 33MHz
  - Supports CardBus Master/Target protocol
  - Transfer transactions
    - All memory read/write transaction (bi-direction)
    - I/O read/write transaction (bi-direction)
    - Configuration read/write transaction (PCI → Card)
    - 2 programmable memory windows
    - 2 programmable I/O windows

- PC Card-16 Bridge
  - Compliant with PC Card Standard Release 8.0 Specification
  - 5 programmable memory windows
  - 2 programmable I/O windows
  - Compliant with i82365SL compatible register set / ExCA

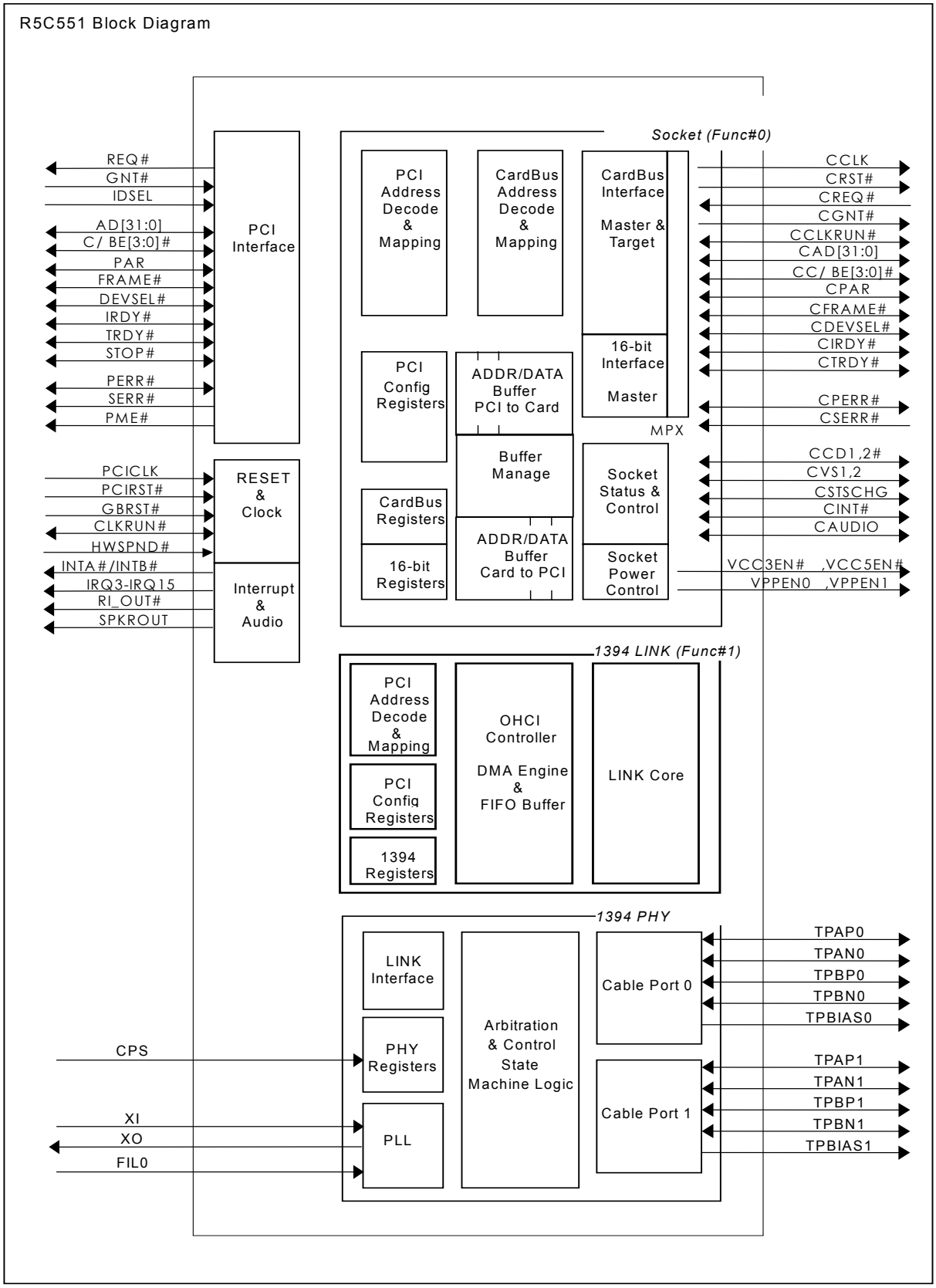
- 1394 OHCI-LINK Bridge
  - Compliant with IEEE1394-1995 and IEEE1394a-2000 Standard Specification
  - Compliant with 1394OHCI Release 1.1/1.0 Standard Specification
  - Cycle Master support
  - FIFO Buffer support
  - Self-ID, physical DMA support
  - Data transmission rate: 100, 200, 400Mbps support

- 1394 PHY
  - Compliant with IEEE1394-1995 and IEEE1394a-2000 Standard Specification
  - Data transmission rate: 100, 200, 400Mbps
  - 2 ports of 1394 Cable interface
  - 24.576MHz crystal oscillator and Internal 393.216MHz PLL
  - Supports cable power monitoring (CPS)
  - Set Initial values of Power Class and CMC by PCI Configuration registers

- System Interrupt
  - INTA# and INTB# support for PCI system interrupt (Each unit is programmable.)
  - IRQn support for ISA system interrupt (Non shared IRQn pins: CardBus only)
  - Supports Serialized IRQ
  - Supports Remote Wake Up by CSTSCHG

- 1.8V or 2.5V/3.3V Mixed Voltage Operation at 3.3MHz
- Supports General Purpose IO
- Supports Posting Write and Prefetching Read for PC Card bridge
- Supports16-bit Legacy mode (3E0/3E2 I/O port)
- Supports Zoomed Video Port
  - Bypass type
- Supports LED active pins for Card LED and 1394LED
- Pin Compatible with R5C485 (CSP1616-208)
- Package
  - 208pin CSP (size=16x16mm, pitch=0.8mm, t=1.5mm)

2 BLOCK DIAGRAM

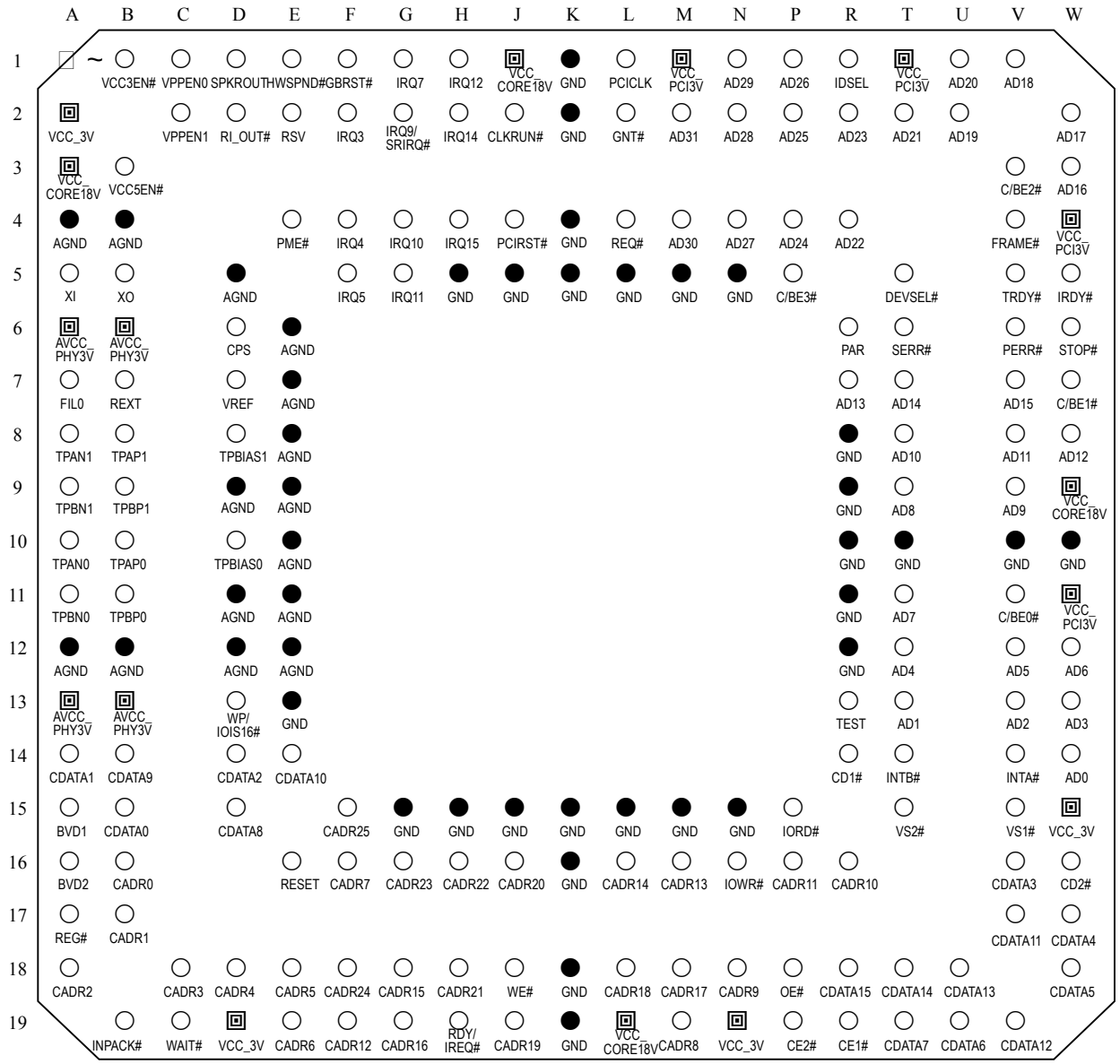


3 PIN DESCRIPTION

3.1 Pin Assignments (208 pin CSP)

- **CSP Pin Assignment**

Bottom View



- **CSP Pin List**

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
B1	VCC3EN#	W2	AD17	V19	CDATA12	A17	REG#
C1	VPPEN0	W3	AD16	U19	CDATA6	B17	CADR1
C2	VPPEN1	V3	C/BE2#	U18	CDATA13	A16	BVD2
D1	SPKROUT	V4	FRAME#	T19	CDATA7	B16	CADR0
D2	RI_OUT#	W5	IRDY#	T18	CDATA14	A15	BVD1
E1	HWSPND#	V5	TRDY#	R19	CE1#	B15	CDATA0
E2	RSV	T5	DEVSEL#	R18	CDATA15	D15	CDATA8
E4	PME#	W6	STOP#	R16	CADR10	A14	CDATA1
F1	GBRST#	V6	PERR#	P19	CE2#	B14	CDATA9
F2	IRQ3	T6	SERR#	P18	OE#	D14	CDATA2
F4	IRQ4	R6	PAR	P16	CADR11	E14	CDATA10
F5	IRQ5	W7	C/BE1#	P15	IORD#	D13	WP/IOIS16#
G1	IRQ7	V7	AD15	N18	CADR9	A11	TPBN0
G2	IRQ9/SRIRQ#	T7	AD14	N16	IOWR#	B11	TPBP0
G4	IRQ10	R7	AD13	M19	CADR8	A10	TPAN0
G5	IRQ11	W8	AD12	M18	CADR17	B10	TPAP0
H1	IRQ12	V8	AD11	M16	CADR13	D10	TPBIAS0
H2	IRQ14	T8	AD10	L18	CADR18	A9	TPBN1
H4	IRQ15	V9	AD9	L16	CADR14	B9	TPBP1
J2	CLKRUN#	T9	AD8	J19	CADR19	A8	TPAN1
J4	PCIRST#	V11	C/BE0#	J18	WE#	B8	TPAP1
L1	PCICLK	T11	AD7	J16	CADR20	D8	TPBIAS1
L2	GNT#	W12	AD6	H19	RDY/IREQ#	A7	FIL0
L4	REQ#	V12	AD5	H18	CADR21	B7	REXT
M2	AD31	T12	AD4	H16	CADR22	D7	VREF
M4	AD30	W13	AD3	G19	CADR16	D6	CPS
N1	AD29	V13	AD2	G18	CADR15	A5	XI
N2	AD28	T13	AD1	G16	CADR23	B5	XO
N4	AD27	R13	TEST	F19	CADR12	B3	VCC5EN#
P1	AD26	W14	AD0	F18	CADR24		
P2	AD25	V14	INTA#	F16	CADR7		
P4	AD24	T14	INTB#	F15	CADR25		
P5	C/BE3#	R14	CD1#	E19	CADR6		
R1	IDSEL	V15	VS1#	E18	CADR5		
R2	AD23	T15	VS2#	E16	RESET		
R4	AD22	W16	CD2#	D18	CADR4		
T2	AD21	V16	CDATA3	C19	WAIT#		
U1	AD20	W17	CDATA4	C18	CADR3		
U2	AD19	V17	CDATA11	B19	INPACK#		
V1	AD18	W18	CDATA5	A18	CADR2		

Pin Name	Ball#	Pin Name	Ball#
VCC_CORE18V	A3, J1, W9, L19	GND	E13, G15, H5, H15, J5, J15, K1, K2, K4, K5, K15, K16, K18, K19, L5, L15, M5, M15, N5, N15, R8, R9, R10, R11, R12, T10, V10, W10
VCC_PCI3V	M1, T1, W4, W11		
VCC_3V	A2, N19, D19, W15		
AVCC_PHY3V	A13, B13, A6, B6	AGND	A4, A12, B4, B12, D5, D9, D11, D12, E6, E7, E8, E9, E10, E11, E12

3.2 Pin Characteristics

16-bit Card Interface		CardBus Card Interface		Pin Characteristics			Note
Pin Name	Dir	Pin Name	Dir	5Vtolerant	PwrRail	Drive	
VCC5EN#	O	VCC5EN#	O	✓	3V	4mA	
VCC3EN#	O	VCC3EN#	O	✓	3V	4mA	
VPPEN0	O	VPPEN0	O	✓	3V	4mA	
VPPEN1	O	VPPEN1	O	✓	3V	4mA	
SPKROUT	I/O	SPKROUT	I/O		3V	4mA	
RI_OUT#	O	RI_OUT#	O	✓	3V	4mA	
HWSPND#	I	HWSPND#	I	✓	3V	–	
PME#	O (OD)	PME#	O (OD)	✓	3V	4mA	
GBRST#	I	GBRST#	I		3V	–	
IRQ3	I/O	IRQ3	I/O	✓	3V	4mA	
IRQ4	I/O	IRQ4	I/O	✓	3V	4mA	
IRQ5	I/O	IRQ5	I/O	✓	3V	4mA	
IRQ7	I/O	IRQ7	I/O	✓	3V	4mA	
IRQ9/ SRIRQ#	I/O	IRQ9/ SRIRQ#	I/O	✓	3V	4mA	
IRQ10	O (TS)	IRQ10	O (TS)	✓	3V	4mA	
IRQ11	O (TS)	IRQ11	O (TS)	✓	3V	4mA	
IRQ12	O (TS)	IRQ12	O (TS)	✓	3V	4mA	
IRQ14	O (TS)	IRQ14	O (TS)	✓	3V	4mA	
IRQ15	I/O	IRQ15	I/O (TS)	✓	3V	4mA	
CLKRUN#	I/O	CLKRUN#	I/O	✓	P	PCI	
PCIRST#	I	PCIRST#	I	✓	P	–	
PCICLK	I	PCICLK	I	✓	P	–	
GNT#	I	GNT#	I	✓	P	–	
REQ#	O (TS)	REQ#	O (TS)	✓	P	PCI	
AD31	I/O	AD31	I/O	✓	P	PCI	
AD30	I/O	AD30	I/O	✓	P	PCI	
AD29	I/O	AD29	I/O	✓	P	PCI	
AD28	I/O	AD28	I/O	✓	P	PCI	
AD27	I/O	AD27	I/O	✓	P	PCI	
AD26	I/O	AD26	I/O	✓	P	PCI	
AD25	I/O	AD25	I/O	✓	P	PCI	
AD24	I/O	AD24	I/O	✓	P	PCI	
C/BE3#	I/O	C/BE3#	I/O	✓	P	PCI	
IDSEL	I	IDSEL	I	✓	P	–	
AD23	I/O	AD23	I/O	✓	P	PCI	
AD22	I/O	AD22	I/O	✓	P	PCI	
AD21	I/O	AD21	I/O	✓	P	PCI	
AD20	I/O	AD20	I/O	✓	P	PCI	

16-bit Card Interface		CardBus Card Interface		Pin Characteristics			Note
Pin Name	Dir	Pin Name	Dir	5Vtolerant	PwrRail	Drive	
AD19	I/O	AD19	I/O	✓	P	PCI	
AD18	I/O	AD18	I/O	✓	P	PCI	
AD17	I/O	AD17	I/O	✓	P	PCI	
AD16	I/O	AD16	I/O	✓	P	PCI	
C/BE2#	I/O	C/BE2#	I/O	✓	P	PCI	
FRAME#	I/O	FRAME#	I/O	✓	P	PCI	
IRDY#	I/O	IRDY#	I/O	✓	P	PCI	
TRDY#	I/O	TRDY#	I/O	✓	P	PCI	
DEVSEL#	I/O	DEVSEL#	I/O	✓	P	PCI	
STOP#	I/O	STOP#	I/O	✓	P	PCI	
PERR#	I/O	PERR#	I/O	✓	P	PCI	
SERR#	O (OD)	SERR#	O (OD)	✓	P	PCI	
PAR	I/O	PAR	I/O	✓	P	PCI	
C/BE1#	I/O	C/BE1#	I/O	✓	P	PCI	
AD15	I/O	AD15	I/O	✓	P	PCI	
AD14	I/O	AD14	I/O	✓	P	PCI	
AD13	I/O	AD13	I/O	✓	P	PCI	
AD12	I/O	AD12	I/O	✓	P	PCI	
AD11	I/O	AD11	I/O	✓	P	PCI	
AD10	I/O	AD10	I/O	✓	P	PCI	
AD9	I/O	AD9	I/O	✓	P	PCI	
AD8	I/O	AD8	I/O	✓	P	PCI	
C/BE0#	I/O	C/BE0#	I/O	✓	P	PCI	
AD7	I/O	AD7	I/O	✓	P	PCI	
AD6	I/O	AD6	I/O	✓	P	PCI	
AD5	I/O	AD5	I/O	✓	P	PCI	
AD4	I/O	AD4	I/O	✓	P	PCI	
AD3	I/O	AD3	I/O	✓	P	PCI	
AD2	I/O	AD2	I/O	✓	P	PCI	
AD1	I/O	AD1	I/O	✓	P	PCI	
AD0	I/O	AD0	I/O	✓	P	PCI	
INTA#	O (OD)	INTA#	O (OD)	✓	P	PCI	
INTB#	O (OD)	INTB#	O (OD)	✓	P	PCI	
TEST	I	TEST	I		3V	–	
CD1#	I (PU)	CCD1#	I (PU)		3V	–	
VS1#	I/O	CVS1	I/O		3V	1mA	
VS2#	I/O	CVS2	I/O		3V	1mA	
CD2#	I (PU)	CCD2#	I (PU)		3V	–	
RSV	I/O	RSV	I/O		3V	–	

16-bit Card Interface		CardBus Card Interface		Pin Characteristics			Note
Pin Name	Dir	Pin Name	Dir	5Vtolerant	PwrRail	Drive	
CDATA3	I/O	CAD0	I/O	✓	3V	4mA	
CDATA4	I/O	CAD1	I/O	✓	3V	4mA	
CDATA11	I/O	CAD2	I/O	✓	3V	4mA	
CDATA5	I/O	CAD3	I/O	✓	3V	4mA	
CDATA12	I/O	CAD4	I/O	✓	3V	4mA	
CDATA6	I/O	CAD5	I/O	✓	3V	4mA	
CDATA13	I/O	CAD6	I/O	✓	3V	4mA	
CDATA7	I/O	CAD7	I/O	✓	3V	4mA	
CDATA14	I/O	–	–	✓	3V	4mA	
CE1#	O	CC/BE0#	I/O	✓	3V	4mA	
CDATA15	I/O	CAD8	I/O	✓	3V	4mA	
CADR10	O	CAD9	I/O	✓	3V	4mA	
CE2#	O	CAD10	I/O	✓	3V	4mA	
OE#	O	CAD11	I/O	✓	3V	4mA	
CADR11	O	CAD12	I/O	✓	3V	4mA	
IORD#	O	CAD13	I/O	✓	3V	4mA	
CADR9	O	CAD14	I/O	✓	3V	4mA	
IOWR#	O	CAD15	I/O	✓	3V	4mA	
CADR8	O	CC/BE1#	I/O	✓	3V	4mA	
CADR17	O	CAD16	I/O	✓	3V	4mA	
CADR13	O	CPAR	I/O	✓	3V	4mA	
CADR18	O	–	–	✓	3V	4mA	
CADR14	O	CPERR#	I/O (PU)	✓	3V	4mA	1
CADR19	O	–	I/O (PU)	✓	3V	4mA	1
WE#	O	CGNT#	O	✓	3V	4mA	
CADR20	O	CSTOP#	I/O (PU)	✓	3V	4mA	1
RDY/ IREQ#	I (PU)	CINT#	I (PU)	✓	3V	–	
CADR21	O	CDEVSEL#	I/O (PU)	✓	3V	4mA	1
CADR16	O (TS)	CCLK	O (TS)	✓	3V	CB	
CADR22	O	CTRDY#	I/O (PU)	✓	3V	4mA	1
CADR15	O	CIRDY#	I/O (PU)	✓	3V	4mA	1
CADR23	O	CFRAME#	I/O	✓	3V	4mA	
CADR12	O	CC/BE2#	I/O	✓	3V	4mA	
CADR24	O	CAD17	I/O	✓	3V	4mA	
CADR7	O	CAD18	I/O	✓	3V	4mA	
CADR25	O	CAD19	I/O	✓	3V	4mA	
CADR6	O	CAD20	I/O	✓	3V	4mA	
CADR5	O	CAD21	I/O	✓	3V	4mA	
RESET	O (TS)	CRST#	O (TS)	✓	3V	2mA	

16-bit Card Interface		CardBus Card Interface		Pin Characteristics			Note
Pin Name	Dir	Pin Name	Dir	5Vtolerant	PwrRail	Drive	
CADR4	O	CAD22	I/O	✓	3V	4mA	
WAIT#	I (PU)	CSERR#	I (PU)	✓	3V	–	
CADR3	O	CAD23	I/O	✓	3V	4mA	
INPACK#	I (PU)	CREQ#	I (PU)	✓	3V	–	
CADR2	O	CAD24	I/O	✓	3V	4mA	
REG#	O	CC/BE3#	I/O	✓	3V	4mA	
CADR1	O	CAD25	I/O	✓	3V	4mA	
BVD2/ SPKR#/ LED	I (PU)	CAUDIO	I (PU)	✓	3V	–	
CADR0	O	CAD26	I/O	✓	3V	4mA	
BVD1/ STSCHG#/ RI#	I (PU)	CSTSCHG	I (PD)	✓	3V	–	2
CDATA0	I/O	CAD27	I/O	✓	3V	4mA	
CDATA8	I/O	CAD28	I/O	✓	3V	4mA	
CDATA1	I/O	CAD29	I/O	✓	3V	4mA	
CDATA9	I/O	CAD30	I/O	✓	3V	4mA	
CDATA2	I/O	–	–	✓	3V	4mA	
CDATA10	I/O	CAD31	I/O	✓	3V	4mA	
WP/ IOIS16#	I (PU)	CCLKRUN#	I/O (PU)	✓	3V	4mA	1
XI	I	XI	I		AP		
XO	O	XO	O		AP		
FIL0	I/O	FIL0	I/O		AP		
CPS	I	CPS	I		AP	1394	
VREF	I/O	VREF	I/O		AP		
REXT	I/O	REXT	I/O		AP		
TPBN0	I/O	TPBN0	I/O		AP	1394	
TPBP0	I/O	TPBP0	I/O		AP	1394	
TPAN0	I/O	TPAN0	I/O		AP	1394	
TPAP0	I/O	TPAP0	I/O		AP	1394	
TPBIAS0	O	TPBIAS0	O		AP	1394	
TPBN1	I/O	TPBN1	I/O		AP	1394	
TPBP1	I/O	TPBP1	I/O		AP	1394	
TPAN1	I/O	TPAN1	I/O		AP	1394	
TPAP1	I/O	TPAP1	I/O		AP	1394	
TPBIAS1	O	TPBIAS1	O		AP	1394	

Pin Type
I: Input Pin, O: Output Pin, I/O: Input Output Pin,
I (PU): Input Pin with Internal Pullup Resister,
I (PD): Input Pin with Internal Pulldown Resister,
I/O (PU): Input Output Pin with Internal Pullup Resister,
I/O (PD): Input Output Pin with Internal Pulldown Resister,
O (TS): Three State Output Pin, O (OD): Open Drain Output Pin

Power Rail
P: VCC_PCI3V C: VCC_CORE18V AP: AVCC_PHY3V
3V: VCC_3V

Drive
PCI: PCI Compliant
CB: PCMCIA CardBus PC Card Compliant
1394: IEEE1394a-2000 Compliant

Note
1: Pullup is attached when PC Card Interface is configured as a CardBus Interface Mode.
2: Pullup or Pulldown is configured according to the type of a card inserted.

3.3 Pin Functions Outline

In this chapter, the detailed signal pins in the R5C551 are explained. Every signal is divided according to their relational interface.

Card Interface signal pin is multi−functional pin. Card Interface mode is configured automatically by the card insertion; CardBus card or 16−bit card. And the pin function is redefined again.

mark means the signal is on either active or asserted when the signal is low−level. Otherwise, no−mark means the signal is asserted when the signal is high−level.

The following the notations are used to describe the signal type.

IN	Input Pin
OUT	Output Pin
OUT (TS)	Three State Output Pin
OUT (OD)	Open Drain Output Pin
I/O	Input Output Pin
I/O (OD)	Input Output Pin (Output is Open Drain)
s/h/z	Sustained Tri−State is an active low tri−state signal owned and driven by one and only one agent at a time. The agent that drives a s/h/z pin low must drive it high for at least one clock before letting it float. A new agent cannot start driving a s/h/z signal any sooner than one clock after the previous owner tri−state is.

3.3.1 PCI Local Bus interface signals

Pin Name	Type	Description
		PCI Bus Interface Pin Descriptions
PCICLK	IN	***PCI CLOCK:*** PCICLK provides timing for all transactions on PCI. All other PCI signals are sampled on the rising edge of PCICLK.
CLKRUN#	I/O (OD)	***PCI CLOCK RUN:*** This signal indicates the status of PCICLK and an open drain output to request the starting or speeding up of PCICLK. This pin complies with Mobile PCI specification. If CLKRUN# is not implemented, then this pin should be tied low. In this case, CardBus clock is controlled by setting of StopClock bit included Socket Control Register. This signal has no meaning for the PC Card16 Cards, the CardBus Cards that does not support CCLKRUN# and not insert Cards to socket. During PCI bus reset is asserted, this pin placed in a high-impedance state. And also, refer to the chapter 4.18 on the LED output.
PCIRST#	IN	***PCI RESET:*** This input is used to initialize all registers except PHY block, sequences and signals of the R5C551 to their reset states. PCIRST# causes the R5C551 to place all output buffers in a high-impedance state. The negation of PCIRST# requires no-bounds.
AD [31:0]	I/O	***ADDRESS AND DATA:*** Address and Data are multiplexed on the same PCI pins.
C/BE [3:0]#	I/O	***BUS COMMAND AND BYTE ENABLES:*** Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of transaction, C/BE [3:0]# define the bus command. During the data phase C/BE [3:0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data.
PAR	I/O	***PARITY:*** Parity is even parity across AD [31:0] and C/BE [3:0]#. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. The master drives PAR for address and write data phases; the target drives PAR for read data phases.
FRAME#	I/O s/h/z	***CYCLE FRAME:*** This signal is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase or has complete.
TRDY#	I/O s/h/z	***TARGET READY:*** This signal indicates the initialing agent's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a read, TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD [31:0]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted both IRDY# and TRDY# are asserted together.
IRDY#	I/O s/h/z	***INITIATOR READY:*** This signal indicates the initiating agent's ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD [31:0]. During a read, it indicates the target is prepared to accept data. Wait cycles are inserted both IRDY# and TRDY# are asserted together.
STOP#	I/O s/h/z	***STOP:*** This signal indicates the current target is requesting the master to stop the current transaction.
IDSEL	IN	***INITIALIZATION DEVICE SELECT:*** This signal is used as a chip select during configuration read and write transactions.
DEVSEL#	I/O s/h/z	***DEVICE SELECT:*** When actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.
PERR#	I/O s/h/z	***PARITY ERROR:*** This signal is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The R5C551 drives this output active "low" if it detects a data parity error during a write phase.

Pin Name	Type	Description
		PCI Bus Interface Pin Descriptions (Continued)
SERR#	OUT (OD)	***SYSTEM ERROR:*** This signal is pure open drain. The R5C551 actively drives this output for a single PCI clock when it detects an address parity error on either the primary bus or the secondary bus.
REQ#	OUT (TS)	***REQUEST:*** This signal indicates to the arbiter that the R5C551 desires use of the bus. This is a point to point signal.
GNT#	IN	***GRANT:*** This signal indicates the R5C551that access to the bus has been granted. This is a point to point signal.
PME#	OUT (OD)	***POWER MANAGEMENT EVENT:*** This signal is pure open drain. This signal indicates a change in the power management state.
GBRST#	IN	***GLOBAL RESET:*** This input is used to initialize registers for control of PME_Context register. This should be asserted only once when system power supply is on.

3.3.2 System Interrupt signals

Pin Name	Type	Description
		System Interrupt Pin Descriptions
INTA#	OUT (OD)	***PCI INTERRUPT REQUEST A:*** This signal indicates a programmable interrupt request generated from the card socket interface. This signal is connected PCI bus INTA# interrupt line.
INTB#	OUT (OD)	***PCI INTERRUPT REQUEST B:*** This signal indicates a programmable interrupt request generated from the IEEE 1394 interface. This signal is connected PCI bus INTB# interrupt line.
IRQ3/GPIO0 IRQ4/GPIO1 IRQ5/GPIO2 IRQ7/GPIO3 IRQ9/SRIRQ#	I/O (TS)	***SYSTEM INTERRUPT REQUEST IRQ 3-15:*** These signals indicate the interrupt requests from one of the cards and are connected to the ISA bus IRQx signal. IRQ12 is reassigned as an LED output when LED enable bit in ATA control register is set to one. When Serial IRQ Enable bit in Misc Control register is set to one, IRQ9 is reassigned as SRIRQ# signal, at the same time IRQ15 is reassigned as LED1394# and IRQ10are reassigned as LED# signal. When Serial IRQ signal is enabled, IRQ3, 4,5 and 7 are assigned as GPIO (General Purpose I/O) pins. These are input/output pins determined by user without effect on the controller transaction. *IRQ [3:9] are three-state pin on IRQ.
IRQ10/LED# IRQ11 IRQ12/ LEDOUT IRQ14 IRQ15/ LED1394#	OUT (TS)	
RI_OUT#	OUT (TS)	***RING INDICATE OUTPUT:*** When 16-bit card is inserted, this signal is assigned as RI_OUT# from a socket's RI# input when Ring Indicate Enable bit in Interrupt and General control register is set to one.

3.3.3 16-bit PC Card Interface signals

Pin Name	Type	Description
		16-bit PC Card Interface Pin Descriptions
CDATA [15:0]	I/O	***16-bit Card DATA BUS SIGNALS [15:0]:*** Input buffer is disabled when the card socket power supply is off or card is not inserted.
CADR [25:0]	OUT (TS)	***16-bit Card ADDRESS BUS SIGNALS [25:0]:***
IORD#	OUT (TS)	***16-bit Card I/O READ:***
IOWR#	OUT (TS)	***16-bit Card I/O WRITE:***
OE#	OUT (TS)	***16-bit Card OUTPUT ENABLE:***
WE#	OUT (TS)	***16-bit Card WRITE ENABLE:***
CE1#	OUT (TS)	***16-bit Card CARD ENABLE 1:***
CE2#	OUT (TS)	***16-bit Card CARD ENABLE 2:***
REG#	OUT (TS)	***16-bit Card ATTRIBUTE MEMORY SELECT:*** This signal selects Attribute Memory access or common memory access during 16bit memory cycle. Attribute memory access is selected when this signal is “low” and common memory access is selected when this signal is “high”.
READY/ IREQ#	IN	***16-bit Card READY/BUSY or INTERRUPT REQUEST:*** This signal has two different functions. READY/BUSY# input on the memory PC card, and IREQ# input on the I/O card.
WP/ IOIS16#	IN	***16-bit Card WRITE PROTECT or CARD IS 16-BIT PORT:*** This signal has two different functions. Write Protect Switch input on the memory PC card, and IOIS16 input on the I/O card.
RESET	OUT (TS)	***16-bit Card CARD RESET:***
WAIT#	IN	***16-bit Card BUS CYCLE WAIT:***
BVD1/ STSCHG#/ RI#	IN	***16-bit Card BATTERY VOLTAGE DETECT 1 or STATUS CHANGE:*** This signal has three different functions. The battery voltage detect input 1 on the memory PC card, and Card Status Change#/Ring Indicate# input on the I/O card.
BVD2/ SPKR#/ LED	IN	***16-bit Card BATTERY VOLTAGE DETECT 2 or DIGITAL AUDIO or LED INPUT:*** This signal has three different functions. The battery voltage detect input 2 on the memory PC card, and SPEAKER# input or LED input on the I/O card.
INPACK#	IN	***16-bit Card INPUT ACKNOWLEDGE:***
CD1#	IN	***16-bit Card CARD DETECT 1:*** CD [2:1]# pins are used to detect the card insertion. CD [2:1]# pins are used in conjunction with VS [2:1] to decode card type information.
CD2#	IN	***16-bit Card CARD DETECT 2:*** CD [2:1]# pins are used to detect the card insertion. CD [2:1]# pins are used in conjunction with VS [2:1] to decode card type information.
VS1	I/O	***16-bit Card CARD VOLTAGE CAPABILITY SENSE 1:*** VS [2:1] pins are used in conjunction with CD [2:1]# to decode card type information.
VS2	I/O	***16-bit Card CARD VOLTAGE CAPABILITY SENSE 2:*** VS [2:1] pins are used in conjunction with CD [2:1]# to decode card type information.

3.3.4 CardBus PC Card Interface signals

Pin Name	Type	Description
		CardBus PC Card Interface Pin Descriptions
CCLK	OUT (TS)	***CardBus Clock:*** This signal provides timing for all transactions on the PC Card Standard interface and it is an input to every PC Card Standard device. All other CardBus PC Card signals, except CRST# (upon assertion), CCLKR, CCLKRUN#, CINT#, CSTSCHG, CAUDIO, CCD [2:1]#, and CVS [2:1], are sampled on the rising edge of CCLK, and all timing parameters are defined with respect to this edge.
CCLKRUN#	I/O s/h/z	***CardBus Clock Run:*** This signal is used by cards to request starting (or speeding up) clock; CCLK. CCLKRUN# also indicates the clock status. For PC cards, CCLKRUN# is an open drain output and it is also an input. The R5C551indicates the clock status of the primary bus to the CardBus card.
CRST#	OUT (TS)	***CardBus Card Reset:*** This signal is used to bring CardBus Card specific registers, sequencers and signals to a consistent state. Anytime CRST# is asserted, all CardBus card output signals will be driven to their begin state.
CAD [31:0]	I/O	***CardBus Address/Data:*** These signals are multiplexed on the same CardBus card pins. A bus transaction consists of an address phase followed by one or more data phases. CardBus card supports both read and write bursts. CAD [31:0] contains a physical address (32 bits). For I/O, this is a byte address; for configuration and memory it is a DWORD address. During data phases, CAD [7:0] contains the east significant byte (LSB) and CAD [31:24] contains the most significant byte (MSB). Write data is stable and valid when CIRDY# is asserted and read data is stable and valid when CTRDY# is asserted. Data is transferred during those clocks where both CIRDY# and CTRDY# are asserted.
CC/BE [3:0]#	I/O	***CardBus Command/Bye Enables:*** These signals are multiplexed on the same CardBus card pins. During the address phase of a transaction, CC/BE [3:0]# define the bus command. During the data phase, CC/BE [3:0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. CC/BE [0]# applies to byte 0 (LSB) and CC/BE [3]# applies to byte 3 (MSB).
CPAR	I/O	***CardBus Parity:*** This signal is even parity across CAD [31:0] and CC/BE [3:0]#. Parity generation is required by all CardBus card agents. CPAR is stable and valid clock after either CIRDY# is asserted on a write transaction or CTRDY# is asserted on a read transaction. Once CPAR is valid, it remains valid until one clock after the completion of the current data phase. (CPAR has the same timing as CAD [31:0] but delayed by one clock.) The master drives CPAR for address and write data phases; the target drives CPAR for read data phases.
CFRAME#	I/O s/h/z	***CardBus Cycle Frame*:** This signal is driven by the current master to indicate the beginning and duration of a transaction. CFRAME# is asserted to indicate that a bus transaction is beginning. While CFRAME# is asserted, data transfers continue. When CFRAME# is deasserted, the transaction is in the final data phase.
CIRDY#	I/O s/h/z	***CardBus Initiator Ready:*** This signal indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. CIRDY# is used in conjunction with CTRDY#. A data phase is completed on any clock both CIRDY# and CTRDY# are sampled asserted. During a write, CIRDY# indicates that valid data is present on CAD [31:0]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both CIRDY# and CTRDY# are asserted together.
CTRDY#	I/O s/h/z	***CardBus Target Ready:*** This signal indicates the agent's (selected target's) ability to complete the current data phase of the transaction. CTRDY# is used in conjunction with CIRDY#. A data phase is completed on any clock both CTRDY# and CIRDY# are sampled asserted. During a read, CTRDY# indicates that valid data is present on CAD [31:0]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both CIRDY# and CTRDY# are asserted together.
CSTOP#	I/O s/h/z	***CardBus Stop:*** This signal indicates the current target is requesting the master to stop the current transaction.
CDEVSEL#	I/O s/h/z	***CardBus Device Select:*** This signal indicates the driving device has decoded its address as the target of the current access when actively driven. As an input, CDEVSEL# indicates whether any device on the bus has been selected.

Pin Name	Type	Description
CardBus PC Card Interface Pin Descriptions (Continued)		
CREQ#	IN	***CardBus Request:*** This signal indicates to the arbiter that this agent desires use of the bus. Every master has its own CREQ#.
CGNT#	OUT	***CardBus Grant:*** This signal indicates to the agent that access to the bus has been granted. Every master has its own CGNT#.
CPERR#	I/O s/h/z	***CardBus Parity Error:*** This signal is only for the reporting of data parity errors during all CardBus Card transactions except a Special Cycle. An agent cannot report a CPERR# until it has claimed the access by asserting CDEVSEL# and completed a data phase.
CSERR#	IN	***CardBus System Error:*** This signal is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result could be catastrophic.
CINT#	IN	***CardBus Interrupt Request:*** This signal is an input signal from CardBus card. It is level sensitive, and asserted low (negative true), using an open drain output driver. The assertion and deassertion of CINT# is asynchronous to CCLK.
CSTSCHG	IN	***CardBus Card Status Change:*** This signal is an input signal used to alert the system to changes in the READY, WP, or BVD [2:1] conditions of the card. It is also used for the system and/or CardBus card interface Wake up. CSTSCHG is asynchronous to CCLK.
CAUDIO	IN	***CardBus Card Audio:*** This signal is a digital audio input signal from a CardBus Card to the system's speaker. CAUDIO has no relationship to CCLK.
CCD1#	IN	***CardBus Card Detect 1:*** CCD [2:1]# pins are used to detect the card insertion. CCD [2:1]# pins are used in conjunction with CVS [2:1] to decode card type information.
CCD2#	IN	***CardBus Card Detect 2:*** CCD [2:1]# pins are used to detect the card insertion. CCD [2:1]# pins are used in conjunction with CVS [2:1] to decode card type information.
CVS1	I/O	***CardBus Card Voltage Sense 1:*** CVS [2:1] pins are used in conjunction with CCD [2:1]# to decode card type information.
CVS2	I/O	***CardBus Card Voltage Sense 2:*** CVS [2:1] pins are used in conjunction with CCD [2:1]# to decode card type information.

3.3.5 Socket Power Control signals

Pin Name	Type	Description
Socket Power Control Signal Descriptions		
VCC5EN#	OUT	***VCC 5V ENABLE:***
VCC3EN#	OUT	***VCC 3.3V ENABLE:***
VPPEN0	OUT	***VPP ENABLE 0:***
VPPEN1	OUT	***VPP ENABLE 1:***

3.3.6 Audio signal

Pin Name	Type	Description
Audio Pin Descriptions		
SPKROUT	I/O	***SPEAKER OUTPUT:*** This signal is a digital audio output from SPKR#.

3.3.7 Hardware Suspend signal

Pin Name	Type	Description
		Hardware Suspend
HWSPND#	I	***Hardware Suspend:*** This signal works as HWSPND# input. PCIRST# is not accepted as long as HWSPND# is asserted so that VCC_PCI3V can be powered off. When Serial IRQ mode is set, HWSPND# must be asserted after Serial IRQ mode on the chip-set has been deasserted. When Hardware Suspend mode is off, HWSPND# must be deasserted before Serial IRQ mode is enabled. When a power is on, follow the reset sequence shown in the chapter 4.10 in order to confirm the input of PCIRST# and PCLK.

3.3.8 TEST signal

Pin Name	Type	Description
		Test Pin Descriptions
TEST	I	***TEST:*** This signal is a test mode pin. Usually, this pin must be tied low.
RSV	I/O	***Reserve:*** Reserved. Usually, this pin must be opened.

3.3.9 IEEE1394 PHY Interface signals

Pin Name	Type	Description
		IEEE1394 Cable Interface Pin Descriptions
TPAP1 TPAP0	I/O	***TPA Positive:*** Twisted-pair cable A (positive) differential signal terminals.
TPBP1 TPBP0	I/O	***TPB Positive:*** Twisted-pair cable B (positive) differential signal terminals.
TPAN1 TPAN0	I/O	***TPA Negative:*** Twisted-pair cable A (negative) differential signal terminals.
TPBN1 TPBN0	I/O	***TPB Negative:*** Twisted-pair cable B (negative) differential signal terminals.
TPBIAS1 TPBIAS0	OUT	***TP Bias:*** Twisted-pair bias output.
CPS	IN	***Cable Power Status:*** This pin detects the Cable Power Status. Please refer to Chapter 4.19.3 for details of CPS.

3.3.10 IEEE1394 Control signals

Pin Name	Type	Description
		IEEE1394 Control Pin Descriptions
VREF	I/O	***Voltage reference Resistance:*** It is necessary to connect a capacitance of 0.01uF between this pin and AGND.
REXT	I/O	***Resistance External:*** It is necessary to connect a resistor of 10kΩ±1% between this pin and AGND.
XI	IN	***X'tal In:*** 24.576MHz
XO	OUT	***X'tal Out:*** 24.576MHz
FIL0	I/O	***Filter:*** This pin connects to the PLL Filter. It is necessary to connect a capacitance of 0.01uF between this pin and AGND.

3.3.11 Power and GND signals

Pin Name	Type	Description
		Power Pin Descriptions
VCC_PCI3V	PWR	***PCI VCC:*** Power Supply pins for PCI interface signals. This pin can be powered at 3.3V.
VCC_CORE18V	PWR	***CORE VCC:*** Power Supply pins for the internal core logic. This pin can be powered at 1.8V or 2.5V. Don't turn off this pin during suspension when PME# resume.
VCC_3V	PWR	***3V VCC:*** This supply pin is connected to 3.3V. This pin must not be off on the suspend mode because of the power supply for PME# and GBRST#. This pin supply for a slot of the PC Card Controller also.
AVCC_PHY3V	PWR	***1394 Analog VCC:*** Power Supply for 1394 PHY Analog interface. This pin can be powered at 3.3V. This pin must not be off on the suspend mode because of the power supply for Cable interface block.
GND	PWR	***Digital GND:***
AGND	PWR	***Analog GND:***

4 FUNCTIONAL DESCRIPTION

4.1 Device Configuration

The R5C551 supports PCI-CardBus Bridge Interface functions for PC Card socket and PCI-IEEE1394 (OHCI-LINK) bridge function. Logically the R5C551 looks to the primary PCI as a separate secondary bus residing in a single device. The socket and 1394 have its own register spaces as follows.

4.1.1 PCI Configuration Register Space

PCI Configuration registers are used to control the basic operations, as a setting of PCI device and a status control, in the R5C551. The R5C551 implements 256 bytes of configuration space a socket. The first 64bytes in a socket configuration space adhere to a predefined header format. The remaining 192 bytes of the configuration space are used for a socket control purpose. The R5C551 configuration space is accessible only from the primary PCI bus. No other interfaces respond to configuration cycles.

4.1.2 CardBus (32-bit) Card Control Register Space

CardBus Card Control registers are used to manage status changed events, remote wakeup events and status information about the PC Card in the socket. These registers are used for PC Card-32 as well as PC Card-16. The PC Card Control Register Base Address register points to the 4 Kbyte memory mapped I/O space that contains both the PC Card-32 and PC Card-16 Status and Control registers. Socket Status/Control Registers for Card-32 are placed in the lower 2Kbyte of the 4Kbyte and start at offset 000h.

4.1.3 16-bit Card Control Register Space

Socket Status/Control Registers for PC Card-16 are placed in the upper 2Kbyte of the 4Kbyte pointed by the PC Card Control Register Base Address register and start at offset 800h.

4.1.4 16-bit Legacy Port

Legacy mode allows all 16-bit Card Control registers to be accessed through the index/data port at I/O address 3E0/3E2 in order to maintain the backward compatibility with Intel 82365 compatibles like Ricoh RF5C396/366.

4.1.5 1394 OHCI-LINK Register Space

1394 OHCI-LINK registers are compliant with the 1394 OHCI specifications. The 1394 OHCI Register Base Address register points to the 2Kbyte memory mapped I/O space. These registers are used to control OHCI-LINK and to set DMA context.

4.1.6 1394 PHY Register Space

1394 PHY registers are compliant with the IEEE1394a-2000 standard specifications. The configuration of the PHY block, (ex. the value of Gap Count.), is set in this register, and accessed through the PHY Control register of the1394 OHCI-LINK register space.

4.2 CardBus Card Configuration Mechanism

CardBus Card supports the configuration spaces following the PCI specifications. CardBus Card is also configured by the host. The R5C551 supports functions of changing Type 1 PCI configuration command into Type 0 CardBus configuration command and transferring them.

4.3 Address Window and Mapping Mechanism

The R5C551 supports PCI-Card Bridge Interface functions and determines if it is CardBus Card or 16-bit Card automatically on inserting a card.

On CardBus Card interface, the transaction is forwarded by two I/O windows, two memory map I/Os and a prefetchable memory window. CardBus Card address and PCI system address use a flat address in common. So the address range specified by a base register and a limit register is forwarded from PCI to CardBus Card.

And also, the R5C551 supports CardBus Master, so the transfer transaction from CardBus Card interface to PCI interface or to the other card interface is supported. The transaction out of an address range specified by a base register and a limit register is passed to PCI bus.

On 16-bit Card interface, the transaction is transfered by two I/O windows and five memory windows set on 16-bit Card Status Control registers that are compatible with PCIC. The transfer is permitted only from PCI interface to CardBus.

4.3.1 ISA mode

The R5C551 supports the ISA mode for PCI-CardBus Bridge function. Setting ISA enable bit of Bridge Control register enables ISA mode. This mode applies only to addresses that are enabled by the I/O Base and Limit registers and are in the first 64K Byte of PCI I/O space. When set, the R5C551 block forwarding from PCI to CardBus I/O transactions addressing the last 768bytes in each 1K byte block. In the opposite direction (CardBus to PCI) I/O transaction is forwarded if they address the last 768 bytes in each 1K blocks.

4.3.2 VGA mode

The R5C551 supports the VGA mode. When the VGA enable bit of Bridge Control register is set, the R5C551 forward transactions from PCI to CardBus I/F in the following ranges.

Memory address:	0A0000h to 0BFFFFh
I/O address:	AD [9:0] = 3B0h to 3BBh, and 3C0h to 3DFh (Inclusive of ISA address aliases - AD [15:10] are not decoded.)

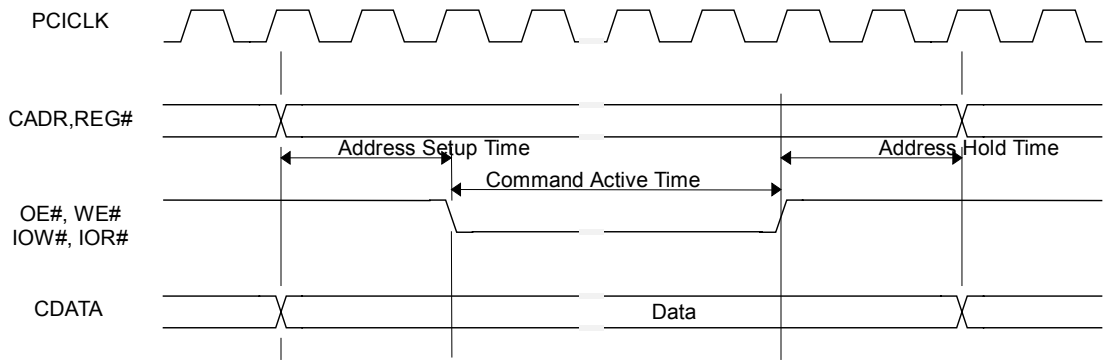
And also, the R5C551 will forward only write transaction to the VGA Palette register in the following ranges.

Palette address:	AD [9:0] = 3C6h, 3C8h, and 3C9h (Inclusive of ISA address aliases - AD [15:10] are not decoded.)

4.4 16-bit Card Interface Timing Control

The R5C551 generates the address, data, and command timing necessary to 16-bit Card interface. Each timing is set in a timer granularity of PCI clock as shown below. When 16-bit I/O enhanced Timing or 16-bit Memory Enhanced Timing bit in each socket control register space is cleared, the default timing is selected regardless of the I/O Win 0-1 Enhanced Timing bit or Memory Enhanced Timing bit. Default timing is selected when the value smaller than the minimum value is set.

16-bit Card Signal Timing Example



Symbol	Parameter	Min	Max	Default	Unit
	I/O Read/ Write				
Tsu	Address Setup Time	2	7	3	PCI Clocks (Typ=30ns)
Tpw	Command Active Time	3	31	6	PCI Clocks (Typ=30ns)
Thl	Address Hold Time	1	7	1	PCI Clocks (Typ=30ns)
	Memory Read/ Write				
Tsu	Address Setup Time	1	7	3 (4) Note 1	PCI Clocks (Typ=30ns)
Tpw	Command Active Time	3	31	6 (8or18) Note 2	PCI Clocks (Typ=30ns)
Thl	Address Hold Time	1	7	1(2) Note1	PCI Clocks (Typ=30ns)

Note1: 4(2) PCI clocks for 3.3v card attribute memory access.

Note2: 8 PCI clocks for 5v card attribute memory access.
18 PCI clocks for 3.3v card attribute memory access.

4.5 PCI Buffers

The R5C551 has data buffers, address buffers, and command buffers between the primary PCI bus and the secondary CardBus in order to maintain the high speed data transferring. An 8-DWORD buffer allows Posting Write Data and Prefetching Read Data from PCI bus to CardBus and a 10-DWORD buffer allows Posting Write Data and Prefetching Read Data from the CardBus to the PCI bus. Posting of write data is permitted when either Memory Write or Memory Write and Invalidate commands are used for transactions that cross the R5C551 in either direction. In other words, writing buffers are not available during the I/O Write and Configuration Write transactions. The R5C551 prefetche data when the transaction uses the Memory Read Line or Memory Read Multiple command. In addition, the R5C551 supports Prefetching Read Data from 1394 interface to PCI bus in order to maintain the high speed data transferring by PCI burst transfer.

4.6 Error Support

4.6.1 Parity Error

The R5C551 supports both parity generation and checking in both address and data phases on both the primary PCI bus and the secondary CardBus. The R5C551 asserts SERR# when an address parity error occurs during the bus transaction on either PCI bus or CardBus. When the R5C551 detect a data parity error, the bad data and bad parity are passed on to the opposite interface if possible and PERR# is asserted. This enable the parity error recovery mechanisms outlined in the PCI Local Bus Specification. If CSERR# is asserted on CardBus interface, the R5C551 forward a SERR# indication on the CardBus to the primary PCI bus.

4.6.2 Master Abort

When the master abort occurs at the destination, the R5C551 behaves in two ways. One is ISA compatible. (Return all ones during a read. The data will be discarded during a write.) The other way is to assert SERR#.

4.6.3 Target Abort

When the target abort occurs at the opposite side, the R5C551 communicates the error as a target abort to the origination master if possible. However, if cannot, the R5C551 assert SERR# and communicate the error to the system.

4.6.4 CardBus System Error

When CSERR# is asserted on the secondary CardBus interface, the R5C551 always asserts SERR# on the primary PCI interface and communicate the error to the system.

4.6.5 PCI Bus Error related to 1394 OHCI

In 1394 OHCI function, the R5C551 provides the occurrence of PCI bus error and the information to recover from PCI bus error to system software, Via Context register or descriptor etc,.

4.7 Interrupts

The R5C551 supports PCI interrupt signals INTA# and INTB# as well as ISA interrupt signals IRQn. They inform to the system the Card Status Change Interrupt as a card insert event, the Function Interrupt by the PC card, and also as the DMA Interrupt and the Device Interrupt defined on 1394 OHCI. INTA# is assigned to socket, and INTB# is assigned to 1394 OHCI. Interrupt of socket and 1394 can be reassigned by INT Select bit (bit1, 0) on the Misc Control 6 register.

INT Select		Slot	1394
bit1	bit0		
0	0	INTA#	INTB#
0	1	INTA#	INTB#
1	0	INTA#	INTA#
1	1	INTA#	INTA#

On PC Card, setting IRQ-ISA enable bit of the Bridge Control register enables the IRQn routing register for PC Card-16/32. On the other hand, clearing CINT-ISA Disable bit (Config.A0h bit6) enables the 32bit Function Interrupt to route into the ISA Interrupt. And also, setting the Card Status Change Interrupt Configuration register on the 16bit Control registers the 16bit Card Status Change Interrupt to route into the ISA Interrupt. But, the R5C551 doesn't support IRQ-ISA function on 1394 OHCI.

On 1394 OHCI, the interrupt signals inform to the host on the end of the DMA transaction. And they inform the interrupts from LINK layer and PHY layer. The IntEvent register and the IntMask register of the 1394 OHCI Registers control these interrupts. The IntEvent register indicates generation of an interrupt event and the IntMask register is used the selected interrupt to enable. Writing into the IntEventClear by software enables the interrupt to clear.

PCI interrupt signals are open drain outputs. IRQn pins are programmable to either positive edge mode or level mode. RI_OUT# can be reassigned as an interrupt signal for the purpose of the remote wakeup.

In addition to primary interrupt functions, the R5C551 supports Serialized IRQ. IRQ9 is reassigned as SRIRQ# by setting SRIRQ Enable bit on the Misc Control register. And LED# and LED1394# are also enabled.

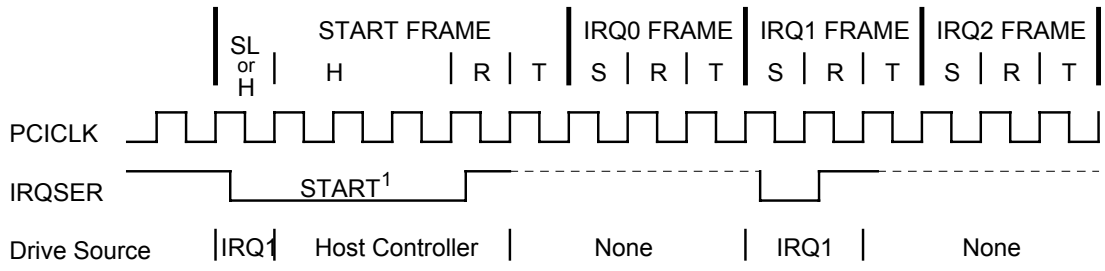
SRIRQ# (Serialized IRQ) output is a Wire-OR structure that simply passes the state of one or more device's IRQ to the host controller. The transfer can be initiated either by a device or by the host controller. A transfer, called an IRQSER Cycle, consists of three frame types: one Start Frame, several IRQ/Data Frames, and one Stop frame. When the SR_PCI_INT_Disable bit (bit5) on the Misc control register is 'Low', the frames of INTA#, INTB#, INTC#, and INTD# (PCI Interrupt signals) following IOCHK# frame are output. When it is 'High', SRIRQ# output only IRQx.

All cycle uses PCICLK as its clock source. There are two modes of operation for the IRQSER Start Frame: Quiet (Active) mode and Continuous (Idle) mode. In Quiet (Active) mode, any device can initiate a Start Frame. The R5C551 outputs 1PCICLK (Low) and Serialized IRQ is kept on Hi-Z during the rest of a Start Frame. After that, IRQ/DATA Frame is repeated.

In Continuous (Idle) mode, only Host Controller can initiate a Start Frame. The R5C551 becomes waiting state to detect 4-8 PCICLK of Start Pulse. These modes change automatically by monitoring the Stop pulse width in a Stop Frame. Quiet (Active) mode is repeated when width of Stop Pulse is 2PCICLK, and Continuous (Idle) mode is repeated when it is 3PCICLK. After assertion of the GBRST#, the default is Continuous (Idle) mode.

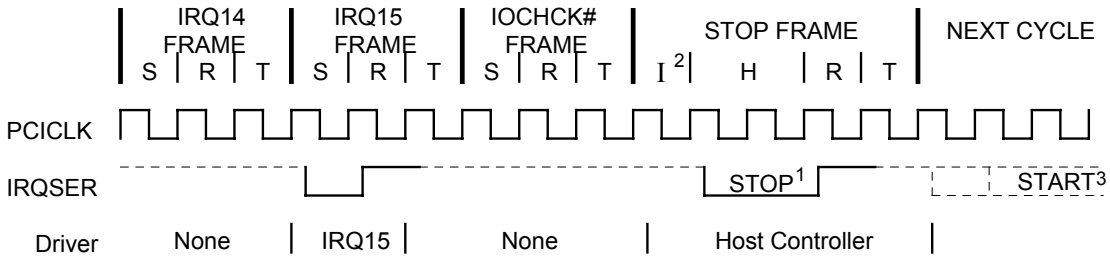
The Start Frame timing and the Stop Frame timing are as follows.

Start Frame timing with source sampled a low pulse on IRQ1



1. Start Frame pulse can be 4-8 clocks wide.

Stop Frame Timing with Host using 17 IRQSER sampling period



H=Host, SL=Slave Control, R=Recovery, T=Turn-around, S=Sample

1. Stop pulse is two clocks wide for Quiet mode, 3 clocks wide for Continuous mode.
2. There may be none, one or more Idle states during the Stop Frame.
3. The next IRQSER cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stop Frame.

IRQSER Sampling Periods		
IRQ/Data Frame	**Signal Sampled**	**# of clocks past Start**
1	IRQ0	2
2	IRQ1	5
3	SMI#	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47
17	IOCHCK#	50
18	INTA#	53
19	INTB#	56
20	INTC#	59
21	INTD#	62
32:22	Unassigned	95

4.8 Card Type Detection

If once a valid insertion is detected, the socket state machine of the R5C551 start to interrogate the PC Card to determine if it is a PC Card Standard or 16-bit PC Card. The R5C551 supports VCC values of 5V, 3.3V and combination of them at the socket interface. Card type can be known by reading the Socket Present State register.

CD2#	CD1#	VS2#	VS1#	Card Type		
				Key	Interface	Voltage
ground	ground	open	open	5V	16bit PC Card	5V
ground	ground	open	ground	5V	16bit PC Card	5V and 3.3V
ground	ground	ground	ground	5V	16bit PC Card	5V, 3.3V and X.XV
ground	ground	open	ground	LV	16bit PC Card	3.3V
ground	connect to CVS1	open	connect to CCD1#	LV	CardBus PC Card	3.3V
ground	ground	ground	ground	LV	16bit PC Card	3.3V and X.XV
connect to CVS2	ground	connect to CCD2#	ground	LV	CardBus PC Card	3.3V and X.XV
connect to CVS1	ground	ground	connect to CCD2#	LV	CardBus PC Card	3.3V, X.XV and X.XV
ground	ground	ground	open	LV	16bit PC Card	X.XV
connect to CVS2	ground	connect to CCD2#	open	LV	CardBus PC Card	X.XV
ground	connect to CVS2	connect to CCD1#	open	LV	CardBus PC Card	X.XV and Y.YV
connect to CVS1	ground	open	connect to CCD2#	LV	CardBus PC Card	Y.YV
ground	connect to CVS1	ground	connect to CCD1#	reserved		
ground	connect to CVS2	connect to CDD1#	ground	reserved		

4.9 Mixed Voltage Operation

The R5C551 has 4 independent power nets. The PC card interface of the R5C551 is powered at 5V or 3.3V. This mechanism allows the R5C551 to maintain the backward compatibility with PCMCIA2.1 compliant cards (R2 card). Each of the power for PCI I/O (VCC_PCI3V) and Card Slot I/O (VCC_3V) are fixed at 3.3V. But the R5C551 is enabled to support either 3.3V or 5V without external level shifters, because the R5C551's interface has the structure of 5V tolerant. The core logic power is fixed at 1.8V or 2.5V and VCC_3V and AVCC_PHY3V are fixed at 3.3V.

4.10 Reset Event

Anytime GBRST# is asserted, all R5C551 internal state machines are reset and all registers are set to their default values (If each signals have followed the reset sequence below). PCIRST# is asserted, all registers are set to their default value except the following registers. The default values of each register are described in each register description.

1. These registers are initialized only by GBRST#, not by PCIRST#. (PCI RESET Resistant register).

PCI-CardBus Bridge Config. Space:

· 40h	Subsystem Vendor ID	[15:0]
· 42h	Subsystem ID	[15:0]
· 80h	Bridge Configuration	[15:0]
· 82h	Misc Control	[15:0]
· 84h	16-bit Interface Control	[15:0]
· 88h	16-bit I/O Timing 0	[15:0]
· 8Ah	16-bit Memory Timing 0	[15:0]
· A0h	Misc Control 2	[15:0]
· A2h	Misc Control 3	[15:0]
· A4h	Misc Control 4	[31:0]
· C0h	Writable Subsystem Vendor ID	[15:0]
· C2h	Writable Subsystem ID	[15:0]

1394 OHCI-LINK Config. Space:

· 2Ch	Subsystem Vendor ID	[15:0]
· 2Eh	Subsystem ID	[15:0]
· 3Eh	MIN Grant & MAX Latency	[15:0]
· ACh	Writable Subsystem Vendor ID	[15:0]
· AEh	Writable Subsystem ID	[15:0]
· 80h	Misc Control 5	[15:0]
· 9Ch	Misc Control 6	[7:0]
· 9Eh	Misc Control 7	[7:0]
· BEh	Writable MIN_GNT & MAX_LAT	[15:0]
· 98h	PHY Power Management	[7:0]
· 99h	PHY Shadow	[7:0]

1394 OHCI Register:

· 24h	Global Unique ID High	[31:0]
· 28h	Global Unique ID Low	[31:0]

1394 PHY Register:

·All Registers

2. These registers are not initialized by PCIRST# when the power state is D3 and PME Enable bit is set to ”1”. (PME_Context register)

PCI-CardBus Bridge Config. Space:

· 000h	Socket Event	[3:0]
· 004h	Socket Mask	[3:0]
· 008h	Socket Present State	[11,10,5,4]
· 010h	Socket Control	[6:4]
· 802h	Power Control	[7:2]
· 804h	Card Status Change	[3:0]
· 805h	Card Status Change interrupt Configuration	[3:0]
· 82Fh	Misc Control 1	[0]
· 0DEh	Power Management Capabilities	[15]
· 0E0h	Power Management Control/ Status	[15,8]

1394 OHCI Register:

· 0DEh	Power Management Capabilities	[15]
· 0E0h	Power Management Control/ Status	[15,8]

3. Excepting the above registers (PCI RESET Resistant register, PME_Context register), all the registers are initialized by the power state transition from D3 to D0 as long as the power state is D3.

≡Reset Sequence≡

Follow the sequence for initialization when a power is on.

1. Supply a power to VCC_CORE18V and VCC_3V, and AVCC_PHY3V.
2. Supply a power to VCC_PCI3V.
3. Deassert GBRST#.
4. Deassert HWSPND#. (when HWSPND# is asserted.)
5. Deassert PCIRST#. (PCLK has to be supplied for 100µsec@33MHz before deasserting PCIRST#.)

Following Step3 by Step2 has no problem.

See the timing a detail of the timing shown in the Chapter 10.3.6.

4.11 Power Management

The R5C551 implements two kinds of power management, software suspend mode and hardware suspend mode, in order to reduce the power dissipation on the suspend, in addition to the adoption of circuit to reduce the power consumption when power on. The software suspend mode conforms to the ACPI (Advanced Configuration and Power Interface) specification and the PCI Bus Power Management Standard. The R5C551, as a PCI device, implements four power states of D0, D1, D2, and D3. Each power states are the following on PC Card and 1394 OHCI-LINK. And also, PHY is enabled to change to the low power mode according to the power states of OHCI-LINK.
The power management events for the R5C551 and their sources are listed below. When the power state is except D0, the interrupt is disabled and only PME# is enabled to assert.

Event	Source
Card Detect Change	R5C551
Ready/Busy change	card
Battery Warning	card
Ring Indicate (Card Status Change)	card
1394 LINKON	R5C551

4.11.1 Function on PC Card

D0	the maximum powered state. All PCI transactions are acceptable.
D1	Only the PCI Configuration Space access is allowed while the power and clock are provided. CardBus CLK is output.
D2	Only the PCI Configuration Space access is allowed while the power and clock are provided. CardBus CLK is stopped by the protocol of CLKRUN.
D3hot	Only the PCI Configuration Space access is allowed while the power and clock are provided. CardBus CLK is stopped compulsorily. If CardBus card is inserted, CardBus RESET# is asserted at the same time this state is set. When the function is brought back to the D0 state, the reset is automatically performed regardless of the assertion of PCIRST#. PCI interface is disabled when reset. CardBus interface is reset by the assertion of CRST# on CardBus card or RESET on 16bit card.
D3cold	PCI-CardBus Bridge defines D3cold state is to change from Vcc to the auxiliary power source. The R5C551 supports power management events from D3cold with the auxiliary power source. The R5C551 can generate PME# even in D3cold state without PCI clock if the event source is Card Detect Change or Ring Indicate.

In the software suspend mode, when the card is inserted, the interface signals on sockets are kept to the following levels.

CardBus: CCLK=low, CPAR=low, CAD=high or low, CCBE#=high or low, CRST#=low, CGNT#=high, pull-up=H, pull-down=L

16-bit : CDATA=hi-z, CADR=low
Other pins keep the level before the software suspend mode.

In addition to the Operating system-directed power management like ACPI, the R5C551 supports CLKRUN# and CCLKRUN# protocol and it results in a clock stopped and a slow clock. Therefore, it is possible to reduce the power consumption. The state of the card interface signals is the same as the software suspend mode. The hardware suspend mode is enabled if HWSPND# is asserted. Once HWSPND# is asserted, all PCI bus interface signals are disabled, and VCC_PCI3V can be powered off. PCIRST# is not accepted as long as HWSPND# is asserted low.

4.11.2 Function on 1394 OHCI-LINK/1394 PHY

D0	Fully functional OHCI device state. Unmask interrupt events generate INTx#. PME_STS is set and PME# also be generated when PME_EN is enabled.
D1	Ack_tardy is returned on accesses from 1394. The PCI configuration space, the 1394 OHCI register and the GUID register are preserved. Functional interrupts are masked. Unmask interrupt event sets PME_STS and PME# is generated when PME_EN is enabled. All transmit contexts must be inactive before it attempts to place the R5C551 into the D1 power state. IEEE1394 bus manager shall not be placed into D1. Placing the R5C551 into D1 enables the ack_tardy generation. Software must ensure that IntEve.ack_tardy is zero and should unmask wake-up interrupt events such as IntEvent.phy and IntEvent.ack_tardy before placing the R5C551 into D1.
D2	LPS is deasserted and stopping supply of SCLK is requested to PHY. The PCI configuration space is retained and capable of access. The GUID register is retained, but the1394 OHCI register is lost. Functional interrupts are masked. But when the LinkOn signal that is occurred by accepting LinkOn packet or PHY.INTERRUPT is accepted from PHY, PME_STS is set and PME# is generated when PME_EN is enabled.
D3hot	LPS is deasserted and stopping supply of SCLK is requested to PHY. The PCI configuration Space is capable of access, but all register except the PME context is lost. The GUID register is retained, but the1394 OHCI register is lost. On transitioning back to D0, the internal reset is automatically done even if PCIRST# is not asserted. Functional interrupts are masked. But when the LinkOn signal is accepted from PHY, PME_STS is set and PME# is generated when PME_EN is enabled.
D3cold	D3cold indicates the state that Vcc is changed to the auxiliary power on D3hot state. D3cold supports functions like D3hot's.

PHY function

On D2 and D3 states, it is possible to set PHY to the following low power consumption mode by Software.

	Doze Mode	Sleep Mode
Select Condition (*1)	All of Ports status is set to Disconnected, Disabled or Suspended.	
Resume Time	less than 200ns	less than 10ms

*1: Setting D2ForcePM bit or D3PhyPM bit ignore these Select Conditions.

Doze Mode: Stopping clock of PHY digital block and Getting the Cable Interface's power down enables the power consumption to be low.

Sleep Mode: Disabling the function of PLL and Oscillator enables the power consumption to be lower than on Doze mode.

Setting D2PhyPM bit or D3PhyPM bit on the PHY Power Management register (1394 PCI Configuration register addr.98h) enables to a selection of Doze mode or Sleep. On Doze mode or Sleep mode, LinkOn event enables to resume from the power consumption mode automatically and PME# is asserted.

Each power consumption modes cannot be set without being concluded above selected conditions, even if the R5C551 is set to D2 state or D3 state.

If above Ports conditions are not satisfied, the R5C551 transacts as the Repeater PHY. In this time, setting D2ForcePM bit or D3ForcePM bit to 1b enables to ignore above conditions and to set Doze mode or Sleep mode automatically. But, it is disabled LinkOn event to resume from the power consumption mode automatically and to assert PME#. Writing into Power State bits enables to return to D0 state.

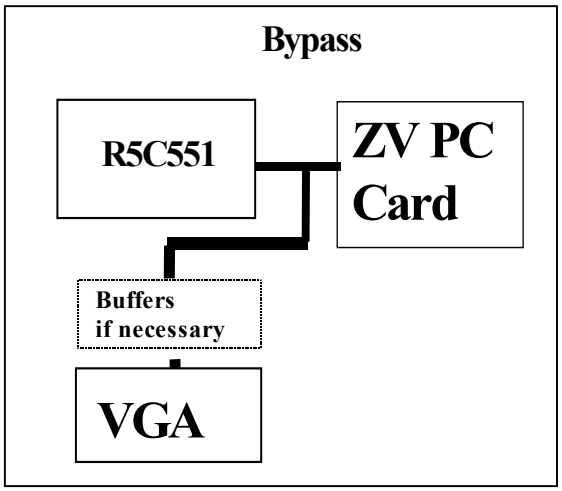
In addition, please don't cut off a power source of AVCC_PHY3V on the suspend mode.

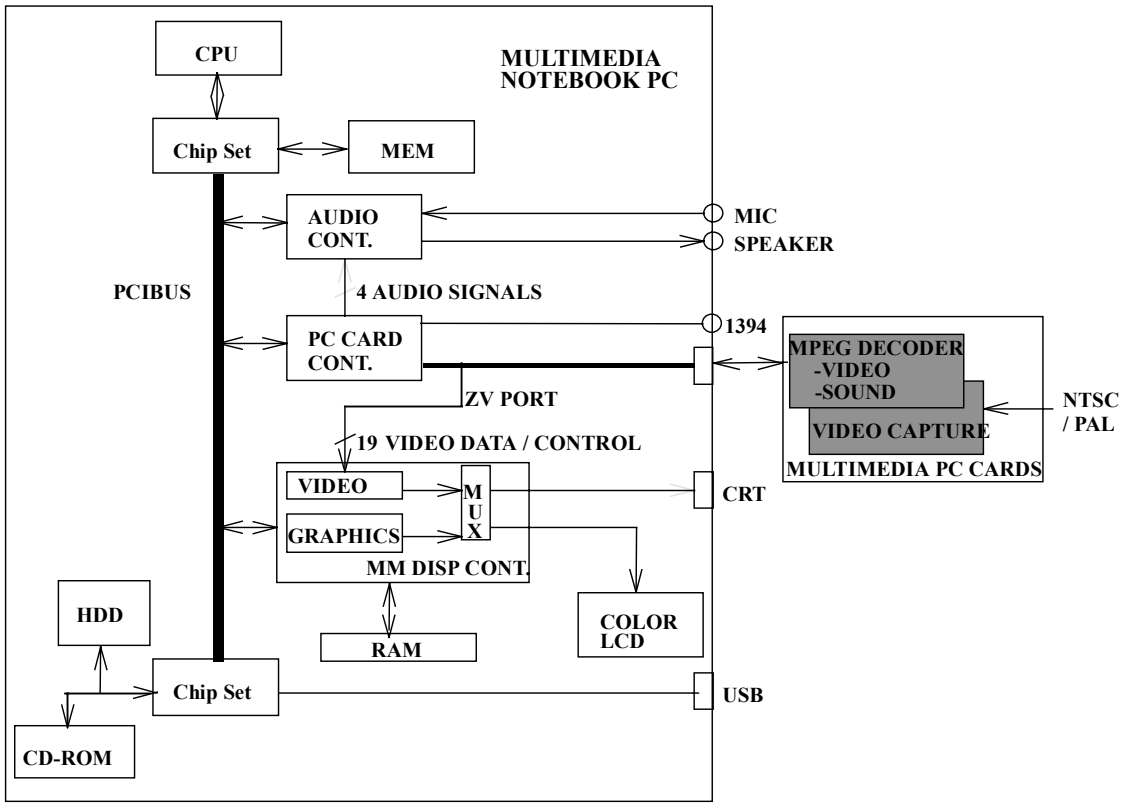
4.12 GPIO

IRQ3, 4, 5 and 7 pins work as GPIO (General Purpose I/O) pin when GPIO Enable bit of the Misc Control 4 register (A4h bit31) is set to one on Serialized IRQ mode or on Multi_IRQ mode of the Misc Control 4 register. When GPIO Enable bit is set to zero, GPIO outputs are Hi-Z and GPIO Inputs are disabled. User can change GPIO pins to either Input or Output by setting either I/O control bits on GPIO register (83Ah) or General Purpose I/O register of the Config register space (AAh). When GPIO Enable bit is set to one, setting of GPIO is input mode (default). And it is possible to read the states of their pins from each bit of the GPIO register. On Output mode, the written states of each bit are output. If GPIO functions are not used on Serialized IRQ mode, no pull-up is required.

4.13 ZV port Interface

The R5C551 has Bypass type ZV port interface. On 16-bit interface, when ZV port Enable bit of either Misc Control 1 (82Fh) or Misc Control 2 (A0h) is enabled, CADR [25:6], IOIS16#, INPACK#, SPKR# are assigned to ZV port input signal as shown in the below diagram.
The R5C551 has no on chip buffer for ZV port interface. So if ZV port is enabled, the signals for ZV port such as CADR [25:4] will be "Hi-Z" or "Input disable" and will be reconfigured as ZV port interface. The R5C551 outputs the control signal for the external buffer. Therefor, the buffer control to switch sockets is enabled.





16 bit interface Signal Name	ZV Port Interface Signal Name	ZV Port card I/O [1]	Comments
A10	**HREF**	O	Horizontal Sync to ZV Port
A11	**VSYNC**	O	Vertical Sync to ZV Port
A9	**Y0**	O	Video Data to ZV Port YUV:4:2:2 format
A8	**Y2**	O	Video Data to ZV Port YUV:4:2:2 format
A13	**Y4**	O	Video Data to ZV Port YUV:4:2:2 format
A14	**Y6**	O	Video Data to ZV Port YUV:4:2:2 format
A16	**UV2**	O	Video Data to ZV Port YUV:4:2:2 format
A15	**UV4**	O	Video Data to ZV Port YUV:4:2:2 format
A12	**UV6**	O	Video Data to ZV Port YUV:4:2:2 format
A7	**SCLK**	O	Audio SCLK PCM Signal
A6	**MCLK**	O	Audio MCLK PCM Signal
A[5::4]	**RESERVED**	RFU	Put in three state by Host Adapter No connection in PC Card
A[3::0]	**ADDRESS[3::0]**	I	Used for accessing PC Card
IOIS16#	**PCLK**	O	Pixel Clock to ZV Port
A17	**Y1**	O	Video Data to ZV Port YUV:4:2:2 format
A18	**Y3**	O	Video Data to ZV Port YUV:4:2:2 format
A19	**Y5**	O	Video Data to ZV Port YUV:4:2:2 format
A20	**Y7**	O	Video Data to ZV Port YUV:4:2:2 format
A21	**UV0**	O	Video Data to ZV Port YUV:4:2:2 format
A22	**UV1**	O	Video Data to ZV Port YUV:4:2:2 format
A23	**UV3**	O	Video Data to ZV Port YUV:4:2:2 format
A24	**UV5**	O	Video Data to ZV Port YUV:4:2:2 format
A25	**UV7**	O	Video Data to ZV Port YUV:4:2:2 format
INPACK#	**LRCLK**	O	Audio LRCLK PCM signal
SPKR#	**SDATA**	O	Audio PCM Data signal

ZV Port Interface Pin Assignments

1. "I" indicates signal is input to PC Card, "O" indicates signal is output from PC Card.

4.14 Subsystem ID, Subsystem Vendor ID

The R5C551 supports Subsystem ID and Subsystem Vendor ID to meet PC98/99/2001 Design Requirements. There are three ways to write into Subsystem ID register and Subsystem Vendor ID register from the system through BIOS.

1. Write Enable bit (Card: Misc Control bit6, 1394:Misc Control 6 bit4) control method.
   The BIOS can turn this bit on, change the Subsystem IDs, and turn it off.
2. Copy of the Subsystem ID and the Subsystem Vendor ID in PCI user defined space (Card: C0h, 1394:ACh) method.
3. Load the Subsystem IDs from the Serial ROM method.
   Connecting SPKROUT to pull-down enables to use the Serial ROM. The R5C551 has the Serial ROM interface, and load the Subsystem ID and the Subsystem Vendor ID after PCI reset disabled.

This register is initialized only by GBRST#.

4.15 Power Up/Down Sequence

Sustain to the following sequence when the power sequence is ON/OFF.

* On the power sequence is ON.
    1. Supply to VCC_CORE18V.
    2. Supply to VCC_3V, AVCC_PHY3V
    3. Supply to VCC_PCI3V.
* On the power sequence is OFF.
    1. Stop supplying to VCC_PCI3V.
    2. Stop supplying to VCC_3V, AVCC_PHY3V.
    3. Stop supplying to VCC_CORE18V.

On the power sequence is on, sustain timing of Global Reset (Chapter 10.3.6) in regards to the control of HWSPND# and GBRST#. Specially, asserting GBRST# enables to supply power to AVCC_PHY3V, because the only GBRST# enables to initialize Cable interface. Also, it is necessary to do rising of VCC_PCI3V power within asserting times of HWSPND#.

On the power sequence is off, a special limit for Delay Time is none.

If only PHY is operated as Repeater, sustain to the following power sequence.

* On the power sequence is ON.
    1. Supply to VCC_CORE18V.
    2. Supply to VCC_3V, AVCC_PHY3V.
* On the power sequence is OFF.
    1. Stop supplying to VCC_3V, AVCC_PHY3V.
    2. Stop supplying to VCC_CORE18V.

In this case also, a special limit for Delay Time is none on the power sequence is off. It is not necessary to supply VCC_PCI3V. But, sustain the following notes if these pins are used.

a. Asseritng GBRST# enables to supply power to AVCC_PHY3V, because the only GBRST# enables to initialize Cable interface. Also, sustain the delay time shown in the chapter 10.3.6 on use of GBRST#. It is not necessary to control PCIRST#.

b. HWSPND# is always set to ‘Low’.

4.16 1394 OHCI

The 1394 OHCI in the R5C551 employs DMA engines for high-performance data transfer, host bus interface and FIFO. The R5C551 supports two types of data transfer: asynchronous and isochronous. See the 1394 OHCI release 1.1/1.0 specifications with regard to detailed settings and procedures for the controller.

4.16.1 Asynchronous functions

The R5C551 supports all of transmission and reception defined in 1394 packet formats. Transmitted Packets are read out of host memory and received packets are written into host memory, both using DMA. And also, the R5C551 can be programmed to act as a bus bridge between host bus and 1394 by directly executing 1394 read and write requests as reads and writes to host bus memory space.

4.16.2 Isochronous functions

The R5C551 includes the cycle master function as defined by the 1394 specification. The cycle start packet is transferred at intervals of 8KHz cycle clock. This cycle master uses the internal cycle clock. When the R5C551 is not the cycle master, the R5C551 sustains its internal cycle timer sychronized with the cycle master node by correcting its own cycle timer with the reload value from the cycle start packet.
The R5C551 supports one DMA controller each for isochronous transmit and isochronous receive. Each DMA controller supports 4 different DMA contexts.

4.16.3 DMA

The R5C551 supports seven types of DMA. Each type of DMA has register space and data stream referred to as a DMA context.

DMA Type	Number of Contexts
Asynchronous Transmit	Request x 1, Response x 1
Asynchronous Receive	Request x 1, Response x 1
Isochronous Transmit	x 4
Isochronous Receive	x 4
Self-ID Receive	x 1
Physical Request & Physical Response	No Context

Each asynchronous and isochronous context is comprised of a buffer descriptor list called a DMA context program, stored in main memory. The DMA controller finds the necessary data buffers through the DMA context programs.
The Self-ID receive controller is controlled not by the DMA context program but by the two other registers. The R5C551 supports the Physical Request DMA and the Physical Response DMA controllers to transmit receive requests that reads and writes directly to host bus memory space. These controllers are also controlled not by the DMA context program but by the other register.

4.16.4 LINK

The Link module sends packets which appear at the transmit FIFO interfaces to PHY, and places correctly addressed packets into the receive FIFO. The features are as follows.

- Transmits and receives correctly formatted 1394 serial bus packets.
- Generates the appropriate acknowledge for all received asynchronous packets.
- Performs the function of cycle master.
- Generates and checks 32-bit CRC.
- Detects missing cycle start packets.
- Interfaces to PHY.
- Receives isochronous packets at all times (Supports of asynchronous streams and cycle start packets including a CRC error).
- Ignores asynchronous packets received during the isochronous phase.

4.17 Serial ROM Interface

The R5C551 can load data for Subsystem ID/Subsystem Vendor ID (PCI Interface) and GUID (OHCI) from Serial ROM (I^2C BUS).

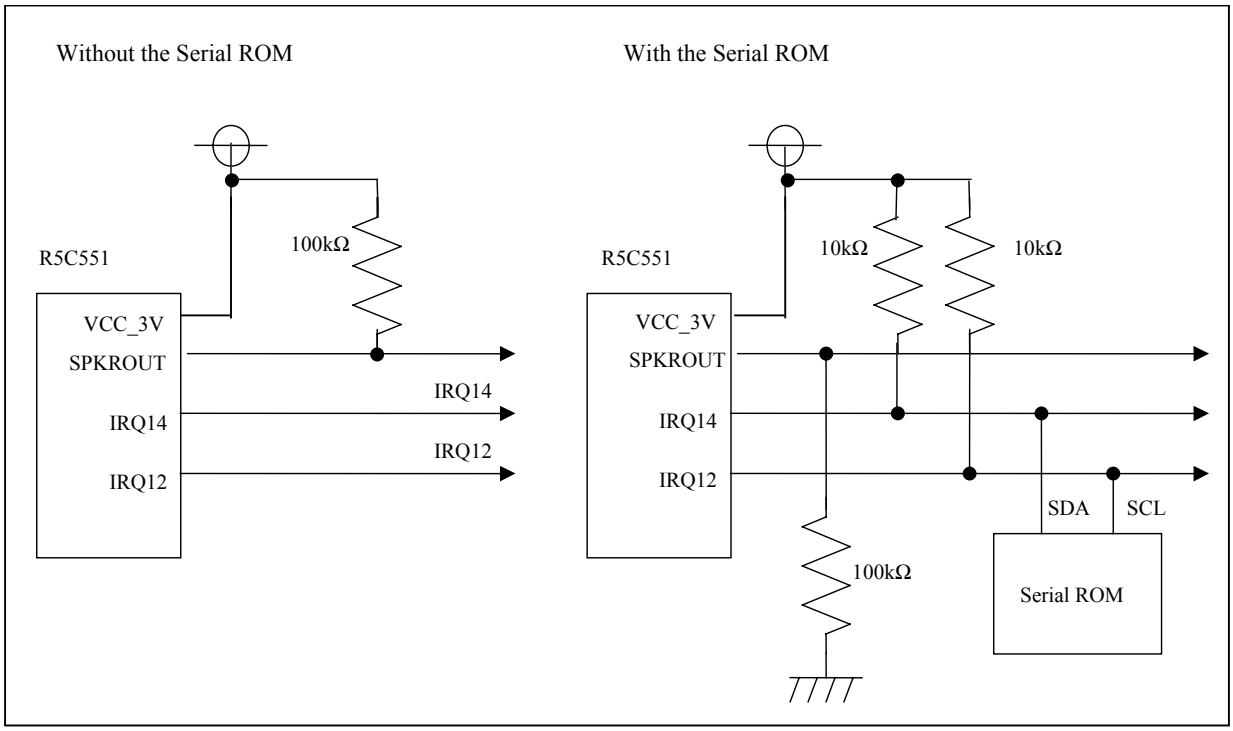
* 「I^2C BUS」is registered trademark of PHILIPS ELECTRONICS N.V.
  Purchase of Ricoh's I^2C components conveys a license under the Philips I^2C patent to use the components of the I^2C system, provided the system conforms to the I^2C specifications defined by Philips.

4.17.1 Outline

The R5C551 supports 100K mode and 7-bit address, and automatically stores the data (See. 4.17.3) from the Serial ROM when the first PCI Reset is deasserted after deassertion of the GBRST#.

4.17.2 User's setting

Connecting SPKROUT pin to pull-down resistor of 100kΩ enables to use the Serial ROM. When the first PCI Reset is deasserted, the R5C551 starts to sample SPKROUT pin. When SPKROUT pin is connected to pull-down resistor of 100kΩ, the R5C551 attempts to load data through the Serial ROM. In this case, IRQ12 is reaasigned to SCL (Clock signal) and IRQ14 is reassigned to SDA (Data signal). SDA (Data signal) and SCL (Clock signal) must be connected to VCC_3V through pull-up resistor of 10kΩ.
When SPKROUT pin is connected to VCC_3V through pull-up resistor of 100 kΩ, the R5C551 does not load data through the Serial ROM. In this case, the function of IRQ12 and IRQ14 depends on setting of the Misc Control 4 register (See 5.4.34).



4.17.3 Format

The R5C551 has access to the Serial ROM by PCI Reset after detecting of Serial ROM. The accessed data is loaded to each register as follows. The retry states don't allow PCI's slave access during access to Serial ROM.
Each parts register of 1394OHCI-LINK Configuration Space, 1394 OHCI Register and PCI-CARDBUS Bridge Configuration Space are used to store. Setting bit 7 of the Serial ROM address 25h enables to store to PCI-CARDBUS Bridge Configuration Space.

4.17.3.1 1394OHCI-LINK Configuration Space

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	Subsystem Vendor ID [7:0]							
01h	Subsystem Vendor ID [15:8]							
02h	Subsystem ID [7:0]							
03h	Subsystem ID [15:8]							
04h	LEDRX [1]	LEDRX [0]	LEDTX [1]	LEDTX [0]	-	-	-	-
05h	OHCI10	-	-	-	-	-	-	-
06h	Reserved							
07h	Reserved							
08h	Reserved							
09h	Reserved							
0Ah	Reserved							
0Bh	Reserved							
0Ch	Reserved							
0Dh	Reserved							
0Eh	Reserved							
0Fh	Reserved							
10h	Reserved							
11h	Reserved							
12h	Reserved							
13h	Reserved							
14h	Reserved							
15h	Reserved							
16h	Reserved							
17h	Reserved							
18h	Reserved							
19h	Reserved							
1Ah	Reserved							
1Bh	Reserved							
1Ch	D2PhyPM		D2ForcePM	D3PhyPM		D3ForcePM	CPSDis	CPSFixVal
1Dh	CMC Shadow	PrwCShadow			P0Dis Shadow	P1Dis Shadow	-	-
1Eh	Reserved							
1Fh	Reserved							
20h	Reserved			SIDWREN	PMbit15 WrEn	Reserved	INTXSel	
21h	Reserved							
22h	Reserved				LEDtoCB	Reserved		
23h	Reserved							
24h	Max Latency [3:0]				Min Grant [3:0]			
25h	Cardbus Load	-	-	-	-	-	-	-

4.17.3.2 1394 OHCI Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
26h	ProgPhyEn	aPhy EnhanceEn	-	-	-	-	-	-
27h	MiniROM Address [7:0]							
28h	Config ROM Header [7:0]							
29h	Config ROM Header [15:8]							
2Ah	Config ROM Header [23:16]							
2Bh	Config ROM Header [31:24]							
2Ch	Bus Option [7:0]							
2Dh	Bus Option [15:8]							
2Eh	Bus Option [23:16]							
2Fh	Bus Option [31:24]							
30h	Global Unique ID High [7:0]							
31h	Global Unique ID High [15:8]							
32h	Global Unique ID High [23:16]							
33h	Global Unique ID High [31:24]							
34h	Global Unique ID Low [7:0]							
35h	Global Unique ID Low [15:8]							
36h	Global Unique ID Low [23:16]							
37h	Global Unique ID Low [31:24]							

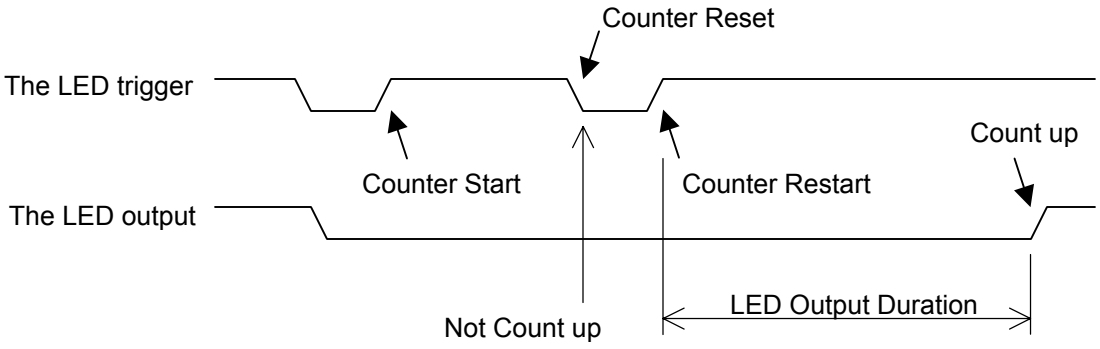
4.17.3.3 PCI-CARDBUS Bridge Configuration

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
38h	Subsystem Vendor ID [7:0]							
39h	Subsystem Vendor ID [15:8]							
3Ah	Subsystem ID [7:0]							
3Bh	Subsystem ID [15:8]							
3Ch	IOMinTim	MemMinTim	16bitMem EnhTim	16bitIOEnh Tim	LegacyIdx Sel	PrefetchEn	I/O1Adr Mode	I/O0Adr Mode
3Dh	SIRQEn	-	SR_PCIINT Dis	-	LEDPol	5VDis	VPPENPol	VCCxENPol
3Eh	CmdPlsWdt(I/O)				-	AdrSetupTim (I/O)		
3Fh	-	-	-	AdrHoldTim (I/O)			-	CmdPlsWdt
40h	CmdPlsWdt (Mem)				-	AdrSetupTim (Mem)		
41h	AWPPUP Dis	ARESET PUPEn	-	AdrHoldTim (Mem)			-	CmdPlsWdt
42h	Reserved							
43h	CSCtoINT Dis	CINT-ISADis	-	StopClock Dis	LEDtoOther	RI_OUT#	CSTSCHG InEn	WaitSel
44h	Reserved			DecodeDis	SPKROUT HiZEn	DelatedClr Dis	CBCLK RUNDis	5VReadEn
45h	Reserved							
46h	Multi_IRQ5		Multi_IRQ4			Multi_IRQ3		
47h	Multi_ IRQ10	Multi_IRQ9			Multi_IRQ7			Multi_IRQ5
48h	Multi_IRQ12			Multi_IRQ11			Multi_IRQ10	
49h	GPIOEn	Reserved	Multi_IRQ15			Multi_IRQ14		

4.18 LED# Output

The R5C551 enables to output the activity signals of the PC card and the 1394OHCI, as LED# and LED1394#. The R5C551 uses IRQn pins as LEDA# and LED1394#. Refer to the Misc Control 4 (Config. (func.0) A4h) register as for how to use these pins. The default of the LED signal is 'Low' active. But it is possible to set the LED signal to 'high' active by setting the LED Polarity bit (Config, (func.0) 82h bit11) to 1b. This bit is common to the card and the 1394 OHCI.

The LED signal is asserted at the same time the trigger of its signal is asserted. And the internal counter works after the trigger is deasserted. In default, the LED signal is kept for 64msec after the deassertion of the trigger, and is deasserted. When the trigger is reasserted on work of the counter, the counter is cleared and restarted to count up at the same time the deassertion of the LED signal. See as follows.



The LED Output Duration is selected from among 64msec(default), 1msec and No Duration Time (through the trigger). The card and the 1394 have the different registers for selecting each other (See as follows). The trigger signals for them also are different.

PCLK has operated a counter used for the LED Output Duration and therefore a stop request of PCLK by Clock_run protocol is refused while the counter is worked. When PCLK must be stopped during 64msec on system, change the LED Output Duration.

4.18.1 PC Card LED (CardBus R2)

The trigger signals of the PC Card LED are as follows.

CardBus : CFRAM#, CINT#
R2 : Card command by IORD#, IOWR#, OE#, WE#, IREQ#

Bit 13 and bit 12 of the Config (func.0) A2h register enable to set the counter's hold time.
(These bits are set as the Ricoh Purpose register.)

bit 13 12	the LED Output Duration
0 0	64 msec (default)
1 1	1 msec
1 0	No Duration Time (through)
0 1	Test Mode (3.8µsec)

4.18.2 1394 LED

The 1394 LED signal indicates the condition of the IEEE1394 interface block in the R5C551. This signal is asserted when the R5C551 is on transmission/reception.

Bit 2 and bit 1 of the Config (func.1) 9Eh register enable to set the counter's hold time. (These bits are set as the Ricoh Purpose register.)

bit 2 1	the LED Output Duration
0 0	64 msec (default)
1 1	1 msec
1 0	No Duration Time (through)
0 1	Test Mode (3.8µsec)

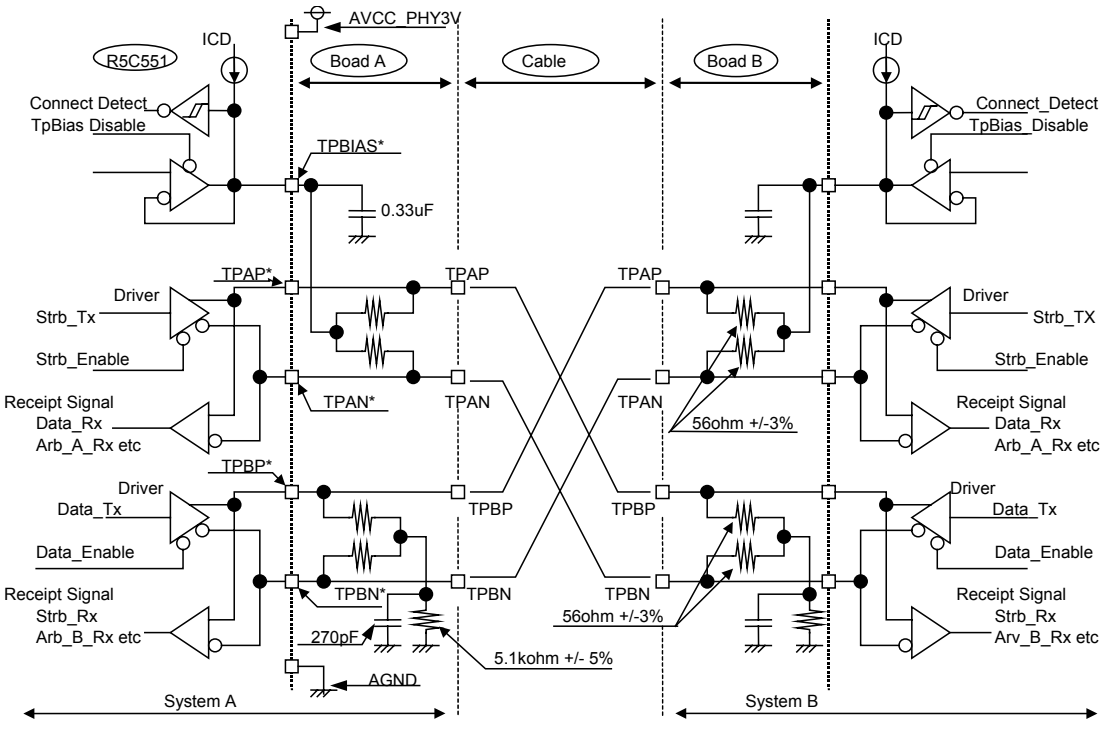
4.18.3 LED Output Selection

Setting Config (func.2) 9Eh bit3 to '1' enables to output LED on 1394 to LED#. The combination of these bits enables to output all LED to LED#.

4.19 1394 Cable Interface

The R5C551 builds in two ports of 1394 Cable interface which support the transmission speed of 400/200/100Mbps compliant with IEEE 1394-1995 and IEEE-1394a-2000 standard.

4.19.1 Cable Interface Circuit



* mark means a port number in this figure.
(Example: TPBIAS*→TPBIAS0 or TPBIAS1)

Each port consists of two twist-pairs; TPA and TPB. TPA/TPB is used for the monitoring transmission/reception of a control signal (Arbitration signal) and data, and the state of a cable line (the insert of a cable).

On both TPA and TPB, it is necessary to connect with a termination of 56Ω resistance according to the cable impedance. This termination resistance should be arranged near the R5C551. On TPA side, TPBIAS should be connected to the center node of the termination resistance in order to set up a cable's common-mode DC potential. A capacitor of 0.33μF for decoupling should be connected to the TPBIAS. On TPB side, a termination of 5.1kΩ and a capacitor of 270pF should be connected to between the center node of the termination resistance and AGND. Please refer to an application manual about a substrate layout.

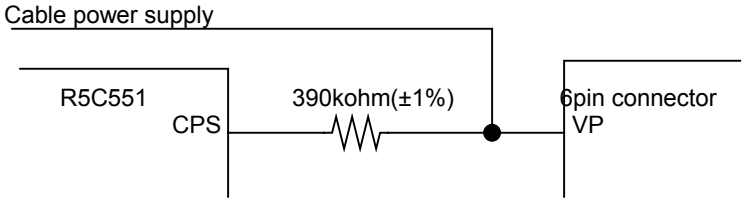
4.19.2 Transaction of Unused ports

On no use of ports, TPBP* and TPBN* are directly connected to AGND, and TPAP*, TPAN* and TPBIAS* are OPEN. Further, set Port Disable bit of the 1394 PHY Register (see the chapter 8.3.1). Port Disable bit can be set also by the PHY Shadow register of the 1394 Configuration registers space (the chapter 5.5.20). Please refer to the Read/Write of the 1394PHY register (the chapter 4.19.4).

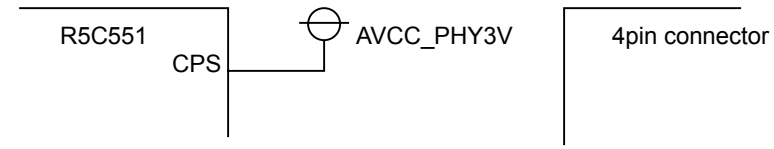
4.19.3 CPS (Cable Power State)

The R5C551 builds in a function monitoring the state of cable power. The CPS pin is connected to cable power through the external resistor (390kΩ±1%) and detects a condition that cable power has lowered below the threshold level (generally 7.5V). When the four pins cable is used (when the CPS function is not used), it is enabled to select two methods: one is connection of the CPS pin with AVCC_PHY3V directly, and the other is control of the CPS by register with the CPS pin open. In case of control by the register, please set CPSDis (bit1) and CPSFixVal (bit0) on the PHY Power Management Register (AddressOffset 98h) of the 1394 Configuration Register space to 1b. These registers can be set also by the Serial ROM. Please refer to the Serial ROM (Chapter 4.17) for details.

On monitoring the state of Cable Power.



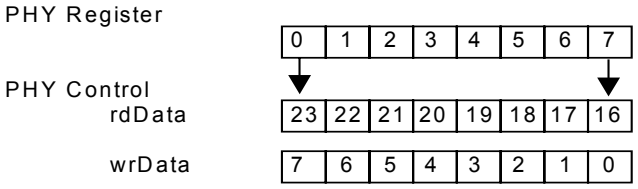
Out of monitoring the state of Cable Power.



4.19.4 Read/Write of 1394 PHY Registers

The R5C551 builds in the 1394 PHY registers compliant with IEEE 1394-1995 and IEEE1394a-2000 standard. Please refer to the 1394PHY Registers (Chapter 8) for details. Access to these registers is enabled by the PHY Control register (Chapter 9.4.24) of the 1394 OHCI Registers, and Access to the PHY Control register (AddressOffset 0ECh) is enabled by offsetting [31-11] bits of the 1394 OHCI Register Base Address (AddressOffset 10h) in the 1394 Configuration register space.

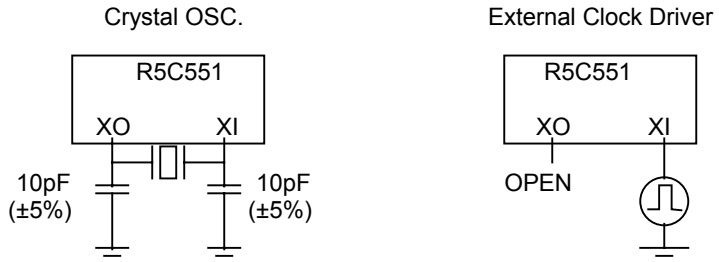
The data of 1394 PHY register is little endian description. Since it is changed into a big endian from a little endian within R5C551 when accessing from PHY Control register, it cannot care about the bit number of data, but data can be dealt with only in a row.



For example, when 53h is written in wrData of PHY Control register (bit 6, 4, 1, and 0 are set to 1), 53h is written in PHY Register as they are (bit 1, 3, 6, and 7 are set to 1). Access to Contender bit, Power_class field, and Disable bit of Port0/Port1 of the 1394 PHY register is enabled through the PHY Shadow register (AddressOffset 99h) of 1394 configuration register space. Please refer to Chapter 5.5.20 about PHY Shadow register.

4.19.5 Clock Circuit

The PHY block of the R5C551 requires 24.576MHz of clock frequency.



Recommended Conditions

Crystal Oscillator

Normal Frequency	: 24.576MHz
Frequency Tolerance	: ±50ppm(at25°C)
Temperature stability	: ±50ppm(reference to 25°C)
Operating Temperature Range	: -20~70°C
Load Capacitance	: 10pF
Driver Level	: 0.1mW
Equivalent Series Resistance	: 50ohms Max
Insulation resistance	: 500M ohm Min (at DC100V±15V)
Shunt Capacitance	: 7.0pF Max

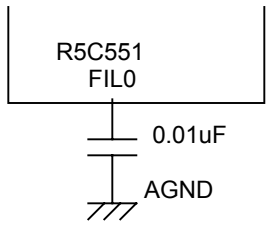
External Clock Driver

Normal Frequency	: 24.576MHz
Frequency Tolerance	: ±50ppm(at25°C)

4.19.6 PLL

The PHY block of the R5C551 produces 393.216MHz of internal clock that is 16-times the 24.576MHz produced by the internal PLL circuit. The PLL circuit is enabled to stop by setting Sleep Mode of the PHY block. Please refer to the power management (Chapter 4.11) about setting of Sleep Mode.

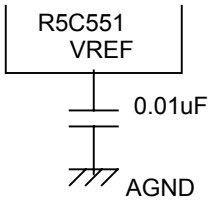
PLL External Circuit



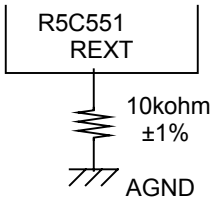
4.19.7 Reference Voltage Circuit and Reference Current Circuit

The PHY block of R5C551 supports terminals of external parts for the Reference voltage circuit and the Reference current circuit. Each terminal should be connected to indicated capacitors and resistors.

Reference Voltage Circuit



Reference Current Circuit



4.20 Notation

The following table shown the notation used in the register description.

NS	**not supported:** is used to indicate that registers and bits are not supported in the R5C551. Writing to these registers and bits has no effect. Returns zero when read.
RO	**read only:** is used to indicate that registers and bits are read only type. Writing to these registers and bits has no effect.
R/W	**read/write:** is used to indicate that registers and bits are readable and writable.
WO	**write only:** is used to indicate that registers and bits are write only type. Writing to these registers and bits has no effect. Returns zero when read.
RC	**read clear:** is used to indicate that registers and bits are read only type. Reading these registers and all bits clear. Writing to these registers and bits has no effect.
R/WC	**read/write clear:** is used to indicate that registers and bits are readable and writable. Writing a 1 to these registers and bits clears the corresponding field. Writing a 0 to them has no effect.

5 PCI CONFIGURATION REGISTERS

5.1 Overview

The R5C551 supports PCI-CardBus Bridge Interface functions for a PC Card socket and 1394 OHCI function. Each function has its own separate configuration space. Each configuration space can be configured independently with two sets of PCI configuration registers in compliance with the PCI Local Bus Specification Revision 2.2. The three sets of configuration registers are accessed through a mechanism defined for multi-function PCI devices.

5.2 Configuration

The R5C551 supports only Type 0 PCI configuration cycles (AD [1:0]=00). The bridge configuration registers for socket are addressed as a function #0 and the registers for 1394 OHCI-LINK are addressed as a function #1 with AD [10:8] as shown in the following table. The R5C551 make no response to attempted access of a register in the 2-7 function range and a PCI-master aborts.

AD [10:8]	R5C551 PCI Function Addressed
000	#0 PCI-CardBus bridge for socket
001	#1 1394 OHCI-LINK
010-111	none (Reserved)

5.3 Register Configuration

Logically the R5C551 looks to the primary PCI as one separate secondary bus and 1394 OHCI-LINK residing in a single device. Each function has its own configuration space. This makes the bridge a multi-function device. The R5C551 implement a 256 byte-configuration space. This space is divided into a predefined header space and a device dependent space. The first 64 bytes in each socket is defined the same predefined header format for all types of devices. The remaining 192 bytes is used as a unique configuration space can have different layouts depending on the base.

The R5C551 configuration space is accessible only from the primary PCI bus. No other interfaces respond to configuration cycles. Based on the configuration command (Read/Write) and the C/BE [3::0]# lines, the R5C551 will provide data from selected register or write the data proffered. Read data will be all 32-bit DWORD register, regardless of byte enables, with the requested data driven in its natural byte location. Write data will be deposited into the selected register using the C/BE [3::0]# lines to enable the write.

The PCI configuration register is consisted of the 8-bit BYTE register, the 16-bit WORD register and the 32-bit DWORD register. During a configuration access cycle, the PCI configuration register is accessed using a 32-bit DWORD. The C/BE [3:0]# byte enable to access to specified BYTE/WORD registers.

Register Space Name: PCI-CARDBUS Bridge Configuration Space

31 24	23 16	15 8	7 0	Bit
Device ID			Vendor ID	00h
PCI Status			PCI Command	04h
Class Code			Revision ID	08h
BIST	Header Type	PCI Latency Timer	Cache Line	0Ch
Card Control Registers Base Address				10h
CardBus Status		Reserved	Cap Ptr	14h
CardBus Latency Timer	Subordinate Bus Number	CardBus Bus Number	PCI Bus Number	18h
Memory Base 0				1Ch
Memory Limit 0				20h
Memory Base 1				24h
Memory Limit 1				28h
I/O Base 0				2Ch
I/O Limit 0				30h
I/O Base 1				34h
I/O Limit 1				38h
Bridge Control		Interrupt Pin	Interrupt Line	3Ch
Subsystem ID		Subsystem Vendor ID		40h
16-bit Legacy Mode Base Address				44h
Reserved				48h~7Ch
Misc Control		Bridge Configuration		80h
Reserved		16-bit Interface Control		84h
16-bit Memory Timing 0		16-bit I/O Timing 0		88h
Reserved				8Ch~9Ch
Misc Control 3		Misc Control 2		A0h
Misc Control 4				A4h
Reserved	GPIO 1	Reserved		A8h
Reserved				ACh~BCh
Writable Subsystem ID		Writable Subsystem Vendor ID		C0h
Reserved				C4h~D8h
Power Management		Next Item Ptr	Capability ID	DCh
Data	Power Management CSR			E0h
Reserved				

Register Space Name: 1394OHCI-LINK Configuration Space

31 24	23 16	15 8	7 0	Bit
Device ID			Vendor ID	00h
PCI Status			PCI Command	04h
Class Code			Revision ID	08h
BIST	Header Type	PCI Latency Timer	Cache Line	0Ch
1394OHCI Registers Base Address				10h
Reserved				14h
Reserved				18h
Reserved				1Ch
Reserved				20h
Reserved				24h
Reserved				28h
Subsystem ID			Subsystem Vendor ID	2Ch
Reserved				30h
Reserved			Cap_Ptr	34h
Reserved				38h
MAX Latency	MIN Grant	Interrupt Pin	Interrupt Line	3Ch
PCI OHCI Control				40h
Reserved				44h~7Ch
Reserved			MiscControl 5	80h
Reserved				84h~94h
Reserved		Phy Shadow	Phy Power Management	98h
Reserved	Misc Control 7	Reserved	Misc Control 6	9Ch
Reserved				A0h~A8h
Writable Subsystem ID			Writable Subsystem Vendor ID	ACh
Reserved				B0h~B4h
Serial ROM Control				B8h
Writable MAXLAT	Writable MINGNT	Reserved		BCh
Reserved				C0h~D8h
Power Management Capabilities		Next Item Ptr	Capability ID	DCh
Data	Power Management CSR			E0h
Reserved				

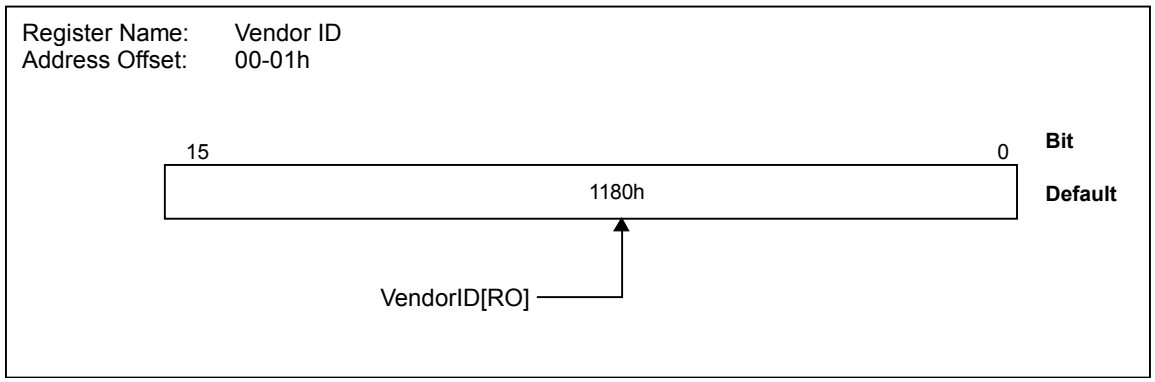
►Do not write-access to the reserved registers of the 80h~DBh registers on Ricoh's use.

5.4 Register Description

5.4.1 Vendor ID register

Register Name:	Vendor ID
Address Offset:	00h-01h(16bit)
Default:	1180h
Access:	RO

This is a unique 16-bit value that is assigned to the vendor identification, and it is used with the Device ID in order to identify each PCI device. Writing to this register has no effect.



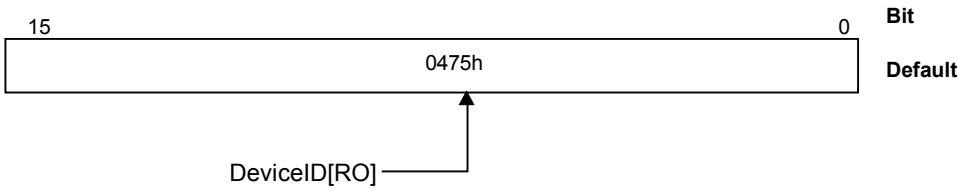
Bit	Field Name	Description
15-0	Vendor ID	This read-only field is the vendor identification assigned to RICOH by the PCI Special Interest Group. This field always returns 1180h when read.

5.4.2 Device ID register

Register Name: Device ID
Address Offset: 02h-03h(16bit)
Default: 0475h
Access: RO

This is a unique 16-bit value that is assigned to the PCI CardBus Bridge function, and it is used with the Vendor ID in order to identify each PCI device. Writing to this register has no effect.

Register Name: Device ID
Address Offset: 02-03h

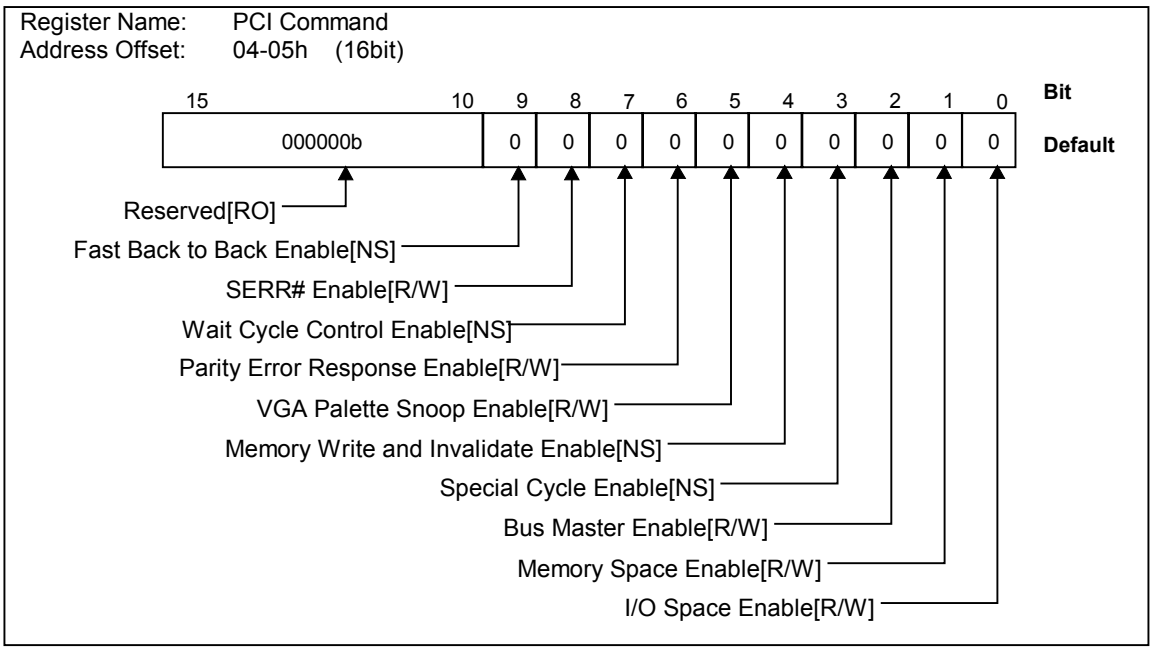


Bit	Field Name	Description
15-0	Device ID	This read-only field is the device identification assigned to the R5C551 by RICOH. This field always returns 0475h when read.

5.4.3 PCI Command register

Register Name:	PCI Command
Address Offset:	04h-05h(16bit)
Default:	0000h
Access:	R/W

The PCI Command Register controls the R5C551's responses to PCI Bus transactions on the primary interface. When this register has a value of '0', the function accepts only configuration accesses. The bits, with the exception of VGA Palette Snoop Enable bit, in this register adhere to the definitions in the PCI Local Bus Specification.

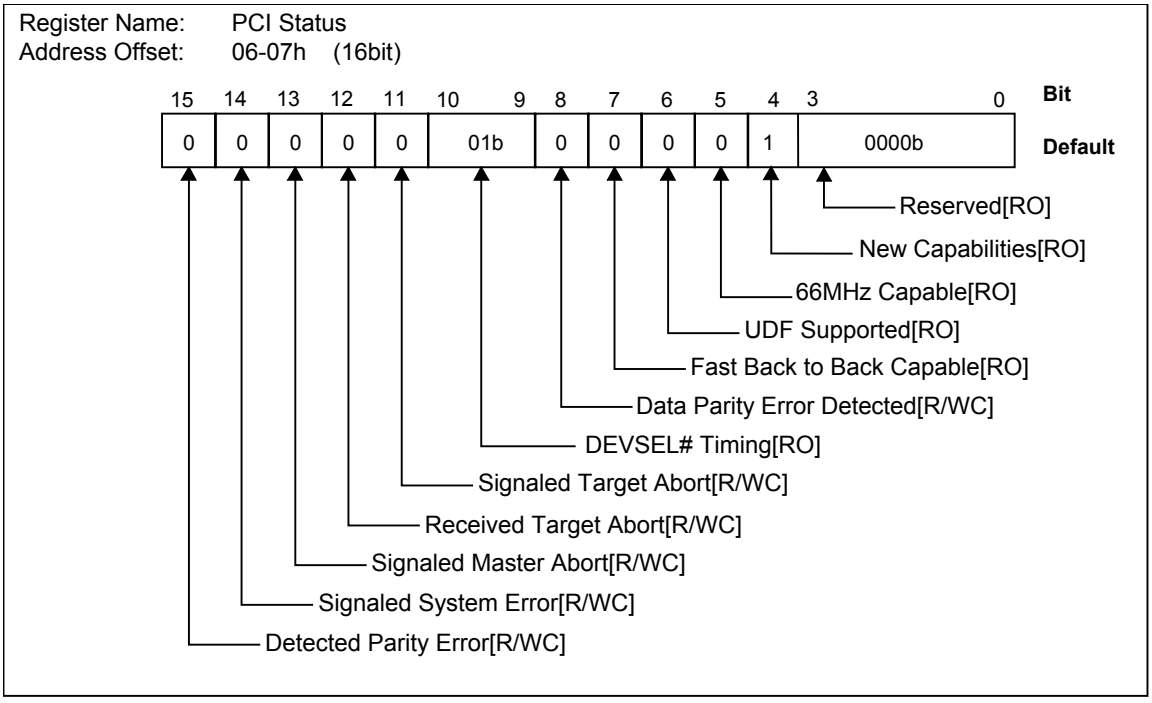


Bit	Field Name	Description
15-10	Reserved	This field is reserved for future use by PCI Local Bus specification 2.2. This field always returns zero when read.
9	Fast Back to Back Enable	This bit controls whether the PCI master performs fast back-to-back transactions or not. But, this function is not implemented in the R5C551. This bit always returns zero when read. Writing to this bit has no effect.
8	SERR# Enable	This bit controls whether or not the SERR# output buffer is enabled on the PCI interface. The default after reset is zero. 0 - disable the SERR# driver. 1 - enable the SERR# driver. This bit must be set to report address parity errors.
7	Wait Cycle Control Enable	This bit controls whether or not a card does address/data stepping. But, this function is not implemented in the R5C551. This bit always returns zero when read. Writing to this field has no effect.
6	Parity Error Response Enable	This bit controls the device's response to parity errors. When this bit is set to 1, the R5C551 takes its normal action - enable an error bit and assert PERR#, when a parity error is detected. When this bit is set to 0, the R5C551 ignores any parity errors and continue normal operation. The default after reset is zero.
5	VGA Palette Snoop Enable	This bit controls the R5C551's response to VGA palette registers. When this bit is set to 1, palette snooping is enabled (AD [9:0] = 3C6h, 3C8h and 3C9h are decoded, AD [15:10] are not). The R5C551 forwards these addresses to the CardBus interface. Conversely, the R5C551 ignores to read from these addresses on the CardBus interface. When this bit is set to 0, the R5C551 ignores palette accesses. The default after reset is zero.
4	Memory Write and Invalidate Enable	This bit controls whether or not the PCI master uses the Memory Write and Invalidate command. But, this function is not implemented in the R5C551. This bit always returns zero when read. Writing to this bit has no effect.
3	Special Cycle Enable	This bit controls an action on Special Cycle operations. But, this function is not implemented in the R5C551. This bit always returns zero when read. Writing to this bit has no effect.
2	Bus Master Enable	This bit controls the R5C551's ability to operate as a master on the PCI interface. Setting this bit has no effect upon the configuration command operations. When this bit is set to 0, the R5C551 ignores all memory or I/O transactions on the CardBus interface. The default after reset is zero. 0 - inhibit the R5C551 to operate as a master on the PCI interface. 1 - allow the R5C551 to operate as a master on the PCI interface
1	Memory Space Enable	This bit controls the R5C551's response to memory accesses for both the memory mapped I/O ranges and the prefetchable memory ranges. The default after reset is zero. 0 - ignore all memory transactions on the PCI interface, and the R5C551 DEVSEL# logic is inhibited during the memory cycle. 1 - enable response to memory transactions on the PCI interface. And also, this bit controls accesses to the memory mapped I/O ranges that are defined in the Card Control Base Address register.
0	I/O Space Enable	This bit controls the R5C551's response to I/O accesses for transactions on the PCI interface. The default after reset is zero. 0 - ignore all I/O transactions on the PCI interface, and the R5C551. DEVSEL# logic is inhibited during the I/O cycle. 1 - enable response to I/O transactions on the PCI interface.

5.4.4 PCI Status register

Register Name:	PCI Status
Address Offset:	06h-07h(16bit)
Default:	0210h
Access:	RO, R/WC

This 16-bit register is used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A bit is reset whenever the register is written and the data in the corresponding bit location is a one. Writing a zero to this register has no effect. The bits in this register adhere to the definitions in the PCI Local Bus Specification, but only apply to the primary PCI interface.



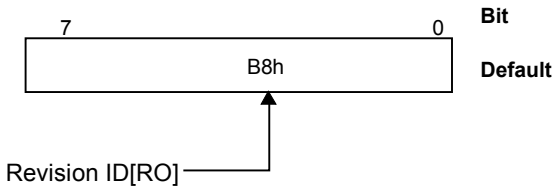
Bit	Field Name	Description
15	Detected Parity Error	This bit is set by the R5C551 whenever it detects a parity error, even if parity error handing is disabled (as controlled by bit 6 in the Command register). Writing a one to this bit clears the state.
14	Signaled System Error	This bit is set whenever the R5C551 asserts SERR#. Writing a one to this bit clears the state.
13	Signaled Master Abort	This bit is set by the R5C551 as a master device whenever its transaction is terminated with Master-abort. Writing a one to this bit clears the state.
12	Received Target Abort	This bit is set by the R5C551 as a master device whenever its transaction is terminated with Target-abort. Writing a one to this bit clears the state.
11	Signaled Target Abort	This bit is set by the R5C551 as a target device whenever its transaction is terminated with Target-abort. Writing a one to this bit clears the state.
10-9	DEVSEL# Timing	These bits encode the timing of DEVSEL#. These are encoded as 01b for medium speed. These bits are read-only. Writing to these bits has no effect.
8	Data Parity Error Detected	This bit is set when three conditions are met: 1) the bus agent asserted PERR# itself or observed PERR# asserted. 2) the agent setting the bit acted as the bus master for the operation in which the error occurred. 3) the Parity Error Response bit (Command register) is set. Writing a one to this bit has no effect.
7	Fast Back to Back Capable	This read-only bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. The R5C551 returns zero when read, because it is not capable of accepting fast back-to-back transactions. Writing to this bit had no effect.
6	UDF Supported	This read-only bit indicates whether or not the PCI device supports the UDF function. The R5C551 doesn't support the UDF function, and therefore returns a zero when read. Writing to this bit has no effect.
5	66MHz Capable	This read-only bit indicates whether or not the PCI device is capable of running at 66MHz. The R5C551 is capable of running only at 33MHz, and therefore returns a zero when read. Writing to this bit has no effect.
4	New Capabilities	This bit indicates whether PCI device implements a list of new capabilities such as PCI Power Management. The R5C551 implements it, and therefore returns a one when read. The register at 14h provides an offset into the configuration space pointing to the location of Power Management Register Block.
3-0	Reserved	These read-only bits are reserved for future use by PCI Local Bus specification 2.2. Return a zero when read. Writing to these bits has no effect.

5.4.5 Revision ID register

Register Name:	Revision ID
Address Offset:	08h(8bit)
Default:	B8h
Access:	RO

This is a unique 8-bit value that is asserted to the device revision information. It is used with the Vendor ID and the Device ID in order to identify each PCI device. Writing to this register has no effect.

Register Name: Revision ID
Address Offset: 08h (8bit)

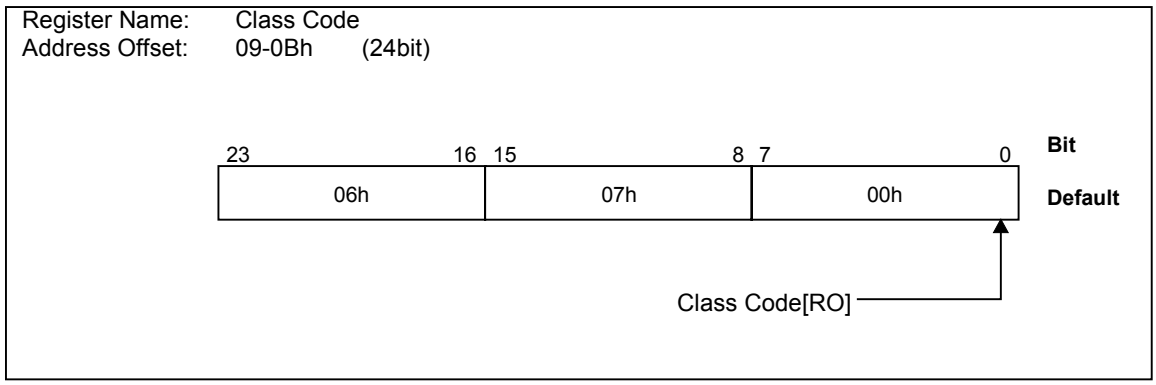


Bit	Field Name	Description
7-0	Revision ID	This read-only field is the revision identification number assigned to the R5C551 by RICOH. This field always returns B8h when read.

5.4.6 Class Code register

Register Name:	Class Code
Address Offset:	09h-0Bh(24bit)
Default:	060700h
Access:	RO

The Class Code register is read-only and is used to identify the generic function of the device. The bits in this register adhere to the definitions in the PCI Local Bus Specification. This register is broken into three byte-size fields: a base class code, a sub-class code and a programming interface. Writing to this register has no effect.



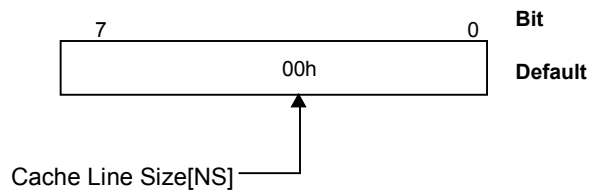
Bit	Field Name	Description
23-0	Class Code	This register is a read-only register and is used to identify the device. This register is broken into three byte-size fields. The upper byte (at offset 0Bh) is a base class code. The middle byte (at offset 0Ah) is a sub-class coded. The lower byte (at offset 09h) identifies a specific register-level programming interface. The R5C551 returns 060700h when this register is indicated as a PCI-CardBus bridge device: a base class of 06h (bridge device), a sub-class code of 07h (PCI to CardBus) and a programming interface of 00h. Writing to this register has no effect.

5.4.7 Cache Line Size register

Register Name:	Cache Line Size
Address Offset:	0Ch(8bit)
Default:	00h
Access:	NS

The Cache Line register specifies the system cache line size in units of 32-bit words. The R5C551 doesn't participate in the caching protocol, and therefore returns zero when read. Writing to this register has no effect.

Register Name: Cache Line Size
Address Offset: 0Ch (8bit)



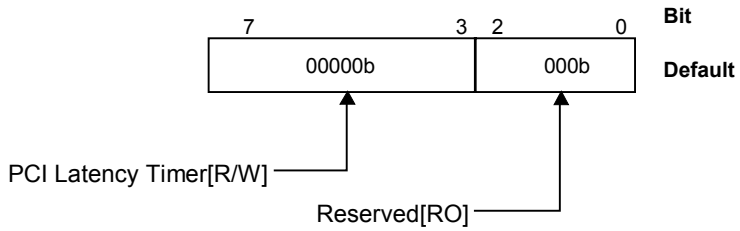
Bit	Field Name	Description
7-0	Cache Line Size	The R5C551 doesn't participate in the caching protocol. This register is read-only. Returns zero when read. Writing to this register has no effect.

5.4.8 PCI Latency Timer register

Register Name:	PCI Latency Timer
Address Offset:	0Dh(8bit)
Default:	00h
Access:	R/W

The PCI Latency Timer specifies, in units of PCI bus clocks, the value of the Latency Timer for the PCI bus master. This register adheres to the PCI Local Bus Specification but applies only to the primary interface. The bottom three bits in this register are read-only and hardwired to 000b, resulting in a timer granularity of eight clocks.

Register Name: PCI Latency Timer
Address Offset: 0Dh (8bit)



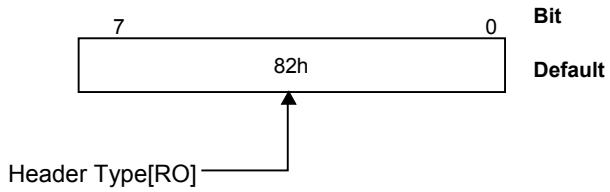
Bit	Field Name	Description
7-3	PCI Latency Timer	This register specifies, in units of PCI bus clocks, the value of the Latency Timer for the PCI bus master.
2-0	Reserved	The bottom three bits in this register are read-only and hardwired to 000b, resulting in a timer granularity of eight clocks. Writing to this field has no effect.

5.4.9 Header Type register

Register Name:	Header Type
Address Offset:	0Eh(8bit)
Default:	82h
Access:	RO

The Header Type register identifies the layout of bytes 10h through 3Fh in configuration space and whether or not the device contains multiple function. The R5C551 is the multi-function device and the PCI-CardBus Bridge, and therefore returns 82h when read. Writing to this register has no effect.

Register Name: Header Type
Address Offset: 0Eh (8bit)



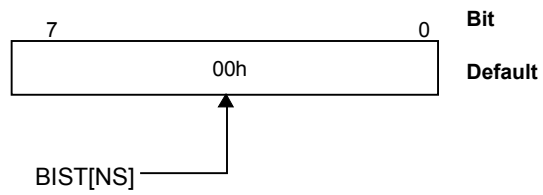
Bit	Field Name	Description
7-0	Header Type	This register identifies the layout of bytes 10h through 3Fh in configuration space and also whether or not the device contains multiple functions. Return 82h when read. Writing to this register has no effect.

5.4.10 BIST register

Register Name:	BIST
Address Offset:	0Fh(8bit)
Default:	00h
Access:	NS

The BIST register is used for control and status of BIST (Built In Self Test). The bits in this register adhere to the definitions in the PCI Local Bus Specification. The R5C551 does not implement BIST, and therefore returns zero when read.

Register Name: BIST
Address Offset: 0Fh (8bit)



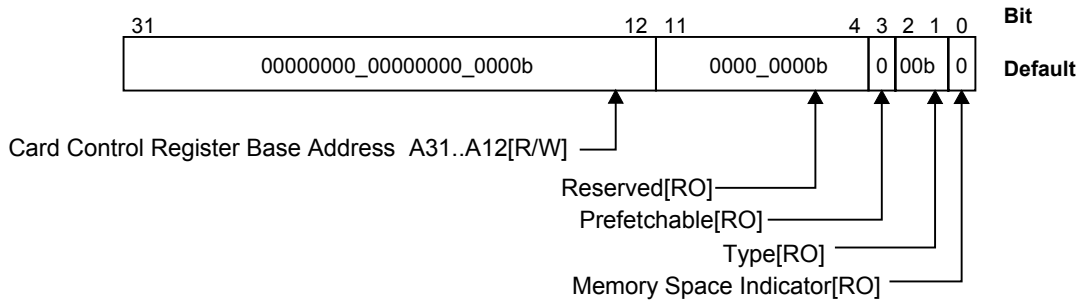
Bit	Field Name	Description
7-0	BIST	The R5C551 doesn't support this register. This read-only register always returns zero when read. Writing to this register has no effect.

5.4.11 Card Control Register Base Address register

Register Name:	Card Control Register Base Address
Address Offset:	10h(32bit)
Default:	0000_0000h
Access:	R/W

The Card Control Register Base Address register points to the memory mapped I/O space that contains Status and Control registers for both the PC Card-32 and the PC Card-16. The upper bits [31:12] are read/write and the lower bits [11:0] are hardwired to zero. This indicates to Configuration software that the R5C551 must take 4K bytes of non-prefetchable memory space. The PC Card-32 (CardBus Card) Status and Control registers start at offset 000h (in the bottom 2K bytes) and the PC Card-16 registers start at offset 800h (in the top 2K bytes). The R5C551 dose not respond to PCI cycles unless specifically loaded with a non-zero address after PCIRST# is deasserted.

Register Name: Card Control Register Base Address
Address Offset: 10h (32bit)

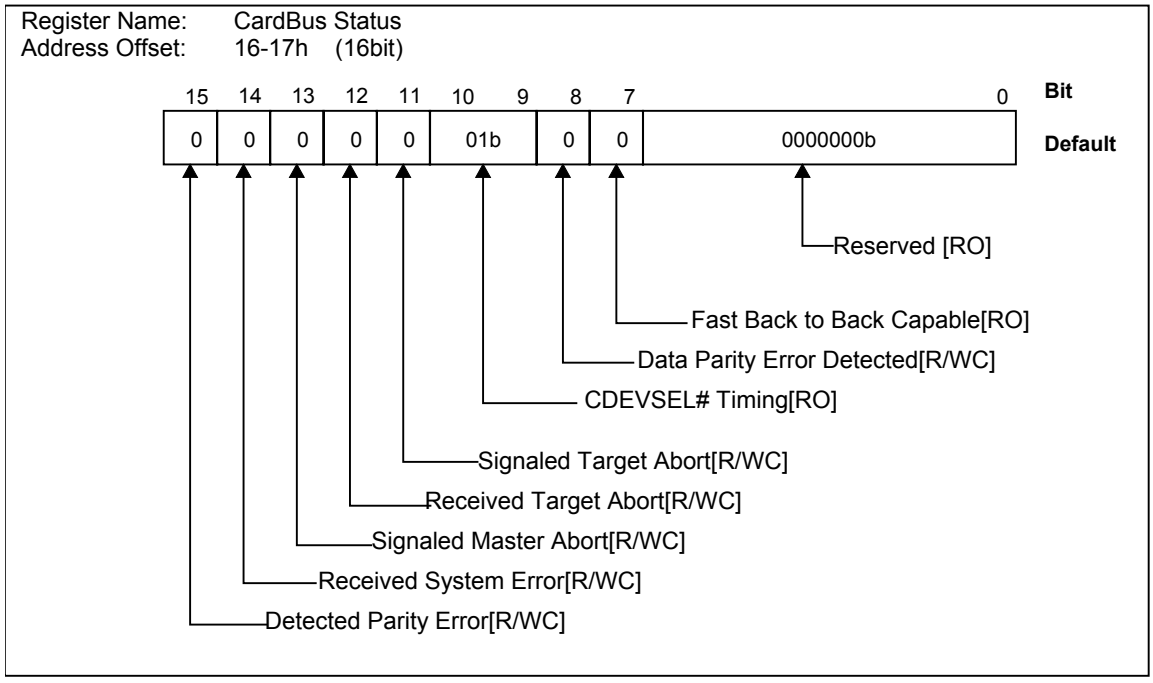


Bit	Field Name	Description
31-12	Card Control Register Base Address A31..A12	These bits indicate the memory mapped I/O space that contains status and control registers for both the PC Card-32 and the PC Card-16. Bits [31:12] are read/write.
11-4	Reserved	These bits are read-only and hardwired to zero. Writing to this field has no effect.
3	Prefetchable	This bit is set to one when the data is prefetchable and reset to a zero otherwise. This filed is hardwired to zero in the R5C551. Writing to this bit has no effect.
2-1	Type	These bits have encoded meanings as shown below for Memory Base Address registers. 00 : locate anywhere in 32-bit address space 01 : locate below 1M 10 : locate anywhere in 64-bit address space 11 : reserved This field is read-only and hardwired to zero in the R5C551. Writing to this field has no effect.
0	Memory Space Indicator	This bit indicates the Base Address register maps into either a memory space or an I/O space. This bit returns zero when the register maps into a memory space and one when the register maps into an I/O space. This bit is read-only and hardwired to zero in the R5C551. Writing to this bit has no effect.

5.4.12 CardBus Status register

Register Name:	CardBus Status
Address Offset:	16h-17h(16bit)
Default:	0200h
Access:	RO, R/WC

The CardBus Status register is used to record status information for CardBus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A bit is reset whenever the register is written and the data in the corresponding bit location is a one. Writing a zero to this register has no effect. The bits in this register adhere to the definitions in the PCI Local Bus Specification, but only apply to the secondary CardBus interface.



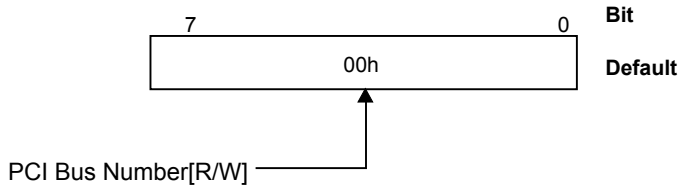
Bit	Field Name	Description
15	Detected Parity Error	This bit is set by the R5C551 whenever it detects a parity error on the secondary bus, even if parity error handing is disabled (as controlled by bit 6 in the Command register). Writing a one to this bit clears the state.
14	Received System Error	This bit is set whenever the R5C551 receives CSERR#. Writing a one to this bit clears the state. When both CSERR# enable bit in the Bridge Control register and SERR# enable bit in the PCI Command register are set, the R5C551 asserts SERR# on the primary PCI bus whenever it receives CSEER#.
13	Signaled Master Abort	This bit is set by the R5C551 as a master device on the CardBus interface whenever its transaction is terminated with master-abort. Writing a one to this bit clears the state.
12	Received Target Abort	This bit is set by the R5C551 as a master device on the CardBus interface whenever its transaction is terminated with target-abort. Writing a one to this bit clears the state.
11	Signaled Target Abort	This bit is set by the R5C551 as a target device on the CardBus interface whenever its transaction is terminated with target-abort. Writing a one to this bit clears the state.
10-9	CDEVSEL# Timing	This field encodes the timing of CDEVSEL#. These read-only bits are encoded as 01b for medium speed in the R5C551. Writing to this field has no effect.
8	Data Parity Error Detected	This bit is set by a CardBus master when three conditions are met: 1) the bus agent asserted CPERR# itself or observed CPERR# asserted. 2) the agent setting the bit acted as the bus master for the operation in which the error occurred. 3) the Parity Error Response bit (Control register) is set. Writing a one to this bit clears the state.
7	Fast Back to Back Capable	This read-only bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not the same agent. The R5C551 returns a zero when read, because it is not capable of fast back-to-back transactions on the CardBus interface. Writing to this bit has no effect.
6-0	Reserved	This bit is reserved for future use by the PCI Local Bus specification 2.2. This field is read-only. Returns zero when read. Writing to this field has no effect.

5.4.13 PCI Bus Number register

Register Name:	PCI Bus Number
Address Offset:	18h(8bit)
Default:	00h
Access:	R/W

The PCI Bus Number register indicates the number of the PCI bus on the primary side of the R5C551. The appropriate configuration software sets this register. The R5C551 doesn't decode Type 1 configuration transactions on the CardBus interface that should be converted to Special Cycle transactions on PCI bus interface.

Register Name: PCI Bus Number
Address Offset: 18h (8bit)

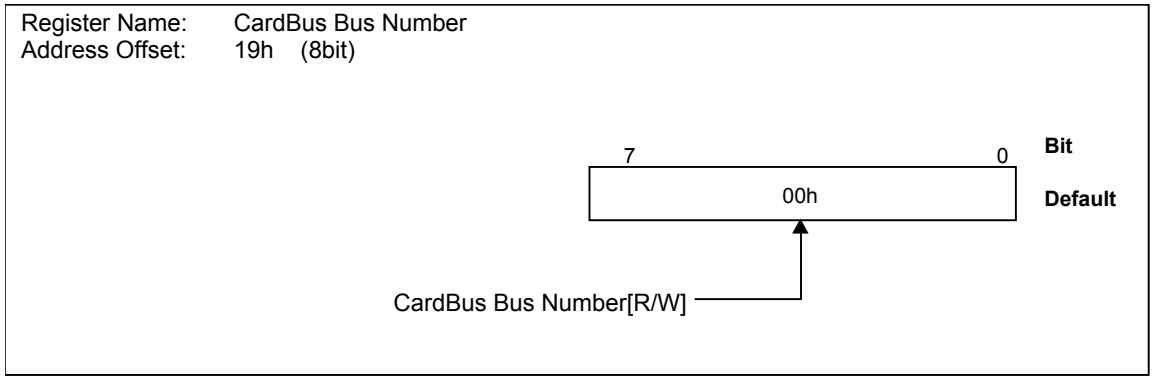


Bit	Field Name	Description
7-0	PCI Bus Number	This field indicates the number of the PCI bus on the primary side of the R5C551. This field is read/write, but this register has no effect upon the R5C551's operation. The default after reset is zero.

5.4.14 CardBus Bus Number register

Register Name:	CardBus Bus Number
Address Offset:	19h(8bit)
Default:	00h
Access:	R/W

The CardBus Bus Number register indicates the number of the CardBus attached to the socket. This read/write register is set by the appropriate configuration software, or the socket services software. The R5C551 uses this register to convert Type 1 configuration transactions on the primary (PCI) interface to Type 0 transactions on the secondary (CardBus) interface.



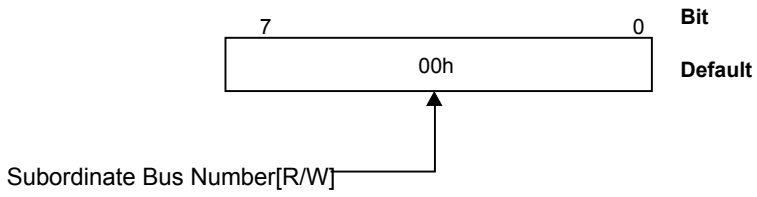
Bit	Field Name	Description
7-0	CardBus Bus Number	This register indicates the number of the CardBus attached to the socket. This is set by the appropriate configuration software or the socket services software. If the values of a Bus Number field agree with the values of this register on a Type 1 configuration transactions on the primary (PCI) interface, the R5C551 converts them to a Type 0 configuration transactions on the secondary (CardBus) interface. The default after reset is zero.

5.4.15 Subordinate Bus Number register

Register Name:	Subordinate Bus Number
Address Offset:	1Ah(8bit)
Default:	00h
Access:	R/W

The Subordinate Bus Number register is used to record the number of the bus at the lowest part of the hierarchy behind the bridge. This read/write register is set by the appropriate configuration software or the socket services software. Normally, a CardBus bridge will be at the bottom of the bus hierarchy and this register will hold the same value as the CardBus Bus Number register. The R5C551 uses this register in conjunction with the Card Bus Number register to convert Type 1 configuration transactions on the primary (PCI) interface to Type 0 or 1 configuration transactions on the secondary interface.

Register Name: Subordinate Bus Number
Address Offset: 1Ah (8bit)



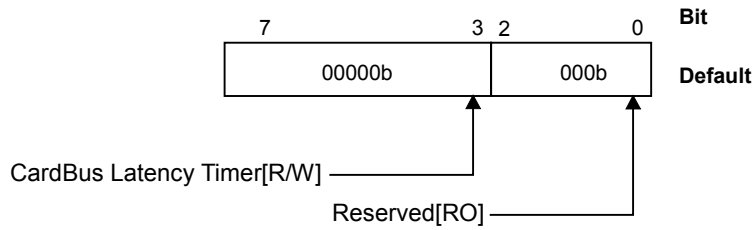
Bit	Field Name	Description
7-0	Subordinate Bus Number	This register is used to record the number of the bus at the lowest part of the hierarchy behind the R5C551. This read/write register is set by the appropriate configuration software, or the socket services software. Normally, a CardBus bridge will be at the bottom of the bus hierarchy and this register will hold the same value as the CardBus Bus Number register. When the value of Bus Number field is more over the CardBus Bus Number register's and less than this register's in Type 1 configuration cycles on the primary (PCI) interface, the R5C551 converts the value to Type1 configuration cycles on the secondary (CardBus) interface. The default after reset is zero.

5.4.16 CardBus Latency Timer register

Register Name:	CardBus Latency Timer
Address Offset:	1Bh(8bit)
Default:	00h
Access:	R/W

The CardBus Latency Timer register has the same functionality of the primary PCI bus Latency Timer but applies to the CardBus attached to this specific socket. This is set by the PCI BIOS configuration software or the socket services software. This register adheres to the PCI Local Bus Specification but applies only to the primary interface. The bottom three bits in this register are read-only and hardwired to zeros, resulting in a timer granularity of eight clocks.

Register Name: CardBus Latency Timer
Address Offset: 1Bh (8bit)

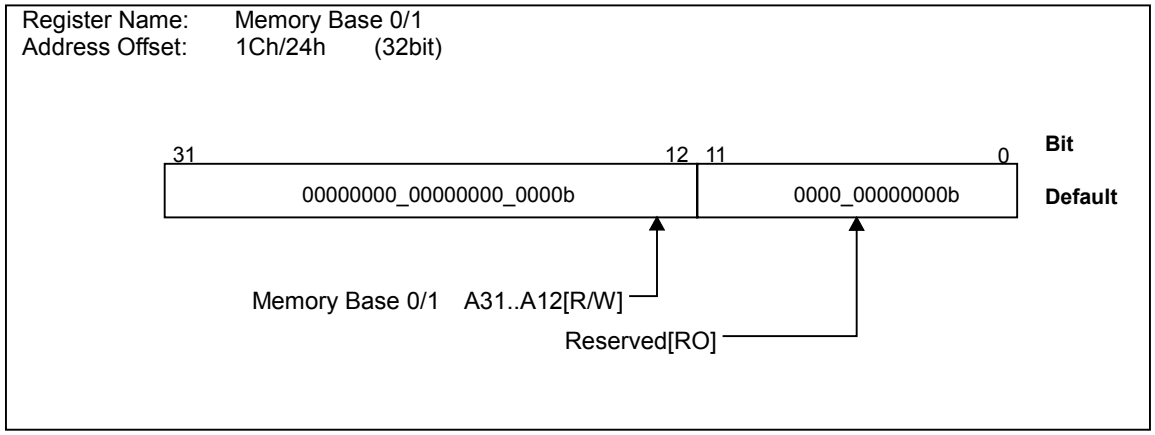


Bit	Field Name	Description
7-3	CardBus Latency Timer	This field specifies, in units of CardBus clocks, the value of the Latency Timer for the CardBus master.
2-0	Reserved	These bits are read-only and hardwired to 000b, resulting in a timer granularity of eight clocks. Writing to this field has no effect.

5.4.17 Memory Base 0/1 register

Register Name:	Memory Base 0/1
Address Offset:	#0: 1Ch-1Fh(32bit)
	#1: 24h-27h(32bit)
Default:	0000_0000h
Access:	R/W

The Memory Base 0/1 register indicates the bottom address of a memory mapped I/O window. The upper 20-bits correspond to address bits AD [31:12] that is read/write. The bottom 12-bits of this register is read-only and hardwired to zeros. The Memory Space Enable bit (bit1) in the Command register enables this window. The Memory #0 Prefetch Enable bit (bit8) in the Bridge Control register specifies whether the memory window is prefetchable or non-prefetchable. The default of this bit is prefetchable, but this bit must be non-prefetchable only when side effects are caused by memory read command on the installed CardBus card. This register has no meaning for PC Card-16.

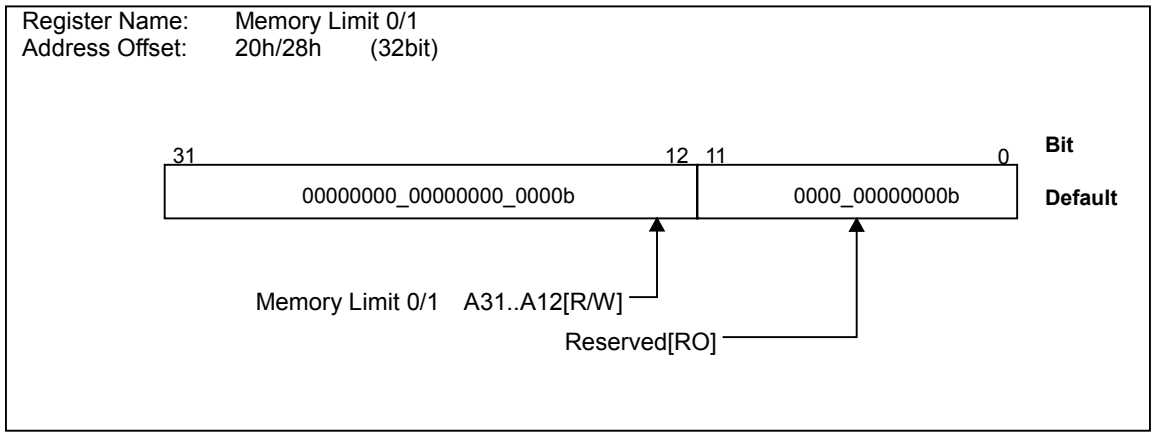


Bit	Field Name	Description
31-12	Memory Base 0/1 A31..A12	This register indicates the base address of a memory mapped I/O range that is used by the R5C551 to determine when to forward memory transactions from PCI interface to CardBus interface. This field is read/write.
11-0	Reserved	This field is read-only and hardwired to zeros. Writing to this field has no effect.

5.4.18 Memory Limit 0/1 register

Register Name:	Memory Limit 0/1
Address Offset:	#0: 20h-23h (32bit)
	#1: 28h-2Bh (32bit)
Default:	0000_0000h
Access:	R/W

The Memory Limit 0/1 register indicates the top address of the memory mapped I/O space 0/1. The upper 20-bits correspond to address bits AD [31:12] that are read/write. The bottom 12-bits of this register is read-only and hardwired to zeros. The bridge assumes the bottom address bits [11:0] are ones when the address range is decoded. So if the Memory Base and Limit registers are set to the same value, a window of 4Kbyte is defined. Both Memory windows #0 and #1 are enabled by the Memory Space Enable bit in the PCI Command register. To disable either window individually, the Limit register of that range should be set below the Base register. This will cause the bridge to never detect a hit on that window. This register has no meaning for PC Card-16.



Bit	Field Name	Description
31-12	Memory Limit 0/1 A31..A12	This field indicates the top address of a PCI memory address range that is used by the R5C551 to determine when to forward memory transactions from the PCI interface to the CardBus interface.
11-0	Reserved	This field is read-only and hardwired to zeros. Writing to this field has no effect.

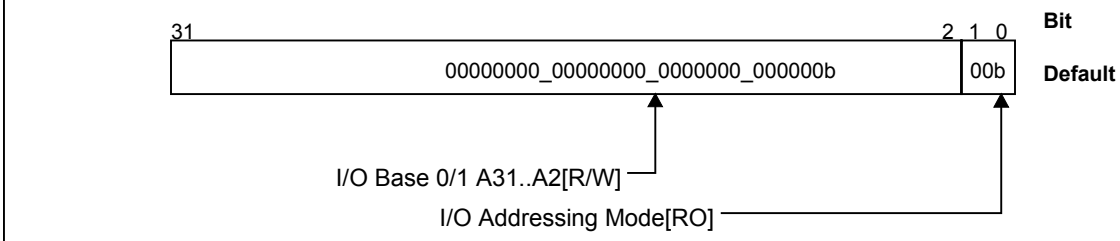
5.4.19 I/O Base 0/1 register

Register Name:	I/O Base 0/1
Address Offset:	#0: 2C-2Fh(32bit)
	#1: 34h-37h(32bit)
Default:	0000_0000h
Access:	R/W

The I/O Base 0/1 register indicates the bottom address of a PCI I/O address range that used by the R5C551 to determine when to forward an I/O transaction to the CardBus. The upper bits of this register corresponding to AD [31:2] are read/write, and the lower bits corresponding to AD [1:0] are read-only. AD [1:0] is fixed to 00b on the R5C551's 16bit I/O addressing mode, and 01b on the R5C551's 32bit I/O addressing mode. Therefore, each 4byte of I/O space 0/1 is enabled.

If these bits have the value 0, then the bridge implements only 16-bit I/O addressing and assumes that the upper 16 address bits AD [31:16] of the I/O base address register are zero. And if they have the value 1, then the bridge implements 32-bit I/O addressing and the 16 bits of the base register hold the upper 16 bits corresponding to AD [31:16] of the 32-bit I/O address space. These I/O window 0/1 are enabled by the I/O Space Enable bit in the PCI Command register. This register has no meaning for PC Card-16.

Register Name: I/O Base 0/1
Address Offset: 2C-2Dh (32bit)



Bit	Field Name	Description
31-2	I/O Base 0/1 A31..A2	This field indicates the base address of an address range that is used by the R5C551 to determine when to forward an I/O transaction from PCI interface to the CardBus interface.
1-0	I/O Addressing Mode	This field is read-only and returns 00b on the 16-bit I/O addressing mode, and returns on 01b on the 32-bit addressing mode. Writing to this field has no effect.

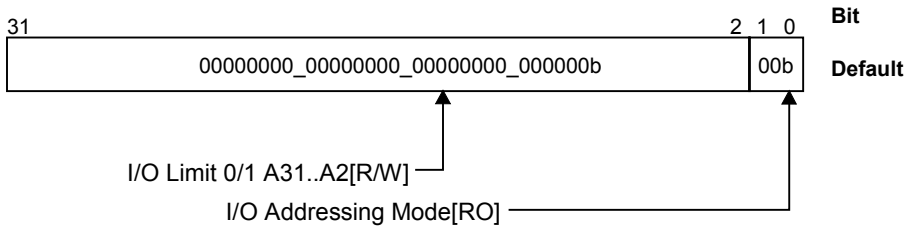
5.4.20 I/O Limit 0/1 register

Register Name:	I/O Limit 0/1
Address Offset:	#0: 30h-33h(32bit)
	#1: 38h-3Bh(32bit)
Default:	0000_0000h
Access:	R/W

The I/O Limit 0/1 registers indicate the top address of an address range that is used by the R5C551 to determine when to forward an I/O transaction to the CardBus. The upper bits of this register correspond to AD [31:2] are read/write, and the lower bits AD [1:0] are read-only. AD [1:0] is fixed to 00b on the R5C551's 16bit I/O addressing mode, and 01b on the R5C551's 32bit I/O addressing mode. Therefore, each 4byte of I/O space 0/1 is enabled.

Both I/O windows #0 and #1 are enabled by the I/O Space Enable bit in the PCI command register. This register has no meaning for PC Card-16.

Register Name: I/O Limit 0/1
Address Offset: 30/38h (32bit)



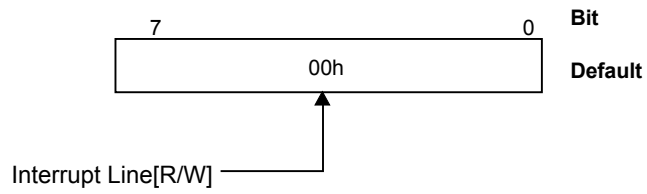
Bit	Field Name	Description
15-2	I/O Limit 0 Lower A31..A2	This field indicates the limit address of an address range that is used by the R5C551 to determine when to forward an I/O transaction from the PCI interface to the CardBus interface.
1-0	I/O Addressing Mode	This field is read-only and returns 00b on the 16-bit I/O addressing mode, and returns 01b on the 32-bit I/O addressing mode. Writing to this field has no effect.

5.4.21 Interrupt Line register

Register Name:	Interrupt Line
Address Offset:	3Ch(8bit)
Default:	00h
Access:	R/W

The Interrupt Line register is read/write register used to communicate interrupt line routing information. This register must be initialized by BIOS software on the system configuration, so a default state is no specified. The value in this register indicates which input of the system interrupt controller the interrupt pin in the R5C551 is connected to. The default after reset is 00h.

Register Name: Interrupt Line
Address Offset: 3Ch (8bit)



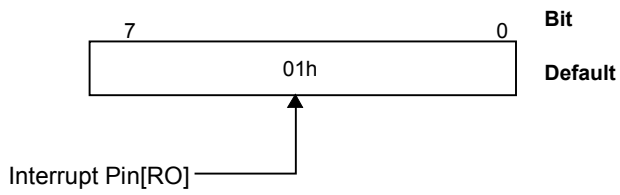
Bit	Field Name	Description
7-0	Interrupt Line	The value in this register indicates which input of the system interrupt controller the interrupt pin in the R5C551 is connected to. The default after reset is 00h.

5.4.22 Interrupt Pin register

Register Name:	Interrupt Pin
Address Offset:	3Dh(8bit)
Default:	01h
Access:	RO

The Interrupt Pin register is read-only register that adheres to the definition in the PCI Local Bus Specification. This register indicates which interrupt pin the R5C551 use. A value of 01h corresponding to INTA# is assigned to socket. The value of this register is changed by INT Select bit in the Misc Control 6 register.

Register Name: Interrupt Pin
Address Offset: 3Dh (8bit)

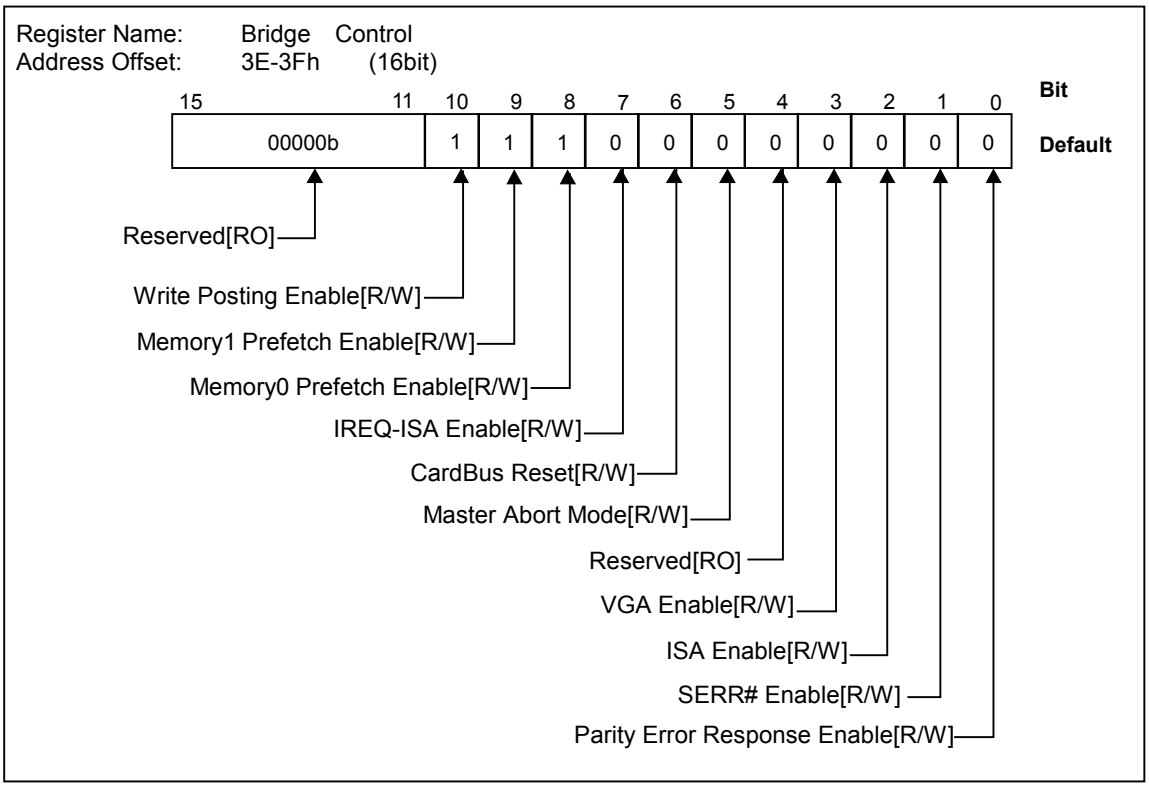


Bit	Field Name	Description
7-0	Interrupt Pin	This field is read-only and returns 01h for socket.

5.4.23 Bridge Control register

Register Name:	Bridge Control
Address Offset:	3Eh-3Fh(16bit)
Default:	0700h
Access:	R/W

The Bridge Control register provides control over the R5C551's bridging functions. Each bit in this register adheres to the definitions in the PC Card Standard.



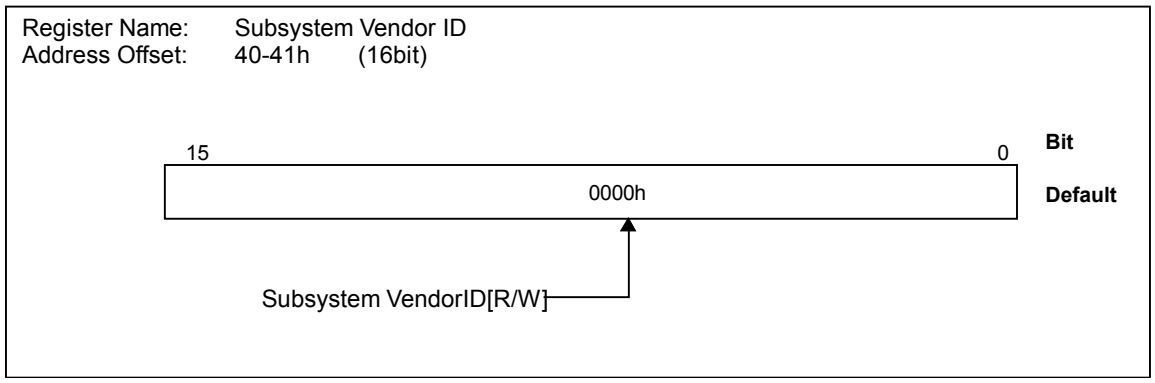
Bit	Field Name	Description
15-11	Reserved	This field is read-only and returns zeros. Writing to this field has no effect.
10	Write Posting Enable	This bit enables posting of Write data to and from the socket. If this bit is not set, the bridge must drain any data in its buffers before accepting data for or from the socket. The target must accept each data word before the bridge can accept the next word from the source master. The bridge must not release the source master, until the target accepts the last word. Operating with write posting disabled will inhibit system performance. This bit is encoded as: 0 : Write Posting Disabled 1 : Write Posting Enabled (default)
9	Memory 1 Prefetch Enable	This bit specifies whether the memory window #1 is prefetchable or non-prefetchable. This bit is encoded as: 0 : the memory window #1 is non-prefetchable. 1 : the memory window #1 is prefetchable. The default after reset is one.

Bit	Field Name	Description
8	Memory 0 Prefetch Enable	This bit specifies whether the memory window #0 is prefetchable or non-prefetchable. This bit is encoded as: 0 : the memory window #0 is non-prefetchable. 1 : the memory window #0 is prefetchable. The default after reset is one.
7	IREQ-ISA Enable	This bit controls the function interrupt for the PC Card-16/CardBus Card. When this bit is set to one, the IREQ#/CINT# interrupt is routed to the ISA system interrupt pins IRQ [15:3] that are indicated by the Interrupt General Control register. When it is set to zero, the IREQ# interrupt is routed to INTA# or INTB# that is the PCI interrupt pin. When this bit controls the function interrupt output pin for the CardBus Card, CINT-ISA Disable bit must be cleared. The default after reset is zero.
6	CardBus Reset	When this bit is set to one, the R5C551 assert and hold CRST#. When this bit is cleared, they deassert CRST#. This bit can be set by software. It can also be set by hardware when the R5C551 executes the power down sequence. CRST# is a wired-OR of this bit and PCIRST#.
5	Master Abort Mode	When the R5C551 is a Master, this bit controls the behavior of the R5C551 when a master abort occurs on either PCI or CardBus interface. When this bit is cleared, the R5C551 returns ones if a master abort occurs during the read transaction, and the R5C551 annuls the data if a master abort occurs during the write transaction. When this bit is set to one, if the corresponding transaction on the opposite bus terminates, with a master abort and without completing the transaction on the source side (reads and non-posted writes), the R5C551 signals a target abort to the requesting master. And the R5C551 asserts SERR# on the PCI bus when the transaction on the source side and SERR# is enabled in the Command register. The default after reset is zero.
4	Reserved	This bit is read-only and returns zero. Writing to this bit has no effect.
3	VGA Enable	This bit controls the R5C551's response to VGA compatible addresses. When the VGA enable bit is set, the R5C551 forward transactions in the following ranges to the CardBus interface. Memory : 000A0000h to 000BFFFFh I/O : AD [9:0] = 3B0h to 3BBh, 3C0h to 3DFh (inclusive of ISA address aliases - AD [15:10] are not decoded.) On the other hand, the R5C551 make no response to transactions in the same ranges from the CardBus interface. The forwarding of these addresses is affected by the I/O and Memory Enable bit in the Command register. The default after reset is zero.
2	ISA Enable	This bit controls the R5C551's access to ISA compatible addresses that adhere to the first 64 Kbytes of PCI I/O space. When the ISA Enable bit is set, the R5C551 forward the only first 64 Kbytes from the PCI to the CardBus and block forwarding the last 768 bytes in 1 K block. In the opposite direction (CardBus to PCI) I/O transactions, the last 768 bytes in 1K block are forwarded. The default after reset is zero.
1	SERR# Enable	This bit controls whether or not the R5C551 forward an assertion of CSERR# on the CardBus interface to SERR# on the PCI interface. 0 : CSERR# is not forwarded to PCI. 1 : CSERR# is forwarded to PCI. The default after reset is zero.
0	Parity Error Response Enable	This bit controls the R5C551's response to parity errors on the CardBus interface. 0 : Parity errors are ignored. 1 : Parity errors are reported. The default after reset is zero.

5.4.24 Subsystem Vendor ID register

Register Name:	Subsystem Vendor ID
Address offset:	40h-41h(16bit)
Default:	0000h
Access:	R/W

The R5C551 supports Subsystem Vendor ID register in order to correspond to the PC 98/99/2001 Design requirements. Setting Subsystem ID Write Enable bit (Bit6 in the Misc Control register) enables the system to write into this register. And also, this register is reflected the written value of C0h (Writable Subsystem Vendor ID register) independent of Write Enable bit. On use of the Serial ROM (SPKROUT is pull-down by an external resistor), Data is read from the Serial ROM. This register is initialized by only GBRST#.

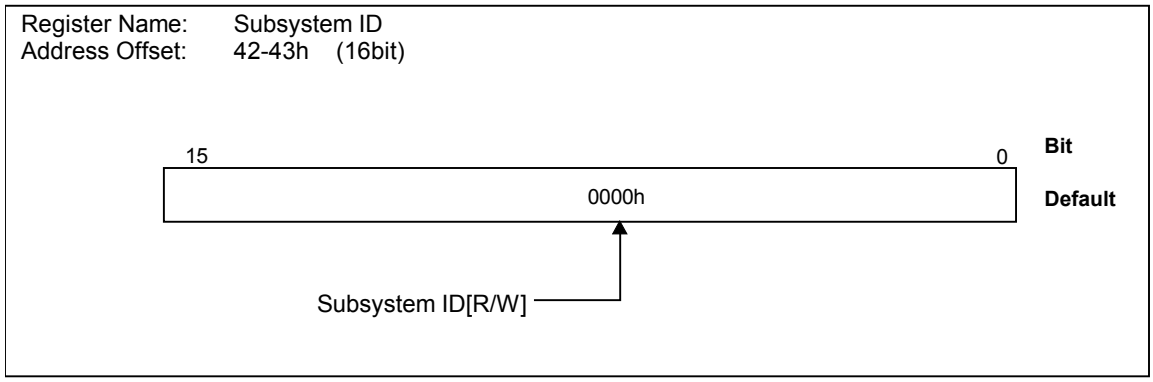


Bit	Field Name	Description
15-0	Subsystem Vendor ID	Setting Subsystem ID Write Enable bit (Bit6 in the Misc Control register) enables the system to write into this register. And also, this register is reflected the written value of C0h (Writable Subsystem Vendor ID register) independent of Write Enable bit. The default after reset is zeros.

5.4.25 Subsystem ID register

Register Name:	Subsystem ID
Address Offset:	42h-43h(16bit)
Default:	0000h
Access:	R/W

The R5C551 supports Subsystem ID register in order to correspond to the PC 98/99/2001 Design requirements. Setting Subsystem ID Write Enable bit (Bit6 in the Misc Control register) enabled to write into this register from the system. And also, this register is reflected the written value of C2h (Writable Subsystem ID register) independent of Write Enable bit. On use of the Serial ROM (SPKROUT is pull-down by an external resistor), Data is read from the Serial ROM. This register is initialized by only GBRST#.

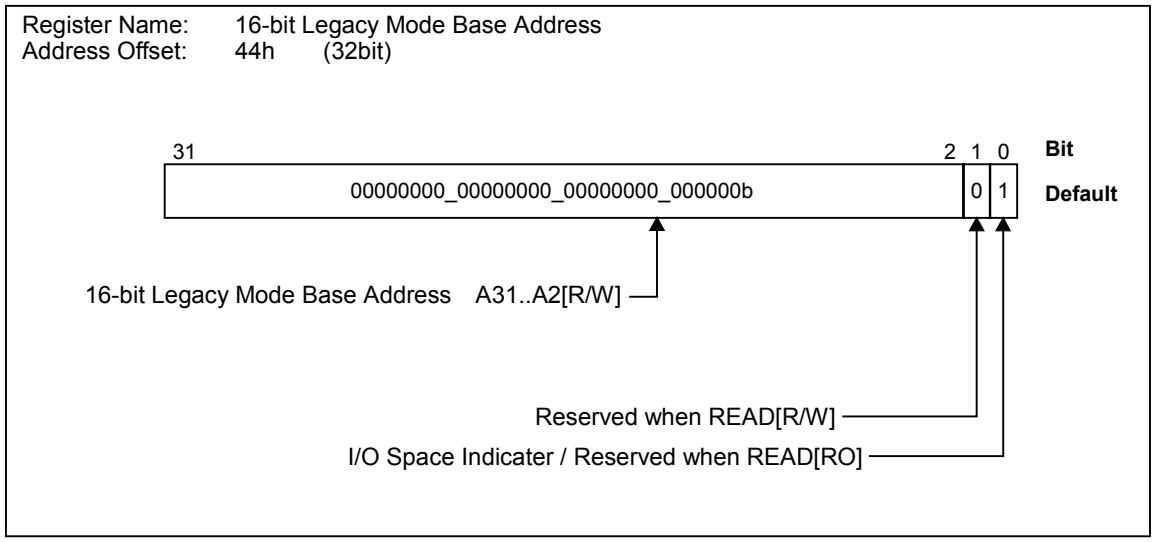


Bit	Field Name	Description
15-0	Subsystem ID	Setting Subsystem ID Write Enable bit (Bit6 in the Misc Control register) enabled to write into this register from the system. And also, this register is reflected the written value of C2h (Writable Subsystem ID register) independent of Write Enable bit. The default after reset is zeros.

5.4.26 16-bit Legacy Mode Base Address register

Register Name:	16-bit Legacy Mode Base Address
Address Offset:	44h-47h(32bit)
Default:	0000_0001h
Access:	R/W

The 16-bit Legacy Mode Base Address register indicates the base address to map the Legacy Port on the PCI Card-16. Normally, this register is set to 3E0h or 3E2h in order to keep corresponding to the PCIC. The bits [31:2] are read/write, but the bits [1:0] are hardwired to 01b when read. It dose not respond to PCI cycles unless specifically loaded with a non-zero address after PCIRST# is deasserted.

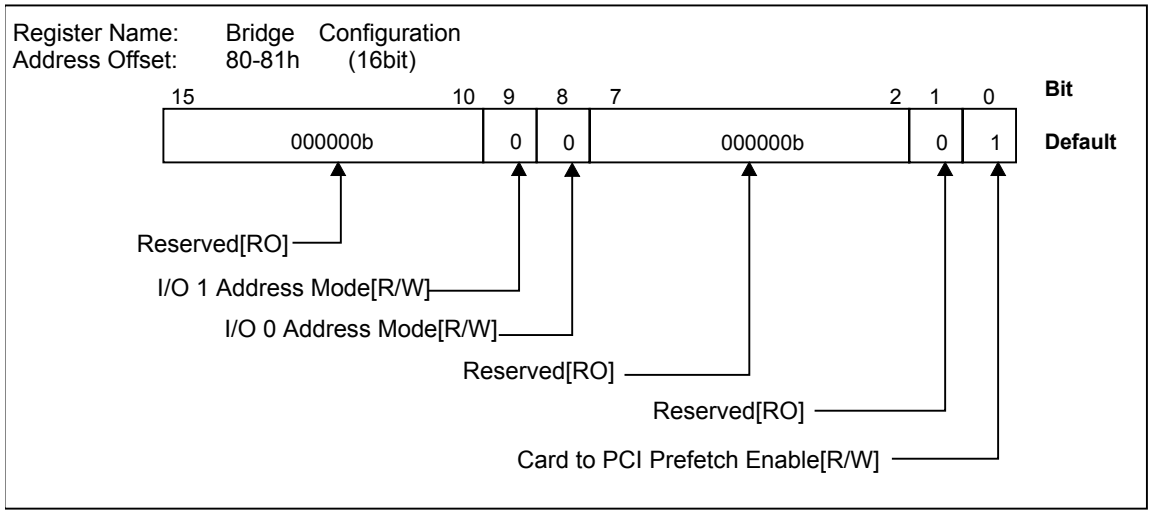


Bit	field Name	Description
31-2	16-bit Legacy Mode Base Address A31..A2	This field indicates the base address to map INDEX/DATA port (3E0h, 3E1h) corresponding to the PCIC when the PCI Card-16 is inserted. This field is read/write, and writing to this field has no effect. The default after reset is zero.
1	Reserved	This bit is enabled to write in a data, therefore this register can be 03E0h or 03E2h. This bit returns zero when read.
0	I/O Space Indicator	This bit indicates whether or not the Card Control register space indicated by the Base Address register is I/O space. This bit returns one when read.

5.4.27 Bridge Configuration register

Register Name:	Bridge Configuration
Address Offset:	80h-81h(16bit)
Default:	0001h
Access:	R/W

The Bridge Configuration register is used to control the bridge functions specific to the R5C551 like an I/O addressing mode and Perfectible memory transactions from CardBus to PCI bus. Each socket has its own Bridge Configuration register.

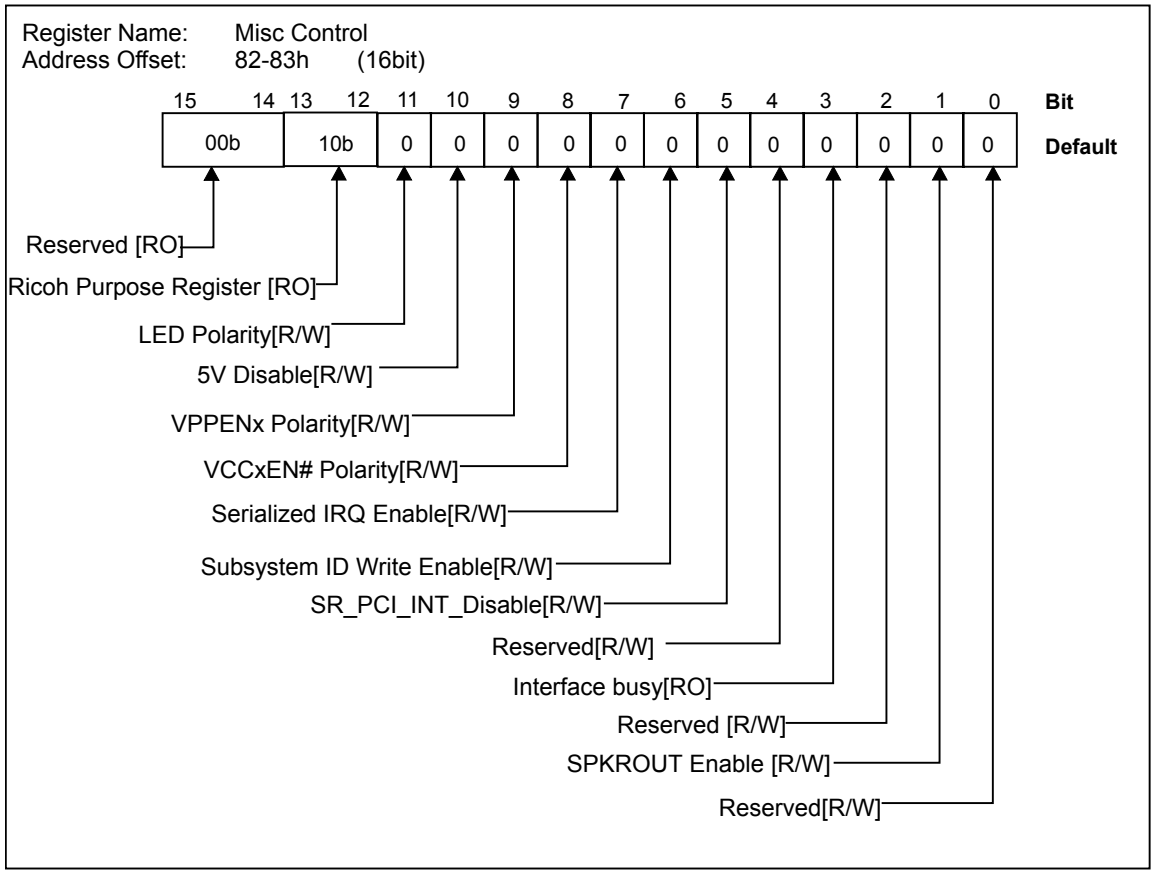


Bit	Field Name	Description
15-10	Reserved	These bits are reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.
9	I/O 1Address Mode	This bit controls the address size of I/O window #1. When this bit is set to one, the I/O Base #1 Upper register and the I/O Limit #1 Upper register are enabled. When this bit is set to zero, the I/O Base #1 Upper register and the I/O Limit #1 Upper register are disabled, and the I/O transaction is forwarded only when the upper 16-bit address [31:16] is zero. The default after reset is zero. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
8	I/O 0Address Mode	This bit controls the address size of I/O window #0. When this bit is set to one, the I/O Base #0 Upper register and the I/O Limit #0 Upper register are enabled. When this bit is set to zero, the I/O Base #0 Upper register and the I/O Limit #0 Upper register are disabled, and the I/O transaction is forwarded only when the upper 16-bit address [31:16] is zero. The default after reset is zero. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
7-2	Reserved	These bits are reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.
1	Reserved	This bit is reserved for future use. This bit is read-only and returns zero when read. Writing to this bit has no effect.
0	Card to PCI Prefetch Enable	When this bit is one, Read Prefetch is enabled from CardBus to PCI bus. The default after reset is one. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.

5.4.28 Misc Control register

Register Name:	Misc Control
Address Offset:	82h-83h(16bit)
Default:	2000h
Access:	R/W

The Misc Control register controls the power-down mode of the R5C551 the polarity of the card power enable signal, serial IRQ and Subsystem ID write signals enable/disable.

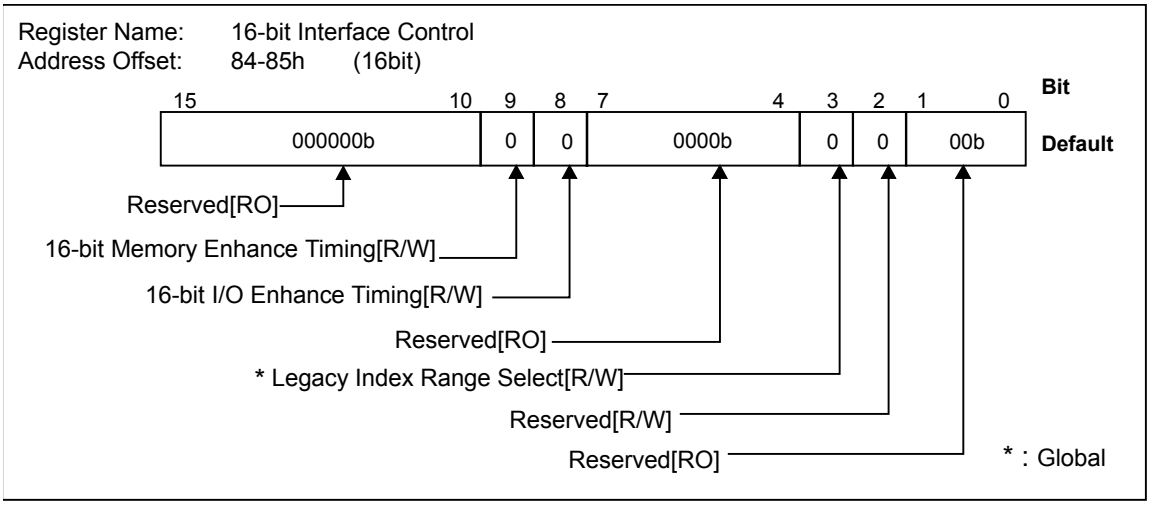


Bit	Field Name	Description
15-14	Reserved	These bits are reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.
13-12	Ricoh Purpose Register	This bit is reserved for future use. This field is read only. The default after reset is 10b. Do not write any value excepting “10b” into this field.
11	LED Polarity	This bit controls the polarity of LED signal. The default is zero and “low” active. When this bit is set to one, LED signal is “high” active. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
10	5V Disable	In the card supplied 5V/3.3V, 5V is disabled when this bit is set. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
9	VPPENx Polarity	This bit controls the polarity of VPPEN1 and VPPEN0 signals. When this bit is set to one, VPPEN1 and VPPEN0 are “low” active signals. When this bit is cleared, VPPEN1 and VPPEN0 are “high” active signals. The default after reset is zero. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
8	VCCxEN# Polarity	This bit controls the polarity of VCC5EN# and VCC3EN# signals. When this bit is set to one, VCC5EN# and VCC3EN# are “high” active signals. When this bit is cleared, VPPEN1 and VPPEN0 are “high” active signals. The default after reset is zero. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
7	SRIRQ Enable	When this bit is set, the serial IRQ mode is enabled. IRQ9 is assigned as SIRQ# signal that is an input pin. The default after reset is zero. When bit2 on the Misc Control 5 register is also set, SIRQ mode is enabled. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
6	Subsystem ID Write Enable	When this bit is set to one, Writing to Subsystem Vendor ID and Subsystem ID is enabled. The default after reset is zero.
5	SR_PCI_INT_Disable	When this bit is set to zero, The R5C551 can insert the frame of INTA#, INTB#, INTC#, and INTD# (PCI Interrupt signals) following IOCHK# frame. The default after reset is zero. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
4	Reserved	This bit is reserved for future use. This bit is read/write and returns zero when read. Writing to this bit has no effect.
3	Interface Busy	This bit is read-only. When this bit is set to one, the card interface is busy. Returns zero when the internal buffers are empty. The default after reset is zero.
2	Reserved	This bit is reserved for future use. This bit is read/write and returns zero when read. Writing to this bit has no effect.
1	SPKROUT Enable	When this bit is set to one, HWSPND# signal is reassigned as SPKROUT that is an output pin and either CAUDIO of CardBus card or SPKR# digital audio input data from 16 I/O card is output. The default after reset is zero.
0	Reserved	This bit is reserved for future use. This bit is read/write and returns zero when read. Writing to this bit has no effect.

5.4.29 16-bit Interface Control register

Register Name:	16-bit Interface Control
Address Offset:	84h-85h(16bit)
Default:	0000h
Access:	R/W

The 16-bit Interface Control register is used to set 16-bit interface timing and the PCIC compatible mode.

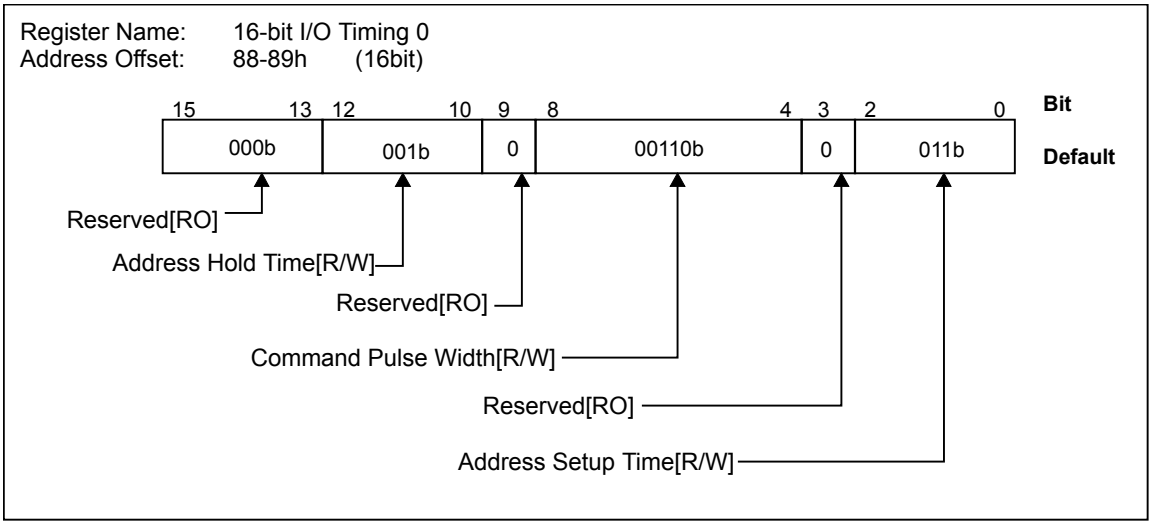


Bit	field Name	Description
15-10	Reserved	These bits are reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.
9	16-bit Memory Enhance Timing	When this bit is set to one, the 16-bit memory enhanced timing is enabled. 16-bit memory access timing is determined by 16-bit Memory Timing #0 register. When this bit is reset to zero, 16-bit memory access timing is reset to the default condition. The default after reset is zero. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
8	16-bit I/O Enhance Timing	When this bit is set to one, the 16-bit I/O enhanced timing is enabled. 16-bit I/O access timing is determined by 16-bit I/O Timing #0 register. When this bit is reset to zero, 16-bit I/O timing is reset to the default condition. The default after reset is zero. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
7-4	Reserved	These bits are reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.
3	Legacy Index Range Select	This bit cannot set it in the R5C551.
2	Reserved	This bit is reserved for future use. The default after reset is zero.
1-0	Reserved	These bits are reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.

5.4.30 16-bit I/O Timing 0 register

Register Name:	16-bit I/O Timing 0
Address Offset:	88h-89h(16bit)
Default:	0463h
Access:	R/W

16-bit I/O access timing parameters are independently configured for each socket by programming this register.

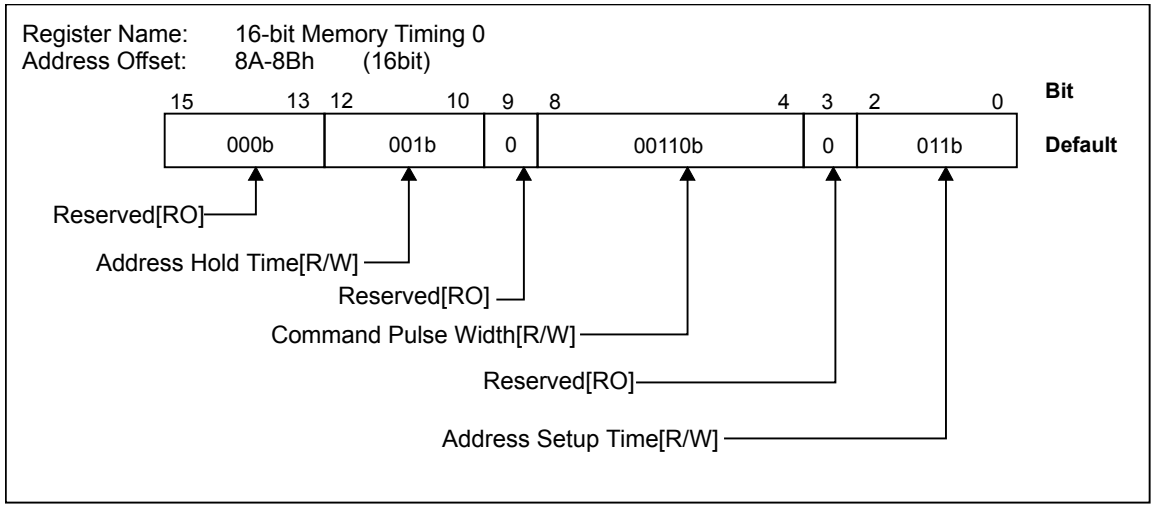


Bit	Field Name	Description
15-13	Reserved	These bits are reserved for future use. This field is read-only and returns zeros when read. Writing to this field has no effect.
12-10	Address Hold Time	This field indicates the address hold time of 16-bit I/O cycle. The hold time can be set in a timer granularity of PCICLK. The default after reset is 001b. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
9	Reserved	This bit is reserved for future use. This bit is read-only and returns zero when read. Writing to this bit has no effect.
8-4	Command Pulse Width	This field indicates the command pulse width of 16-bit I/O cycle for IORD# and IOWR#. The pulse width can be set in a timer granularity of PCICLK. The default after reset is 00110b. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
3	Reserved	This bit is reserved for future use. This bit is read-only and returns zero when read. Writing to this bit has no effect.
2-0	Address Setup Time	This field indicates the address setup time of 16-bit I/O cycle. The setup time can be set in a timer granularity of PCICLK. The default after reset is 011b. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.

5.4.31 16-bit Memory Timing 0 register

Register Name:	16-bit Memory Timing 0
Address offset:	8Ah-8Bh(16bit)
Default:	0463h
Access:	R/W

16-bit Memory access timing parameters are independently configured for each socket by programming this register.

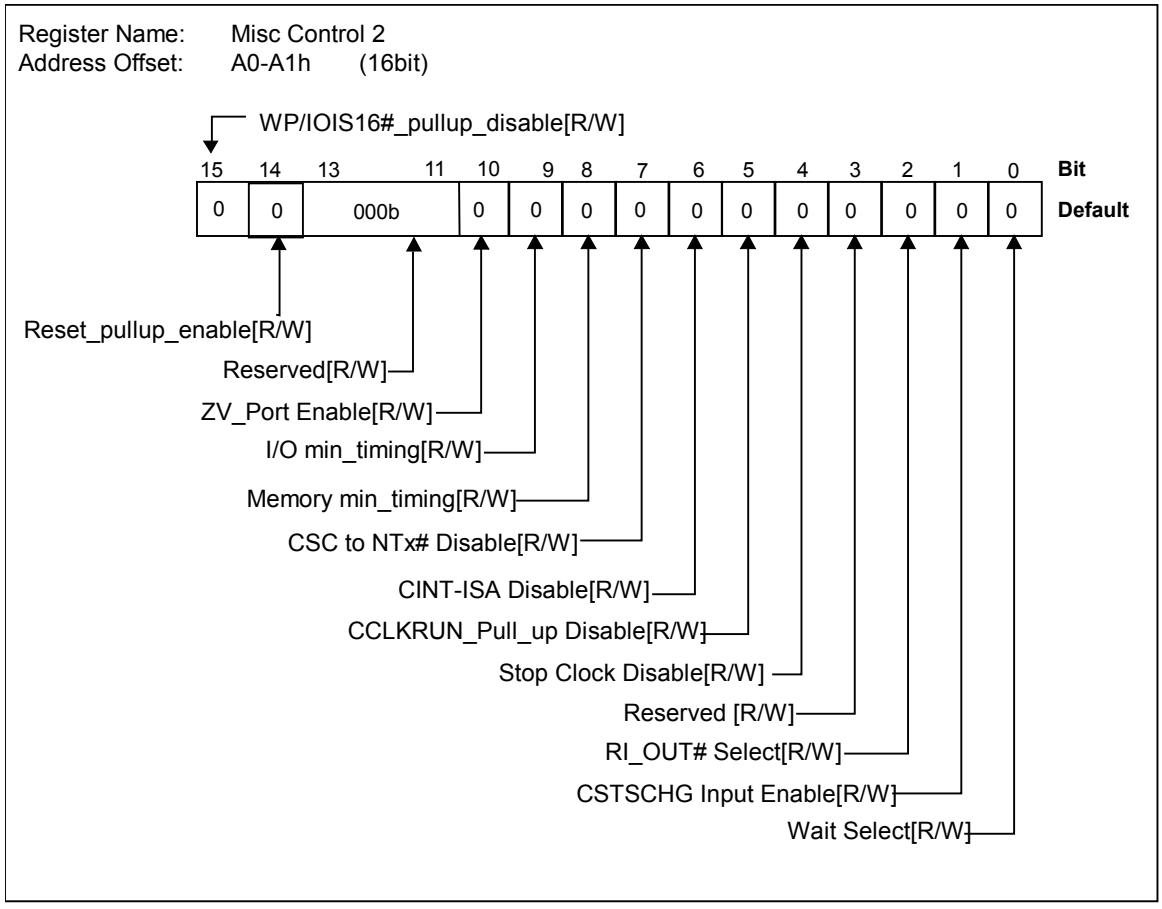


Bit	Field Name	Description
15-13	Reserved	These bits are reserved for future use. This field is read-only and returns zeros when read. Writing to this bit has no effect.
12-10	Address Hold Time	This field indicates the address hold time of 16-bit memory cycle. The hold time can be set in a timer granularity of PCICLK. The default after reset is 001b. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
9	Reserved	This bit is reserved for future use. This bit is read-only and returns zero when read. Writing to this bit has no effect.
8-4	Command Pulse Width	This field indicates the command pulse width of 16-bit memory cycle for OE# and WE#. The pulse width can be set in a timer granularity of PCICLK. The default after reset is 00110b. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
3	Reserved	This bit is reserved for future use. This bit is read-only and returns zero when read. Writing to this bit has no effect.
2-0	Address Setup Time	This field indicates the address setup time of 16-bit memory cycle. The setup time can be set in a timer granularity of PCICLK. The default after reset is 011b. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.

5.4.32 Misc Control 2 register

Register Name:	Misc Control 2
Address Offset:	A0h-A1h (16 bit)
Default:	0000h
Access:	R/W

The Misc Control 2 register indicates each kinds of control for the R5C551. This register is initialized by only GBRST#.

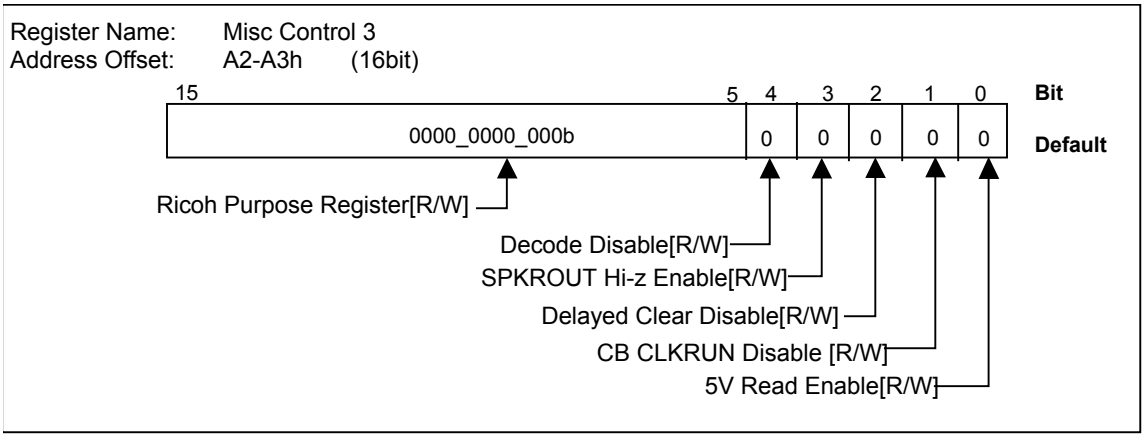


Bit	Field Name	Description
15	WP/IOIS16#_pullup _disable	When this bit is set to one, an internal pull-up of the WP/IOIS16# signal on 16bit mode is disabled. The default after reset is zero. Therefore, inserting the 16bit card on default makes this signal pull-up. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
14	Reset_pullup_enable	When this bit is set to one, an internal pull-up of the RESET signal is enabled. The default after reset is zero. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
13-11	Reserved	These bits are reserved for future use. This field is read/write. The default after reset is zero.
10	ZV_Port Enable	When this bit is set to one, ZV Port is enabled as the Misc Control 1 (82Fh) in the EXCA register. (When either one is set, ZV Port is enabled.) The default after reset is zero.
9	I/O min_timing	When this bit is set to one, 16bit I/O Enhance Timing is enabled and Minimum timing is set compulsory. The default after reset is zero. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
8	Memory min_timing	When this bit is set to one, 16bit Memory Enhance Timing is enabled and Minimum timing is set compulsory. The default after reset is zero. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
7	CSC to INT# Disable	On the default, the 16bit status Change interrupt signal is output to either INTA# or INTB#. When this bit is set to one, it is output to the ISA interrupt signal only. The default after reset is zero. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
6	CINT-ISA Disable	When this bit is set to one, CINT# is disable to output to the ISA interrupt signal by the IREQ-ISA Enable bit of the Bridge Control register (3Eh). The default after reset is zero. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
5	CCLKRUN_Pull-up Disable	When this bit is set to one, this pin must have an external pull-up. Because setting this bit to one disables an internal pull-up of the CCLKRUN pin on CardBus. Details see the serial ROM in Chapter 4.
4	Stop Clock Disable	When this bit is set to one, the Stop Clock bit of the CardBus register is disabled. The default after reset is zero. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
3	Reserved	This bit is reserved for future use. This bit is read/write. The default after reset is zero. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
2	RI_OUT# Select	When this bit is set to one, the PME# pin is enabled to work as RI_OUT# only on D0 State. But, if PME_En bit is set to one even if the D0 State is on, it works as PME#. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
1	CSTSCHG Input Enable	When this bit is set to one, CSTSCHG Input signal is enabled and WOL (Wake On LAN) is supported even if VCC_3V power is off. When this bit is cleared, CSTSCHG Input signal is disabled. The default after reset is zero. But, when the card is off, CSTSCHG Input signal is disabled even if this bit is set. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
0	Wait Select	When this bit is set to one, the internal wait time of the device is extended for one clock. That is, when the WAIT# for the 16bit card is asserted, the width of command pulse is extended for one clock. The default after reset is zero. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.

5.4.33 Misc Control 3 register

Register Name: Misc Control 3
Address Offset: A2h-A3h (16 bit)
Default: 0000h
Access: R/W

The Misc Control 3 register indicates each kind of controls for the R5C551 as the Misc Control 2.

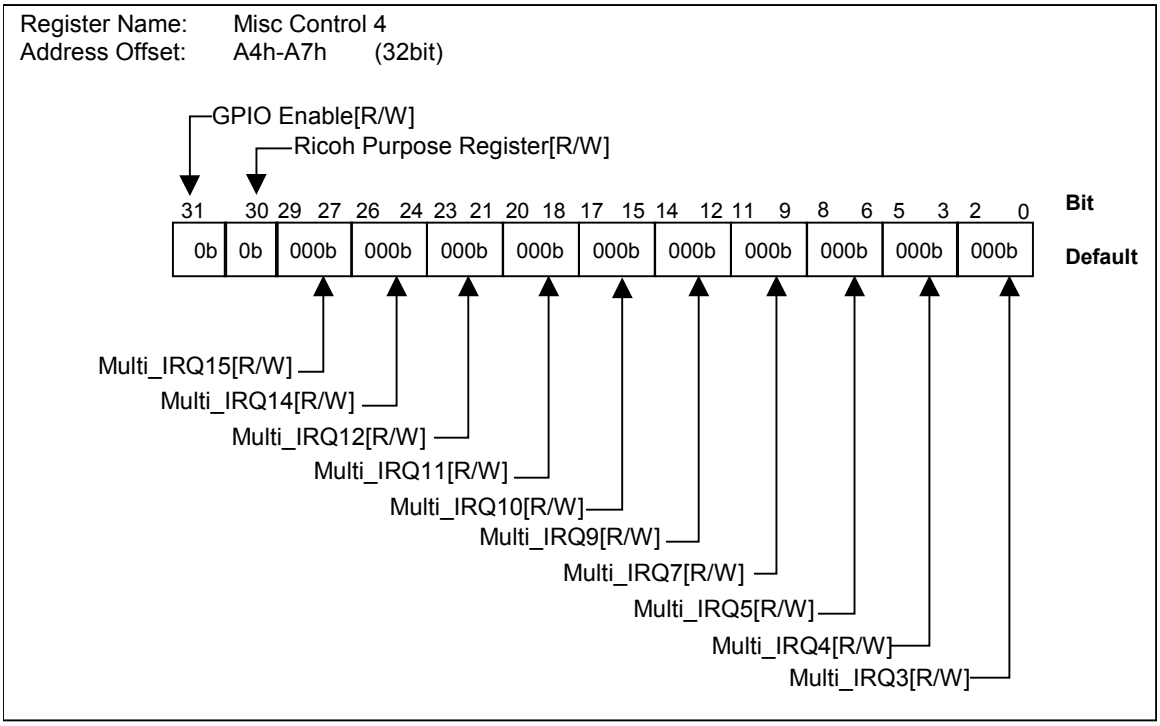


Bit	Field Name	Description
15-5	Ricoh Purpose Register	These bits are reserved for future use. This field is read only. The default after reset is zero. Do not write any value excepting "0" into this field.
4	Decode Disable	When this bit is set to one, NotACard is enabled under the conditions of detecting the card. When this is cleared, as the 16bit card for 5V is detected. The default after reset is 0b. CD2# / CD1# / VS2# / VS1# ground / ground / ground / open Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
3	SPKROUT Hi-z Enable	When this bit is set to one, SPKROUT output is forced to be Hi-z on HW_Suspend mode. But when this bit is cleared, it is not. The default after reset is 0b. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
2	Delayed Clear Disable	The R5C551 repeats to retry on the Delayed transaction until the transaction for the CardBus Card is finished. On default, when the R5C551 recognizes an abnormality to repeat retrying for 2 msec, the R5C551 will stop the transaction. But, when this bit is set to one, the R5C551 will not stop the transaction, and repeat to retry until the transaction for CardBus card is finished. (This bit is usually used when WAIT# is long on the 16bit card is asserted.) Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
1	CB CLKRUN Disable	When this bit is set to one, Host's CLKRUN request is refused on the CardBus Card. The default after reset is zero. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
0	5V Read Enable	When the R5C551 is inserted a 3.3V/5V Card, as the 3V Card bit of the Socket Present State register (008h) is set to one, the 5V Card bit is not. But, both are enabled to set by setting this bit to one. When this bit is set to one, note that the 5V Card bit is set by inserting a 3V Card. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.

5.4.34 Misc Control 4 register

Register Name:	Misc Control 4
Address Offset:	A4h-A7h (32 bit)
Default:	0000_0000h
Access:	R/W

The Misc Control 4 register is used to define the IRQ3-15 pins. These pins are defined as the following functions. The default is IRQ3-15. This register is initialized by only GBRST#.



Bit	Field Name	Description
31	GPIO Enable	When this bit is set to zero, GPIO outputs assigned to IRQ [3,4,5,7] pins become Hi-Z and GPIO inputs are disabled. When it is set to one, setting of the General Purpose I/O 1 register (the PCI Config.AAh) or the General Purpose I/O register (83Ah) is done. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
30	Ricoh Purpose Register	This bit is reserved for future use. This bit is read only. The default after reset is zero. Do not write any value excepting “0” into this bit.

Bit	Field Name	Description
29-27	Multi_IRQ15	This field defines IRQ15 as follows. The default after reset is zero. 000 - IRQ15/LED1394# (default) / (default on S-IRQ mode) 001 - LED1394# 010 - D3STATE 011 - LED# 100 - ZVEN# 101 - HI-Z 110 - SPKROUT 111 - IRQ5 Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
26-24	Multi_IRQ14	This field defines IRQ14 as follows. The default after reset is zero. 000 - IRQ14 (default) / (default on S-IRQ mode) 001 - LED1394# 010 - LED# 011 - ZVEN# 100 - IRQ4 101 - HI-Z 110 - SPKROUT 111 - D3STATE Notes: This field cannot be multiple if using Serial ROM. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
23-21	Multi_IRQ12	This field defines IRQ12 as follows. The default after reset is zero. 000 - IRQ12 (LEDOUT) Setting Programmable bit (16bitReg.81Fh-bit1) (default) 001 - LED1394# 010 - LED# 011 - ZVEN# 100 - IRQ3 101 - HI-Z 110 - SPKROUT 111 - D3STATE Notes: This field cannot be multiple if using Serial ROM. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
20-18	Multi_IRQ11	This field defines IRQ11 as follows. The default after reset is zero. 000 - IRQ11 (default) / (default on S-IRQ mode) 001 - LED1394# 010 - D3STATE 011 - LED# 100 - ZVEN# 101 - HI-Z 110 - SPKROUT 111 - IRQ12 (LEDOUT) Setting Programmable bit (16bitReg.81Fh-bit1) Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
17-15	Multi_IRQ10	This field defines IRQ10 as follows. The default after reset is zero. 000 - IRQ10/LED# (default)/(default on S-IRQ mode) 001 - LED1394# 010 - LED# 011 - ZVEN# 100 - IRQ12 (LEDOUT) Setting Programmable bit (16bitReg.81Fh-bit1) 101 - IRQ15 110 - SPKROUT 111 - HI-Z Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.

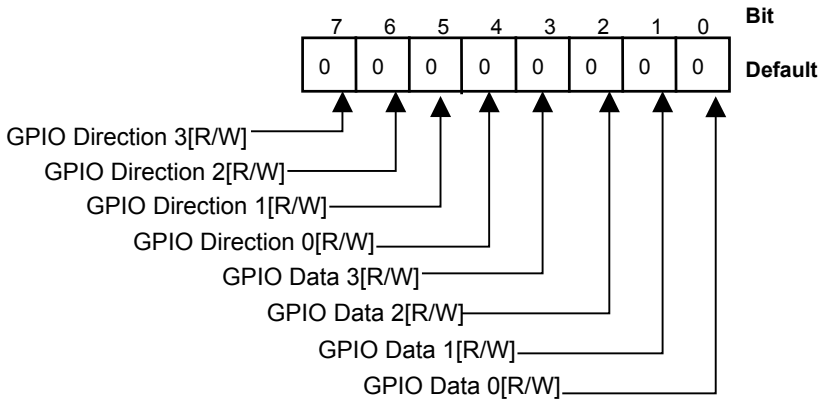
Bit	Field Name	Description
14-12	Multi_IRQ9	This field defines IRQ9 as follows. On S-IRQ mode, this field cannot be multiple (fix on SRIRQ#). The default after reset is zero. 000 - IRQ9/SRIRQ# (default)/(default on S-IRQ mode) 001 - LED1394# 010 - IRQ12 (LEDOUT) Setting Programmable bit (16bitReg.81Fh-bit1) 011 - ZVEN# 100 - LED# 101 - IRQ15 110 - SPKROUT 111 - HI-Z Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
11-9	Multi_IRQ7	This field defines IRQ7 as follows. The default after reset is zero. 000 - IRQ7/GPIO3 (default)/(default on S-IRQ mode) 001 - LED1394# 010 - IRQ14 011 - LED# 100 - ZVEN# 101 - HI-Z 110 - SPKROUT 111 - GPIO3 Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
8-6	Multi_IRQ5	This field defines IRQ5 as follows. The default after reset is zero. 000 - IRQ5/GPIO2 (default)/(default on S-IRQ mode) 001 - LED1394# 010 - IRQ12 (LEDOUT) Setting Programmable bit (16bitReg.81Fh-bit1) 011 - LED# 100 - ZVEN# 101 - HI-Z 110 - SPKROUT 111 - GPIO2 Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
5-3	Multi_IRQ4	This field defines IRQ4 as follows. The default after reset is zero. 000 - IRQ4/GPIO1 (default)/(default on S-IRQ mode) 001 - LED1394# 010 - D3STATE 011 - LED# 100 - ZVEN# 101 - HI-Z 110 - SPKROUT 111 - GPIO1 Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
2-0	Multi_IRQ3	This field defines IRQ3 as follows. The default after reset is zero. 000 - IRQ3/GPIO0 (default)/(default on S-IRQ mode) 001 - LED1394# 010 - IRQ12 (LEDOUT) Setting Programmable bit (16bitReg.81Fh-bit1) 011 - LED# 100 - ZVEN# 101 - HI-Z 110 - SPKROUT 111 - GPIO0 Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.

5.4.35 General Purpose I/O 1 register

Register Name:	General Purpose I/O 1
Address Offset:	AAh (8bit)
Default:	00h
Access:	R/W

The R5C551 assigns IRQ [3,4,5,7] pins to GPIO (General Purpose I/O) pins when serial IRQ mode is selected and the GPIO Enable bit of the Misc Control 4 register is set. User can be free to use these I/O pins. When GPIO Enable bit is set to one, the default of GPIO is Input mode. And Bit [3:0] indicates the state of mode. In Output mode, GPIO [3:0] output the contents written in each bit. This register linking to the General Purpose I/O register reflects the General Purpose I/O register (83Ah). On the other hand, the General Purpose I/O register also reflects this register.

Register Name: General Purpose I/O 1
Address Offset: AAh (8 bit)

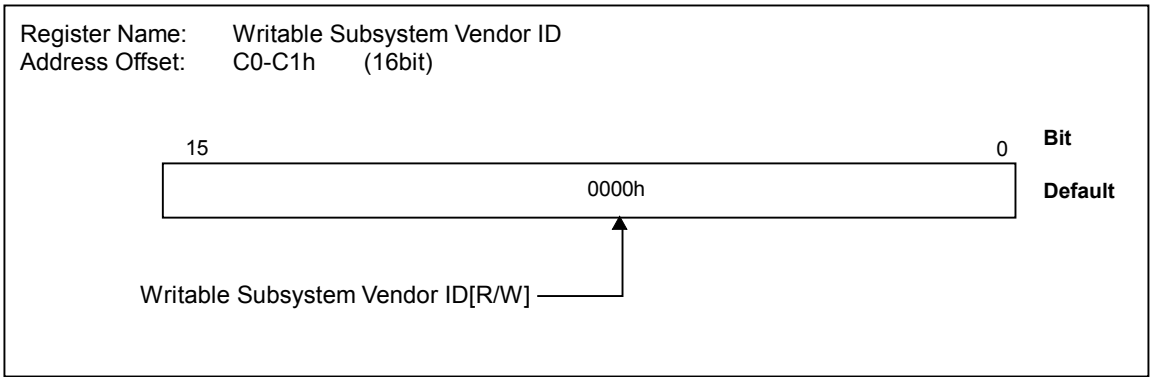


Bit	Field Name	Description
7	GPIO Direction 3	This bit is an I/O changeover signal for GPIO Data 3. GPIO Data 3 is input when this bit is set to 0, and it is output when this bit is set to 1. The default after reset is 0b.
6	GPIO Direction 2	This bit is an I/O changeover signal for GPIO Data 2. GPIO Data 2 is input when this bit is set to 0, and it is output when this bit is set to 1. The default after reset is 0b.
5	GPIO Direction 1	This bit is an I/O changeover signal for GPIO Data 1. GPIO Data 1 is input when this bit is set to 0, and it is output when this bit is set to 1. The default after reset is 0b.
4	GPIO Direction 0	This bit is an I/O changeover signal for GPIO Data 0. GPIO Data 0 is input when this bit is set to 0, and it is output when this bit is set to 1. The default after reset is 0b.
3	GPIO Data 3	General Purpose I/O bit 3. The default is input.
2	GPIO Data 2	General Purpose I/O bit 2. The default is input.
1	GPIO Data 1	General Purpose I/O bit 1. The default is input.
0	GPIO Data 0	General Purpose I/O bit 0. The default is input.

5.4.36 Writable Subsystem Vendor ID register

Register Name:	Writable Subsystem Vendor ID
Address Offset:	C0h-C1h (16bit)
Default:	0000h
Access:	R/W

Writable Subsystem Vendor ID register operates as same as 40h(Subsystem Vendor ID register). The value written in this register is enabled to read through 40h as Subsystem Vendor ID.

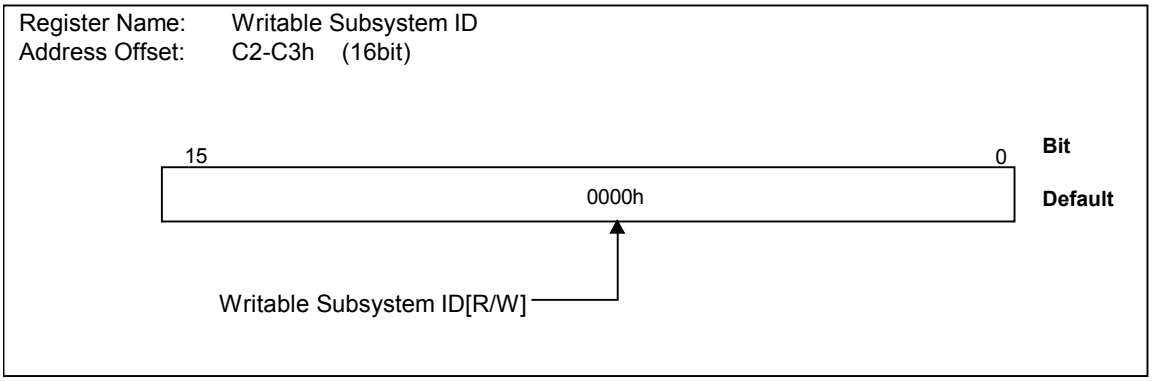


Bit	Field Name	Description
15-0	Writable Subsystem Vendor ID	Writable Subsystem Vendor ID register operates as same as 40h(Subsystem Vendor ID register). The value written in this register is enabled to read through 40h as Subsystem Vendor ID. The default after reset is 0000h.

5.4.37 Writable Subsystem ID register

Register Name:	Writable Subsystem ID
Address Offset:	C2h-C3h (16bit)
Default:	0000h
Access:	R/W

Writable Subsystem ID register operates as same as 42h(Subsystem ID register). The value written in this register is enabled to read through 42h as Subsystem ID.



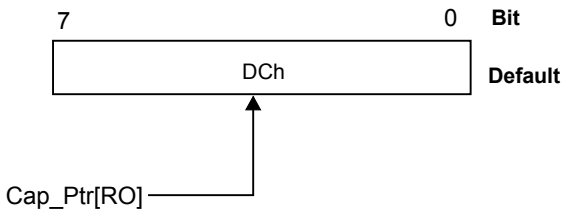
Bit	Field Name	Description
15-0	Writable Subsystem ID	Writable Subsystem ID register operates as same as 42h(Subsystem ID register). The value written in this register is enabled to read through 42h as Subsystem ID. The default after reset is 0000h.

5.4.38 Capabilities Pointer register

Register Name:	Capabilities Pointer
Address Offset:	14h (8 bit)
Default:	DCh
Access:	RO

The Capabilities Pointer register is read-only and provides an offset into the function's PCI Configuration Space for the location of the first item in the New Capabilities List. The R5C551 supports the PCI Power Management. This register is assigned a value of 0DCh for the PCI Power Management.

Register Name: Capabilities Pointer register
Address Offset: 14h (8bit)



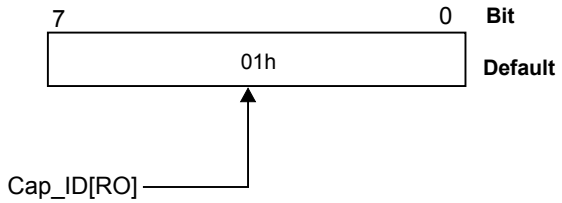
Bit	Field Name	Description
7-0	Capabilities Pointer	This field provides an offset into the function's PCI Configuration Space for the location of the first item in the New Capabilities Linked List. The R5C551 supports the PCI Power Management as a new function. This field is assigned a value of DCh for the PCI Power Management.

5.4.39 Capabilities Identifier register

Register Name:	Capabilities Identifier
Address Offset:	DCh (8 bit)
Default:	01h
Access:	RO

The Capabilities Identifier register is read-only and indicates only one item in the linked list is the register defined for the PCI Power Management. This register is assigned the ID of 01h.

Register Name: Capabilities Identifier register
Address Offset: Cap_Ptr (8bit)



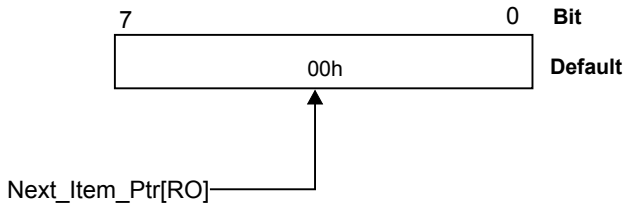
Bit	Field Name	Description
7-0	Capabilities Identifier	This field indicates the R5C551 support the PCI Power Management as a new function. This field is read-only and assigned the ID of 01h.

5.4.40 Next Item Pointer register

Register Name:	Next Item Pointer
Address Offset:	DDh (8 bit)
Default:	00h
Access:	RO

The Next Item Pointer register is read-only and indicates the location of the next item in the function's capability list. The R5C551 doesn't support items in the list except the PCI Power Management. So, this field is assigned a value of 00h.

Register Name: Next Item Pointer register
Address Offset: DDh (8bit)

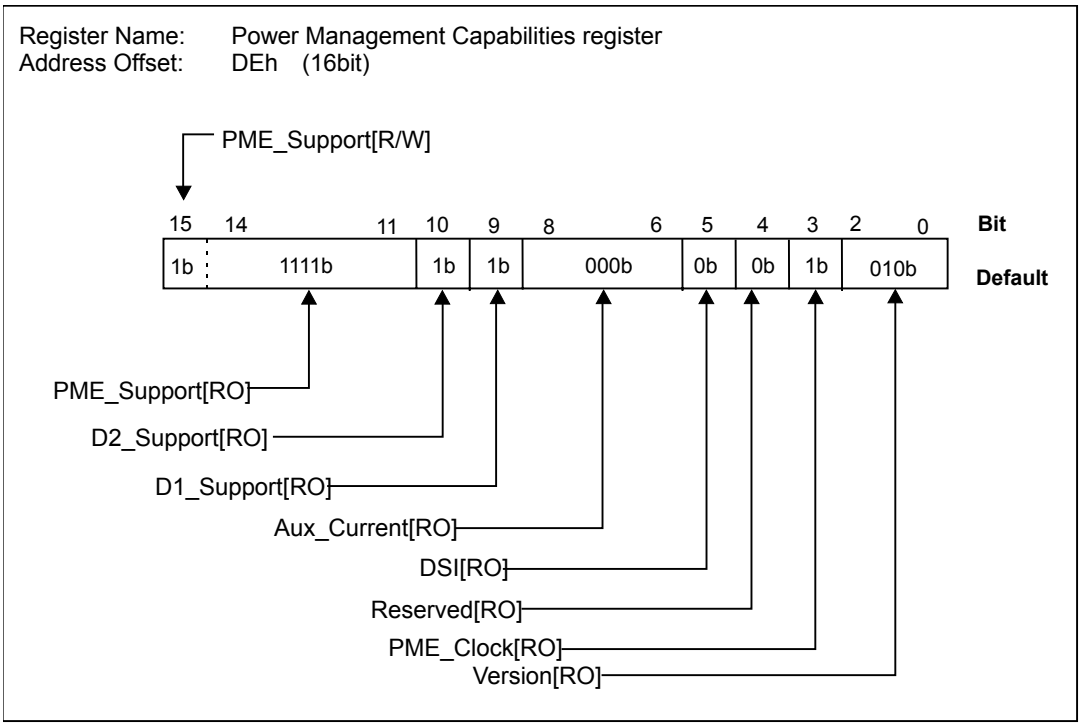


Bit	Field Name	Description
7-0	Next Item Pointer	This field indicates the location of the next item in the function's capability list. The R5C551 does not support items in the list except the PC Power Management. This field is read-only and assigned a value of 00h.

5.4.41 Power Management Capabilities register

Register Name:	Power Management Capabilities
Address Offset:	DEh (16 bit)
Default:	FE0Ah
Access:	RO

The Power Management Capabilities register is read-only and provides information on the capabilities of the function related to the PCI Power Management.

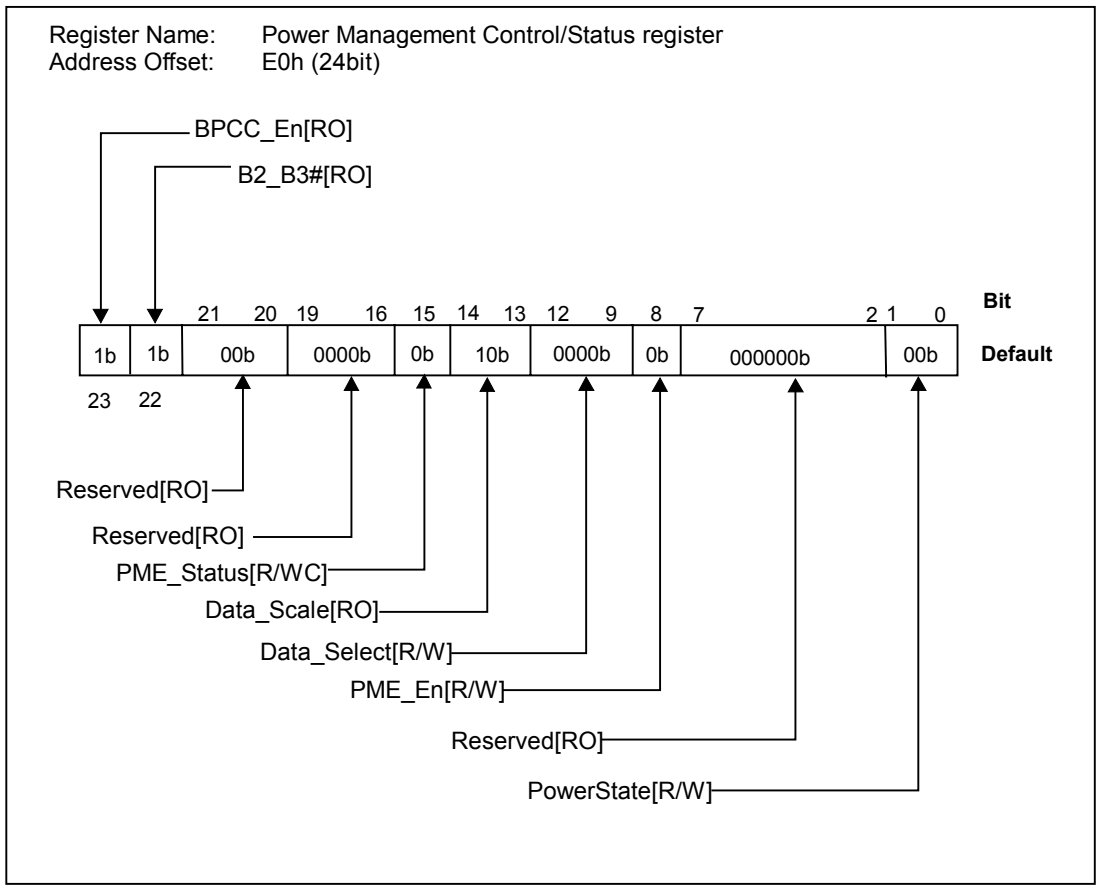


Bit	Field Name	Description
15 14-11	PME_Support	This 4-bit field indicates the power states that the device supports asserting PME#. A value of 0 for any bit indicates that the function is not capable of asserting the PME# signal from that power state. XXX1b - PME# can be asserted from **D0** (bit 11) XX1Xb - PME# can be asserted from **D1** (bit 12) X1XXb - PME# can be asserted from **D2** (bit 13) 1XXXb - PME# can be asserted from **D3**hot (bit 14) Bit 15 is set to one if PME# can be asserted by the supply of auxiliary power, even if the PCI Vcc is turned off. If the auxiliary power is not supported, this bit must be set to zero because PME# is not asserted. The PME# signal indicates Wakeup events that include a “Ring Indication” from a Modem or the receipt of special packet by a Network card. When once PME# is asserted, it is kept at the state until Status bit (bit 15) is cleared or Enable bit (bit 8) is reset in the Power Management Control/Status register.
10	D2_Support	Returns one, because the R5C551 supports the D2 Power Management State.
9	D1_Support	Returns one, because the R5C551 supports the D1 Power Management State.
8-6	Aux_Current	This 3-bit field indicates the 3.3Vaux auxiliary current requirements for the PCI function. Return zeros on read.
5	DSI	This Device Specific Initialization bit is set to one when a device specific device driver is required to reinitialize a device after it leaves the D3 state. Returns zero as it is not necessary to reinitialize in the R5C551.
4	Reserved	Reserved. Returns zero.
3	PME clock	When this bit is a “1” it indicates that the function relies on the presence of the PCI clock for PME# operation. When this bit is a “0” it indicates that no PCI clock is required for the function to generate PME#. This bit returns one because the R5C551 needs PCI clock to generate PME# when the power management event is caused by Card detect change, Ready/Busy change or Battery Warning. The R5C551 can generate PME# without PCI clock if PME is caused by Card status change.
2-0	Version	The R5C551 has 4 bytes of general purpose Power Management registers implemented as described in PCI Bus Power Management specification Rev1.1. These bits usually return 010b.

5.4.42 Power Management Control/Status register

Register Name:	Power Management Control/Status
Address Offset:	E0h (24 bit)
Default:	C04000h
Access:	R/W

The Power Management Control/Status register is used to control the current power state of the PCI function and inform the status information. The contents of this register are not affected by the internally generated reset caused by the transition from D3 to D0.



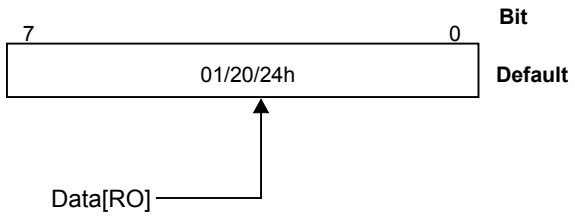
Bit	Field Name	Description
23	BPCC_En	This is Bus Power Clock Control Enable bit. Returns one as the bus power and clock control mechanism in the CardBus follows the power managing state of the R5C551.
22	B2_B3#	The state of this bit determines the action that is to occur as a direct result of programming the function to D3hot. A “1” indicates that when the bridge function is programmed to D3hot, its secondary bus’s PCI clock will be stopped (B2). A “0” indicates that when the bridge function is programmed to D3hot, its secondary bus will have its power removed (B3). Returns one as the CardBus clock will be stopped when the R5C551 function is programmed to D3hot.
21-16	Reserved	Reserved. Return zeros when read.
15	PME_Status	This bit is set when the function normally asserts the PME# signal independent of the state of the PME_En bit (bit 8). Writing a one to this bit clears it and causes the function to stop asserting a PME# (if enabled). Writing a zero has no effect. The default after reset is zero.
14-13	Data_Scale	This 2-bits read-only field indicates the scaling factor to be used when interpreting the value of the Data register. Returns 10b as the R5C551 offers the information of power consumed in a 10mW step.
12-9	Data_Select	This 4-bits field is used to select which data is reported through the Data register and Data_Scale field. The default after reset is zero. 0000 D0 power consumed 0001 D1 power consumed 0010 D2 power consumed 0011 D3 power consumed 0100 D0 power dissipated 0101 D1 power dissipated 0110 D2 power dissipated 0111 D3 power dissipated 1xxx Reserved
8	PME_En	When this bit is set, the function is enabled to assert PME#. When this bit is cleared, assertion of PME# is disabled. The default after reset is zero.
7-2	Reserved	Reserved. Return zeros when read.
1-0	PowerState	This field is used to set the function into a new power state. The definition of the field values is: 00b - D0 01b - D1 10b - D2 11b - D3 The default after reset is zeros.

5.4.43 Data Register

Register Name:	Data
Address Offset:	E3h (8 bit)
Default:	01h / 20h / 24h
Access:	RO

The Date register is read-only and provides a maximum value of the power consumed for each function from the PCI device by using with Data_Select bit fields and Data_Scale bit field.

Register Name: Data register
Address Offset: E3h (8bit)



Bit	Field Name	Description
7-0	Data	This read-only bit field provides the maximum value of the power consumed by the R5C551 for each function from the PCI device. The maximum value of the power consumed is 10mW times the value of Data_Scale bit field. The R5C551 returns the following value. D0 power state : 0010 0100b (360mW) D1 power state : 0010 0000b (320mW) D2 power state : 0000 0001b (10mW) D3 power state : 0000 0001b (10mW)

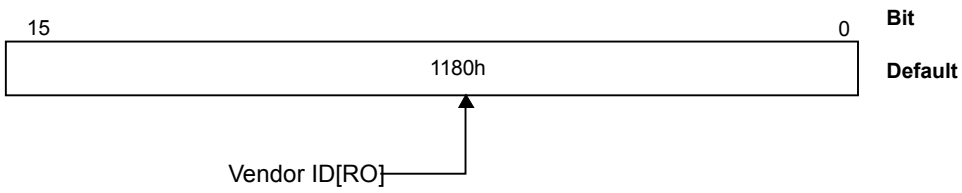
5.5 1394 Configuration register (Function #1)

5.5.1 Vendor ID register

Register Name:	Vendor ID [1394]
Address Offset:	00h-01h (16bit)
Default:	1180h
Access:	RO

This is a unique 16-bit value that is assigned to Vendor Identification, and it is used with the Device ID in order to identify each PCI device. Writing to this register has no effect.

Register Name: Vendor ID
Address Offset: 00-01h



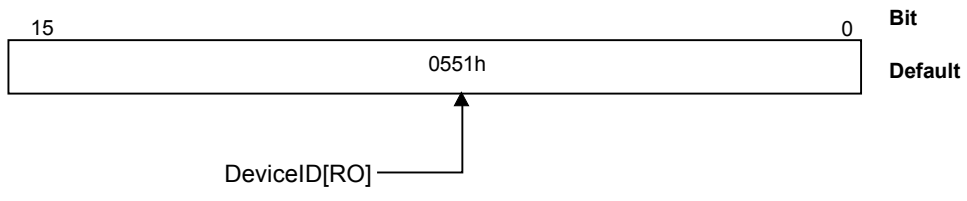
Bit	Field Name	Description
15-0	Vendor ID	This read-only field is the Vendor identification assigned to RICOH by the PCI Special Interest Group. This field always returns 1180h when read.

5.5.2 Device ID register

Register Name:	Device ID [1394]
Address Offset:	02h-03h(16bit)
Default:	0551h
Access:	RO

This is a unique 16-bit value that is assigned to the PCI CardBus Bridge function, and it is used with the Vendor ID in order to identify each PCI device. Writing to this register has no effect.

Register Name: Device ID
Address Offset: 02-03h (16bit)

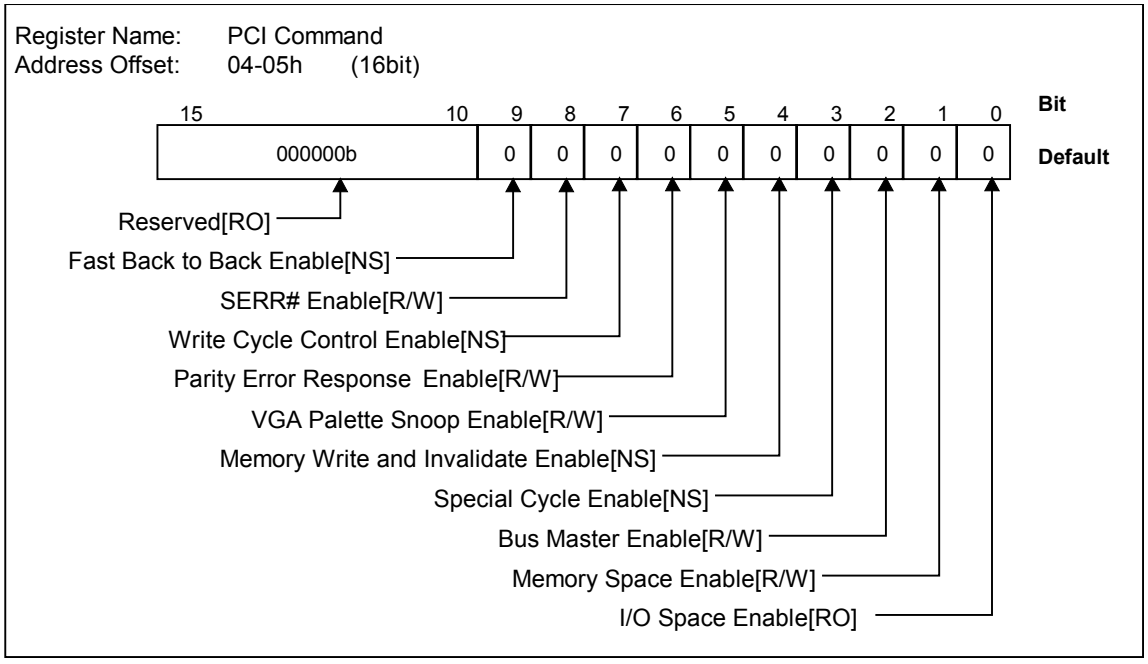


Bit	Field Name	Description
15-0	Device ID	This read-only field is the device identification assigned to the R5C551 by RICOH. This field always returns 0551h when read.

5.5.3 PCI Command register

Register Name:	PCI Command [1394]
Address Offset:	04h-05h(16bit)
Default:	0000h
Access:	R/W

The PCI Command Register controls the R5C551's responses to PCI Bus transactions on the primary interface. When this register has a value of '0', the function accepts only configuration accesses. The bits, with the exception of VGA Palette Snoop bit, in this register adhere to the definitions in the PCI Local Bus Specification.

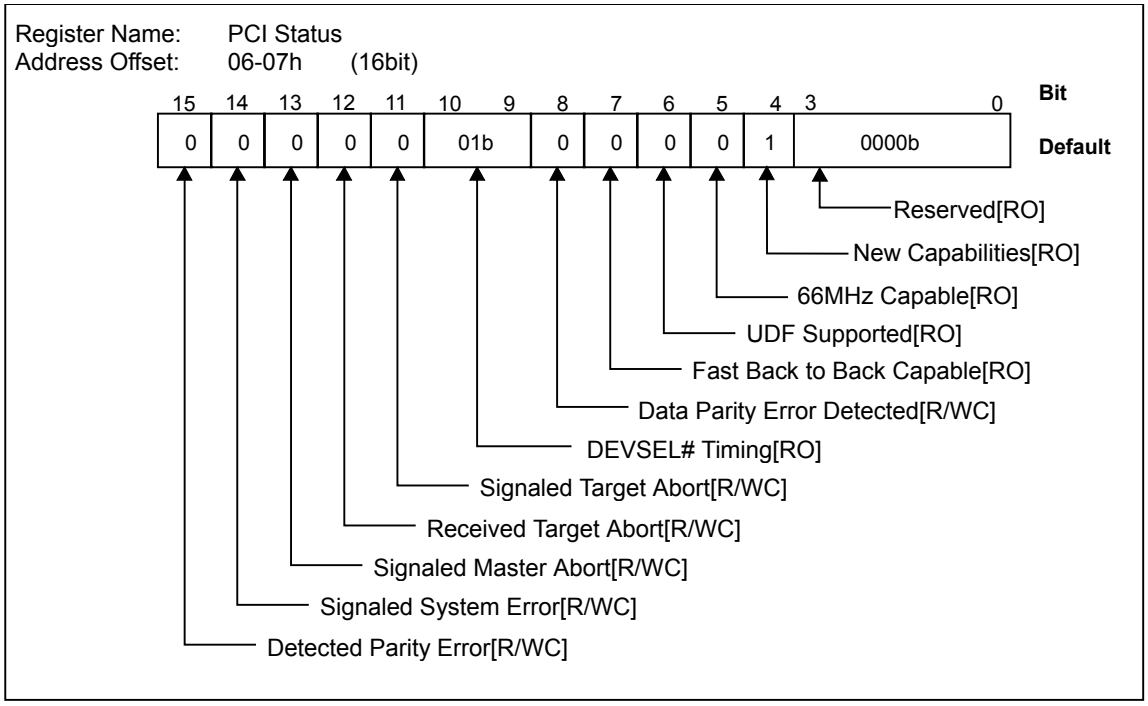


Bit	Field Name	Description
15-10	Reserved	These bits are reserved for future use by PCI Local Bus specification 2.2. This field always returns zero when read.
9	Fast Back to Back Enable	This bit controls whether or not the PCI master does fast back-to-back transactions. But, this function is not implemented in the R5C551. This bit always returns zero when read. Writing to this bit has no effect.
8	SERR# Enable	This bit controls whether or not the SERR# output buffer is enabled on the PCI interface. The default after reset is zero. 0 - disable the SERR# driver. 1 - enable the SERR# driver. This bit must be set to report address parity errors.
7	Write Cycle Control Enable	This bit controls whether or not a card does address/data stepping. But, this function is not implemented in the R5C551. This bit always returns zero when read. Writing to this bit has no effect.
6	Parity Error Response Enable	This bit controls the device's response to parity errors. When this bit is set to 1, the R5C551 takes its normal action - enable an error bit and assert PERR#, when a parity error is detected. When this bit is set to 0, the R5C551 ignores any parity errors and continue normal operation. The default after reset is zero.
5	VGA Palette Snoop Enable	This bit controls the R5C551's response to VGA palette registers. But, this function is not implemented in the R5C551's 1394 block. This bit always returns zero when read. Writing to this bit has no effect.
4	Memory Write and Invalidate Enable	This bit controls whether or not the PCI master uses the Memory Write and Invalidate command. But, this function is not implemented in the R5C551. This bit always returns zero when read. Writing to this bit has no effect.
3	Special Cycle Enable	This bit controls an action on Special Cycle operations. But, this function is not implemented in the R5C551. This bit always returns zero when read. Writing to this bit has no effect.
2	Bus Master Enable	This bit controls the R5C551's ability to operate as a master on the PCI interface. Setting this bit has no effect upon the configuration command operations. When this bit is set to 0, the R5C551 ignores requests of the 1394 OHCI block. The default after reset is zero. 0 - inhibit the R5C551 to operate as a master on the PCI interface. 1 - allow the R5C551 to operate as a master on the PCI interface
1	Memory Space Enable	This bit controls the R5C551's response to memory accesses for both the memory mapped I/O ranges and the prefetchable memory ranges. The default after reset is zero. 0 - ignore all memory transactions on the PCI interface, and the R5C551 DEVSEL# logic is inhibited during the memory cycle. 1 - enable response to memory transactions on the PCI interface. And also, this bit controls accesses to the memory mapped I/O ranges that are defined in the Card Control Base Address register.
0	I/O Space Enable	This bit controls the R5C551's response to I/O accesses for transactions on the PCI interface. The 1394 block on the R5C551 do not support I/O space. This bit is read-only and returns 0b.

5.5.4 PCI Status register

Register Name:	PCI Status [1394]
Address Offset:	06h-07h(16bit)
Default:	0210h
Access:	RO, R/WC

This 16-bit register is used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A bit is reset whenever the register is written and the data in the corresponding bit location is a one. Writing a zero to this register has no effect. The bits in this register adhere to the definitions in the PCI Local Bus Specification, but only apply to the primary PCI interface.



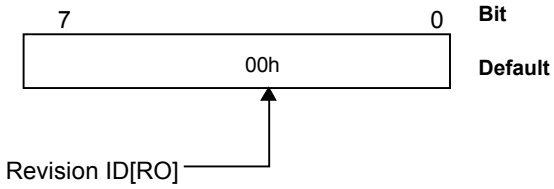
Bit	Field Name	Description
15	Detected Parity Error	This bit is set by the R5C551 whenever it detects a parity error, even if parity error handing is disabled (as controlled by bit 6 in the Command register). Writing a one to this bit clears the state.
14	Signaled System Error	This bit is set whenever the R5C551 asserts SERR#. Writing a one to this bit clears the state.
13	Signaled Master Abort	This bit is set by the R5C551 as a master device whenever its transaction is terminated with Master-abort. Writing a one to this bit clears the state.
12	Received Target Abort	This bit is set by the R5C551 as a master device whenever its transaction is terminated with Target-abort. Writing a one to this bit clears the state.
11	Signaled Target Abort	This bit is set by the R5C551 as a target device whenever its transaction is terminated with Target-abort. Writing a one to this bit clears the state.
10-9	DEVSEL# Timing	These bits encode the timing of DEVSEL#. These are encoded as 01b for medium speed. These bits are read-only. Writing to these bits has no effect.
8	Data Parity Error Detected	This bit is set when three conditions are met: 1) the bus agent asserted PERR# itself or observed PERR# asserted. 2) the agent setting the bit acted as the bus master for the operation in which the error occurred. 3) the Parity Error Response bit (Command register) is set. Writing a one to this bit has no effect.
7	Fast Back to Back Capable	This read-only bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. The R5C551 returns zero when read, because it is not capable of accepting fast back-to-back transactions. Writing to this bit had no effect.
6	UDF Supported	This read-only bit indicates whether or not the PCI device supports the UDF function. The R5C551 doesn't support the UDF function, and therefore returns a zero when read. Writing to this bit has no effect.
5	66MHz Capable	This read-only bit indicates whether or not the PCI device is capable of running at 66MHz. The R5C551 is capable of running only at 33MHz, and therefore returns a zero when read. Writing to this bit has no effect.
4	New Capabilities	This bit indicates whether PCI device implements a list of new capabilities such as PCI Power Management. The R5C551 implements it, and therefore returns a one when read. The register at 14h provides an offset into the configuration space pointing to the location of Power Management Register Block.
3-0	Reserved	These read-only bits are reserved for future use by PCI Local Bus specification 2.1. Return a zero when read. Writing to these bits has no effect.

5.5.5 Revision ID register

Register Name: Revision ID [1394]
Address Offset: 08h(8bit)
Default: 00h
Access: RO

This is a unique 8-bit value that is asserted to the device revision information. It is used with the Vendor ID and the Device ID in order to identify each PCI device. Writing to this register has no effect.

Register Name: Revision ID
Address Offset: 08h (8bit)



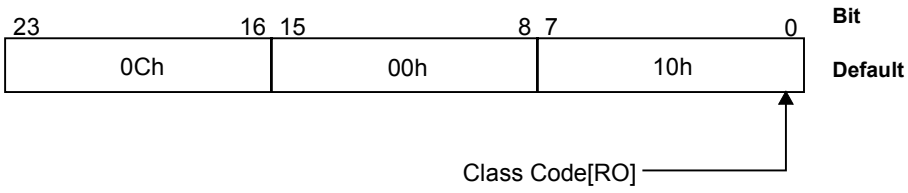
Bit	Field Name	Description
7-0	Revision ID	This read-only field is the revision identification number assigned to the R5C551 by RICOH. This field always returns 00h when read.

5.5.6 Class Code register

Register Name: Class Code [1394]
Address Offset: 09h-0Bh(24bit)
Default: 0C0010h
Access: RO

The Class Code register is read-only and is used to identify the generic function of the device. The bits in this register adhere to the definitions in the PCI Local Bus Specification. This register is broken into three byte-size fields: a base class code, a sub-class code and a programming interface. Writing to this register has no effect.

Register Name: Class Code
Address Offset: 09-0Bh (24bit)



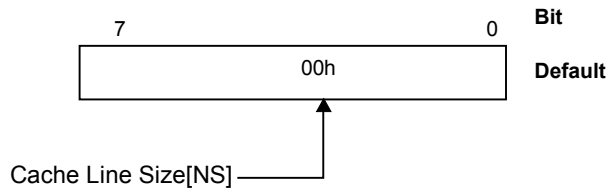
Bit	Field Name	Description
23-0	Class Code	This register is a read-only register and is used to identify the device. This register is broken into three byte-size fields. The upper byte (at offset 0Bh) is a base class code. The middle byte (at offset 0Ah) is a sub-class coded. The lower byte (at offset 09h) identifies a specific register-level programming interface. The R5C551 returns 0C0010h when this register is indicated as an IEEE1394 OHCI Serial Bus Controller device: a base class of 0Ch (bridge device), a sub-class code of 00h (PCI to CardBus) and a programming interface of 10h. Writing to this register has no effect.

5.5.7 Cache Line Size register

Register Name:	Cache Line Size [1394]
Address Offset:	0Ch(8bit)
Default:	00h
Access:	NS

The Cache Line register specifies the system cache line size in units of 32-bit words. The R5C551 doesn't participate in the caching protocol, and therefore returns zero when read. Writing to this register has no effect.

Register Name: Cache Line Size
Address Offset: 0Ch (8bit)



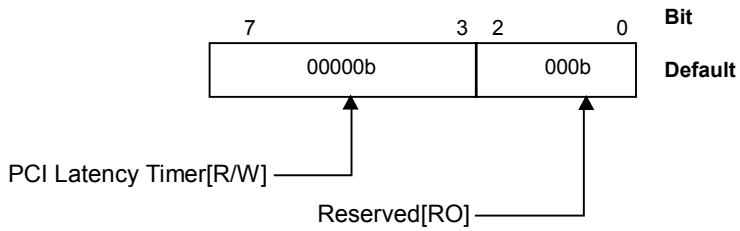
Bit	Field Name	Description
7-0	Cache Line Size	The R5C551 doesn't participate in the caching protocol. This register is read-only. Returns zero when read. Writing to this register has no effect.

5.5.8 PCI Latency Timer register

Register Name: PCI Latency Timer [1394]
Address Offset: 0Dh(8bit)
Default: 00h
Access: R/W

The PCI Latency Timer specifies, in units of PCI bus clocks, the value of the Latency Timer for the PCI bus master. This register adheres to the PCI Local Bus Specification but applies only to the primary interface. The bottom three bits in this register are read-only and hardwired to 000b, resulting in a timer granularity of eight clocks.

Register Name: PCI Latency Timer
Address Offset: 0Dh (8bit)



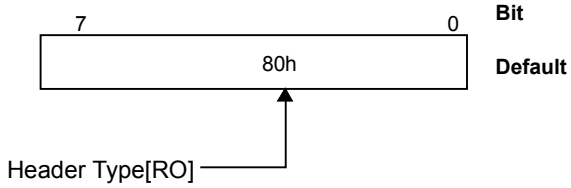
Bit	Field Name	Description
7-3	PCI Latency Timer	This register specifies, in units of PCI bus clocks, the value of the Latency Timer for the PCI bus master.
2-0	Reserved	The bottom three bits in this register are read-only and hardwired to 000b, resulting in a timer granularity of eight clocks. Writing to this field has no effect.

5.5.9 Header Type register

Register Name: Header Type [1394]
Address Offset: 0Eh(8bit)
Default: 80h
Access: RO

The Header Type register identifies the layout of bytes 10h through 3Fh in configuration space and whether or not the device contains multiple function. The R5C551 is the multi-function PCI device, and therefore returns 80h when read. Writing to this register has no effect.

Register Name: Header Type
Address Offset: 0Eh (8bit)



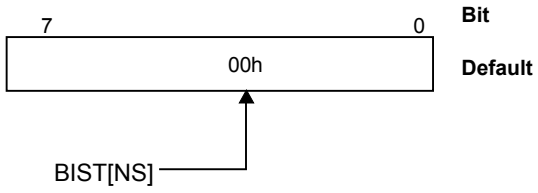
Bit	Field Name	Description
7-0	Header Type	This register identifies the layout of bytes 10h through 3Fh in configuration space and also whether or not the device contains multiple functions. Return 80h when read. Writing to this register has no effect.

5.5.10 BIST register

Register Name: BIST [1394]
Address Offset: 0Fh(8bit)
Default: 00h
Access: NS

The BIST register is used for control and status of BIST (Built In Self Test). The bits in this register adhere to the definitions in the PCI Local Bus Specification. The R5C551 does not implement BIST, and therefore returns zero when read.

Register Name: BIST
Address Offset: 0Fh (8bit)

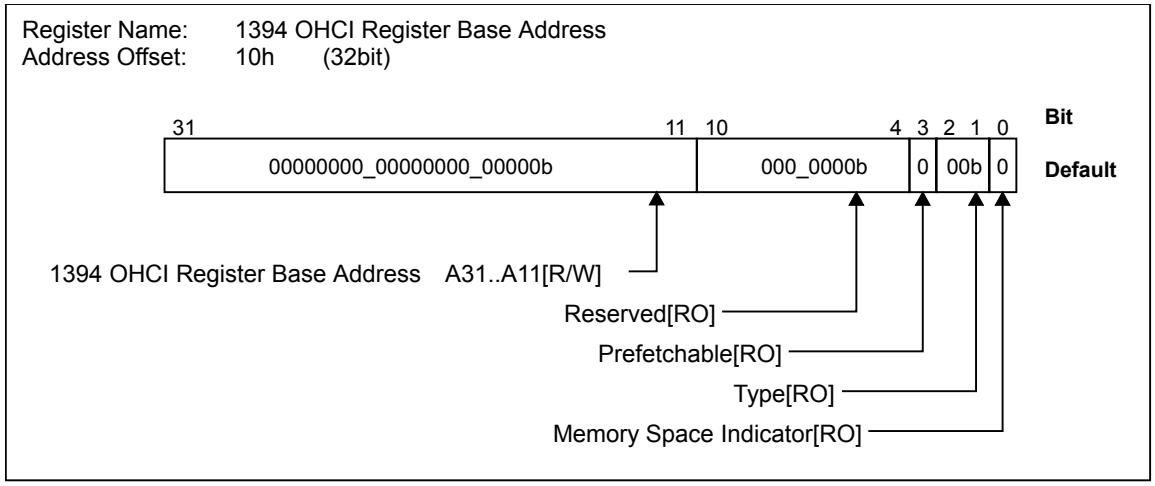


Bit	Field Name	Description
7-0	BIST	The R5C551 doesn't support this register. This read-only register always returns zero when read. Writing to this register has no effect.

5.5.11 1394 OHCI Register Base Address register

Register Name: 1394 OHCI Register Base Address [1394]
Address Offset: 10h(32bit)
Default: 0000_0000h
Access: R/W

The 1394 OHCI Register Base Address register points to the memory mapped I/O space that contains Status and Control registers for 1394 OHCI. The upper bits [31:11] are read/write and the lower bits [10:0] are hardwired to zero. This indicates to Configuration software that the R5C551 must take 2K bytes of non-prefetchable memory space.



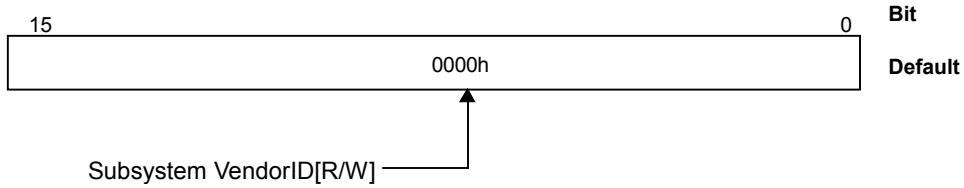
Bit	Field Name	Description
31-11	Card Control Register Base Address A31..A11	These bits indicate the memory mapped I/O space that contains status and control registers for 1394 OHCI. Bits [31:11] are read/write.
10-4	Reserved	These bits are read-only and hardwired to zero. Writing to this field has no effect.
3	Prefetchable	This bit is set to one when the data is prefetchable and reset to a zero otherwise. This filed is hardwired to zero in the R5C551. Writing to this bit has no effect.
2-1	Type	These bits have encoded meanings as shown below for Memory Base Address registers. 00 : locate anywhere in 32-bit address space 01 : locate below 1M 10 : locate anywhere in 64-bit address space 11 : reserved This field is read-only and hardwired to zero in the R5C551. Writing to this field has no effect.
0	Memory Space Indicator	This bit indicates the Base Address register maps into either a memory space or an I/O space. This bit returns zero when the register maps into a memory space and one when the register maps into an I/O space. This bit is read-only and hardwired to zero in the R5C551. Writing to this bit has no effect.

5.5.12 Subsystem Vendor ID register

Register Name:	Subsystem Vendor ID [1394]
Address offset:	2Ch-2Dh(16bit)
Default:	0000h
Access:	R/W

The R5C551 supports Subsystem Vendor ID register in order to correspond to the PC 98/99/2001 Design requirements. Setting Subsystem ID Write Enable bit (Bit4 in the Misc Control 6 register: 1394) enables the system to write into this register. And also, this register is reflected the written value of ACh (WritableSubsystem Vendor ID register) independent of Write Enable bit. On use of the Serial ROM (SPKROUT is pull-down by an external resistor), Data is read from the Serial ROM. This register is initialized by only GBRST#.

Register Name: Subsystem Vendor ID
Address Offset: 2Ch-2Dh (16bit)



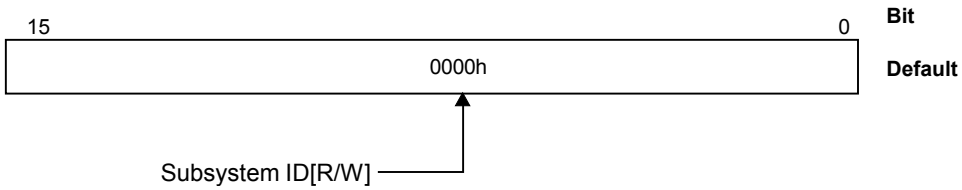
Bit	Field Name	Description
15-0	Subsystem Vendor ID	Setting Subsystem ID Write Enable bit (Bit4 in the Misc Control 6 register) enables the system to write into this register. And also, this register is reflected the written value of ACh (Writable Subsystem Vendor ID register) independent of Write Enable bit. The default after reset is zeros.

5.5.13 Subsystem ID register

Register Name: Subsystem ID [1394]
Address Offset: 2Eh-2Fh(16bit)
Default: 0000h
Access: R/W

The R5C551 supports Subsystem ID register in order to correspond to the PC 98/99/2001 Design requirements. Setting Subsystem ID Write Enable bit (Bit4 in the Misc Control 6 register) enabled to write into this register from the system. And also, this register is reflected the written value of AEh (Writable Subsystem ID register) independent of Write Enable bit. On use of the Serial ROM (SPKROUT is pull-down by an external resistor), Data is read from the Serial ROM. This register is initialized by only GBRST#.

Register Name: Subsystem ID
Address Offset: 2E-2Fh (16bit)



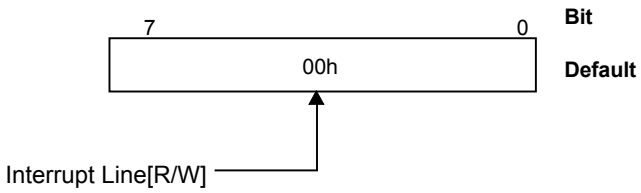
Bit	Field Name	Description
15-0	Subsystem ID	Setting Subsystem ID Write Enable bit (Bit4 in the Misc Control 6 register) enabled to write into this register from the system. And also, this register is reflected the written value of AEh (Writable Subsystem ID register) independent of Write Enable bit. The default after reset is zeros.

5.5.14 Interrupt Line register

Register Name:	Interrupt Line [1394]
Address Offset:	3Ch(8bit)
Default:	00h
Access:	R/W

The Interrupt Line register is read/write register used to communicate interrupt line routing information. This register must be initialized by BIOS software on the system configuration, so a default state is no specified. The value in this register indicates which input of the system interrupt controller the interrupt pin in the R5C551 is connected to. The default after reset is 00h.

Register Name: Interrupt Line
Address Offset: 3Ch (8bit)



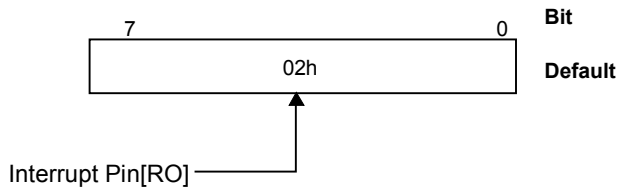
Bit	Field Name	Description
7-0	Interrupt Line	The value in this register indicates which input of the system interrupt controller the interrupt pin in the R5C551 is connected to. The default after reset is 00h.

5.5.15 Interrupt Pin register

Register Name:	Interrupt Pin [1394]
Address Offset:	3Dh(8bit)
Default:	02h
Access:	RO

The Interrupt Pin register is read-only register that adheres to the definition in the PCI Local Bus Specification. This register indicates which interrupt pin the R5C551 use. The default is 02h, as INTB# is assigned to 1394 function #1. The value of this register is changed by INT Select bit in the Misc Control 6 register.

Register Name: Interrupt Pin
Address Offset: 3Dh (8bit)

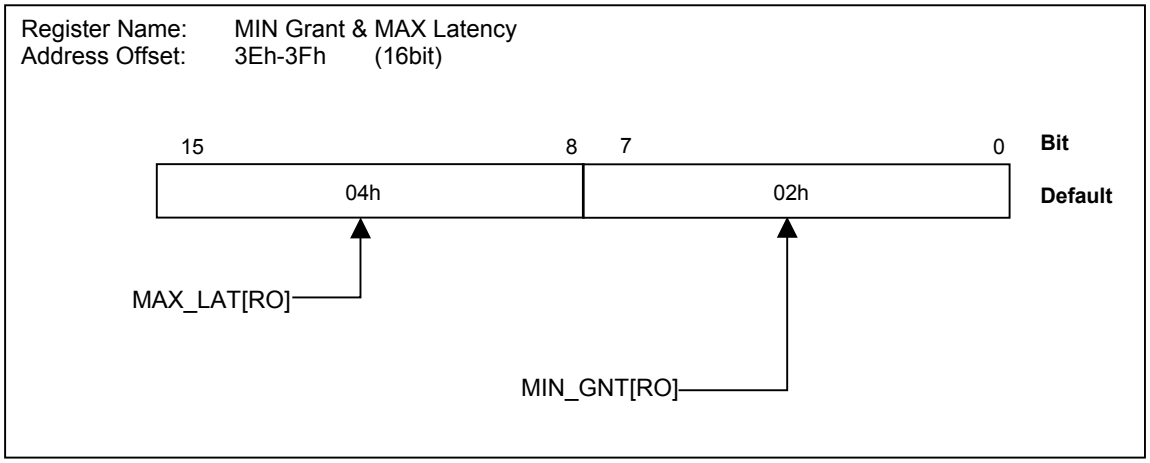


Bit	Field Name	Description
7-0	Interrupt Pin	This field is read-only and returns 02h for 1394 function #1.

5.5.16 MIN_Grant & MAX_Latency register

Register Name:	MIN_Grant & MAX_Latency [1394]
Address offset:	3Eh-3Fh (16 bit)
Default:	0402h
Access:	RO

This register is used to specify the desired settings for Latency timer values. Setting of Write Enable bit enables to set this register as Subsystem ID. And also, the values of Writable MIN_GNT & MAX_LAT register reflect on this register independent of Write Enable bit. On use of the Serial ROM (SPKROUT is pull-down by an external resistor), Data is read from the Serial ROM and written to the lower 4-bit.



Bit	Field Name	Description
15-8	MAX_LAT	MAX Latency: This field is indicated how often the R5C551 needs to gain access to the PCI bus. The upper 4bit of this field is fixed to “4’b0000” and the lower 4bit of this field load to the Serial ROM data (“MAXLAT [3:0])*.
7-0	MIN_GNT	MIN Grant: This field is indicated how long of a burst period the R5C551’ needs. The upper 4bit of this field is fixed to “4’b0000” and the lower 4bit of this field load to the Serial ROM data (“MINGRN [3:0])*.

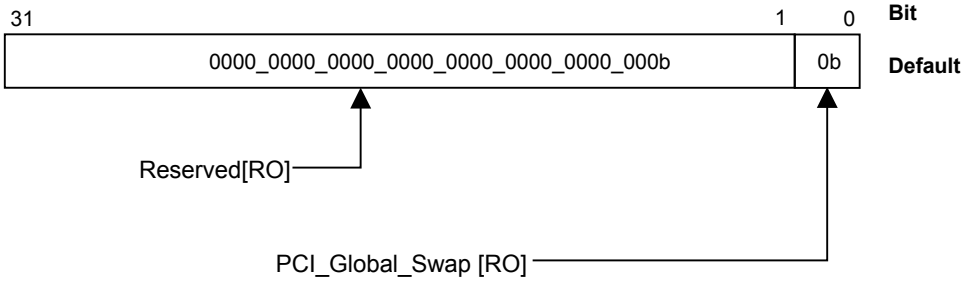
*Cf. 4.17.3 Format

5.5.17 PCI OHCI Control register

Register Name: PCI OHCI Control [1394]
Address offset: 40h-43h (32 bit)
Default: 00000000h
Access: RO

This register has a control bit for 1394 OHCI. But, the R5C551 does not support the control bits. Returns zero when read.

Register Name: PCI OHCI Control
Address Offset: 40h-43h (32bit)

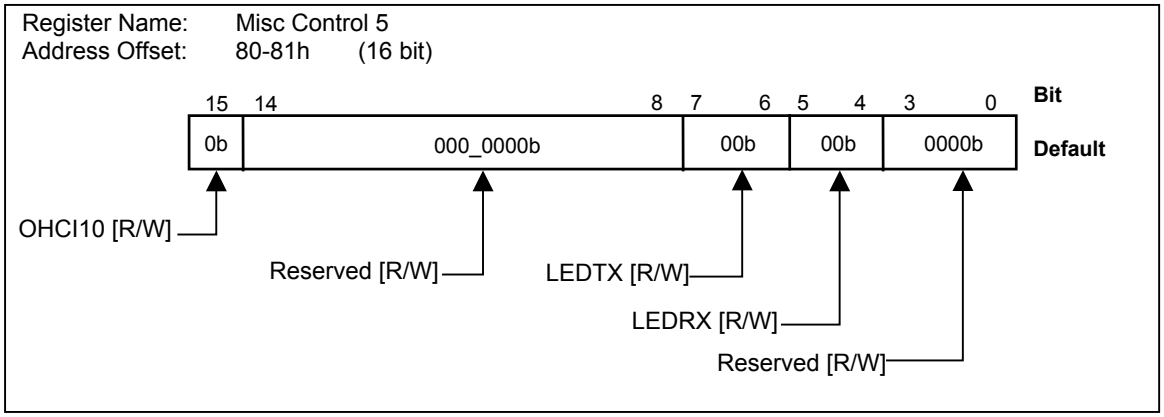


Bit	Field Name	Description
31-1	Reserved	This field is read-only. Returns zeros when read. Writing to this field has no effect.
0	PCI_Global_Swap	PCI Global Swap Bit: This bit is control bit for 1394 OHCI. The R5C551 does not support this bit. Returns zero when read.

5.5.18 Misc Control 5 register

Register Name: Misc Control 5 [1394]
Address offset: 80h-81h (16bit)
Default: 00h
Access: R/W

This register indicates each kinds of control for the R5C551. This register is initialized by only GBRST#.



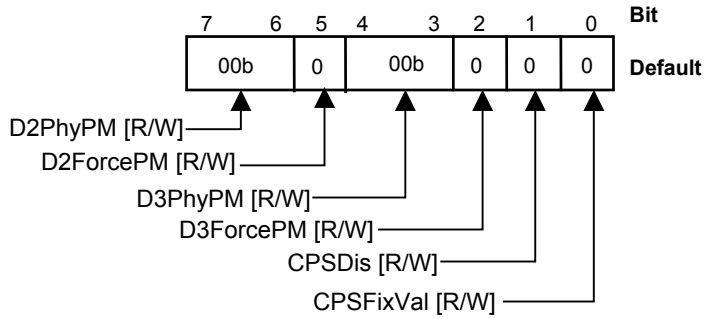
Bit	Field Name	Description
15	OHCI10	When this bit is set to one, the OHCI-Link block operates in compliance with the OHCI1.0. When this bit is set to zero, it operates in compliance with the OHCI1.1. The default is zero. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
14-8	Reserved	This field is reserved for R5C551, and is read/write. This field must be set to 0000b when write. The default after reset is zeros.
7-6	LEDTX	This field indicates the trigger's conditions for LED, when ISA_IRQn correspond to LED1394 output by the Misc Control 4 register (On Card). 0 0 the transmit packet addressed from 1394's node except for the cycle start packet. 0 1 the transmit packet addressed from all of 1394's nodes. 1 0 Reserved 1 1 8KHz trigger signal of the internal cycle timer Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
5-4	LEDRX	This field indicates the trigger's conditions for LED as above. 0 0 the receive packet addressed to 1394's node except for the cycle start packet. 0 1 the receive packet addressed to all of 1394's nodes. 1 0 Reserved 1 1 Reserved Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
3-0	Reserved	This field is reserved for R5C551, and is read/write. This field must be set to 0000b when write. The default after reset is zeros.

5.5.19 PHY Power Management register

Register Name: Phy Power Management [1394]
Address offset: 98h (8bit)
Default: 00h
Access: R/W

This register is used to set the Power Management functions of the R5C551's PHY. This register is initialized by only GBRST#.

Register Name: Phy Power Management
Address Offset: 98h (8 bit)



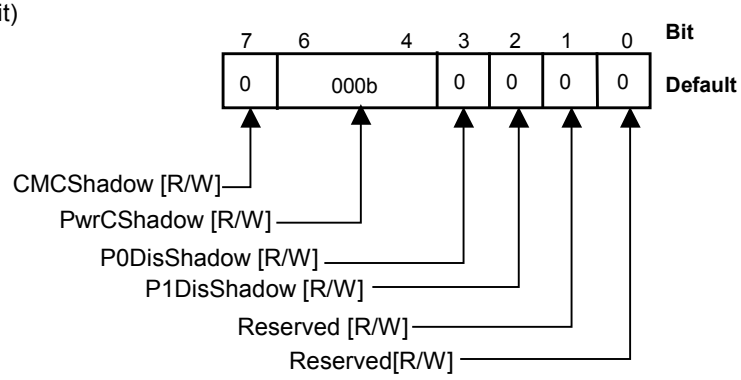
Bit	Field Name	Description
7-6	D2PhyPM	This field indicates the PHY Power Management mode on D2 state. 00b: Power Management Disable 01b: Doze 10b: Sleep Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
5	D2ForcePM	Setting this bit to one enables to force setting of the PHY Power Management mode that is selected by D2PhyPM without regard to Port's state when the power state is on D2 state. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
4-3	D3PhyPM	This field indicates the PHY Power Management mode on D0_Uninitiaized/D3 state. 00b: Power Management Disable 01b: Doze 10b: Sleep Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
2	D3ForcePM	Setting this bit to one enables to force setting of the PHY Power Management mode that is selected by D3PhyPM without regard to Port's state when the power state is on D0_uninitialized/D3 state. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
1	CPSDis	When this bit is set to one, the CPS detect circuit is disabled and a value of CPSFixVal is reflected the PS field of the PHY register. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
0	CPSFixVal	When the CPSDis is set to one, a value of this bit is reflected on the PS field of the PHY register. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.

5.5.20 PHY Shadow register

Register Name: Phy Shadow [1394]
Address offset: 99h (8bit)
Default: 00h
Access: R/W

This register enables to have read/write access to parts of the PHY register (Contender bit, Pwr_class bit and Disabled bit) directly. Moreover, each initial values of Contender bit, Pwr_class bit and Disabled bit can be set by serial ROM because this register can be initialized by serial ROM. This register is initialized by only GBRST#.

Register Name: Phy Shadow
Address Offset: 99h (8 bit)



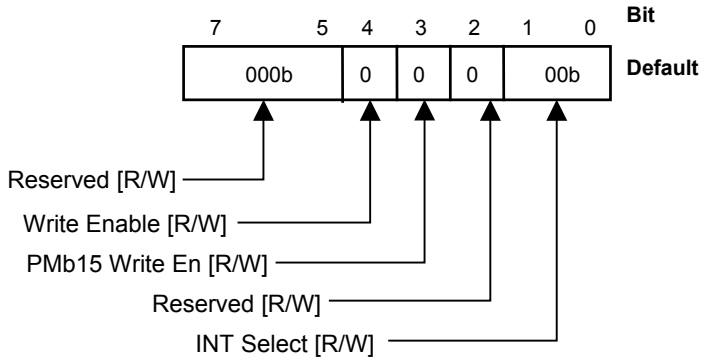
Bit	Field Name	Description
7	CMCShadow	This bit is the shadow register for the Contender bit of the PHY register. The default after reset is zero. The written value to this bit is reflected on the Contender bit of the PHY register, and the present value of this bit is returned on read. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
6-4	PwrCShadow	This field is the shadow register for the Pwr_class field of the PHY register. The written value to this field is reflected on the Pwr_class field of the PHY register, and the present value of this field is returned on read. PwrCShadow [2:0] = Pwr_class [0:2] Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
3	P0DisShadow	This bit is the shadow register for the Disabled bit of the PHY register Port 0. The written value to this bit is reflected on the Disabled bit of the PHY register Port 0, and the present value of this bit is returned on read. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
2	P1DisShadow	This bit is the shadow register for Disabled bit of the PHY register Port 1. The written value to this bit is reflected on the Disabled bit of the PHY register Port1, and the present value of this bit is returned on read. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
1	Reserved	This bit is reserved for R5C551, and is read/write. The default after reset is zero.
0	Reserved	This bit is reserved for R5C551, and is read/write. The default after reset is zero.

5.5.21 Misc Control 6 register

Register Name:	Misc Control 6 [1394]
Address offset:	9Ch (8bit)
Default:	00h
Access:	R/W

The Misc Control 6 register indicates each kinds of control for the R5C551. This register is initialized by only GBRST#.

Register Name: Misc Control 6
Address Offset: 9Ch (8 bit)



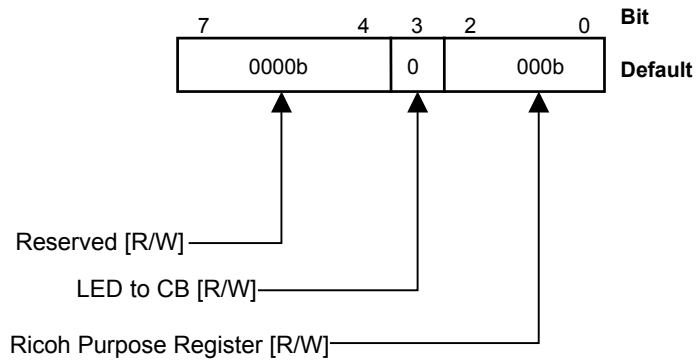
Bit	Field Name	Description
7-5	Reserved	This field is reserved for future use, and read/write. Writing to this field has no effect. The default after reset is zero.
4	Write Enable	When this bit is set to one, Subsystem Vendor ID, Subsystem ID and MIN_GNT&MAX_LAT registers are enabled to write. The default after reset is zero. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
3	PMb15 Write En	When this bit is set to one, bit15 in the Power Management capabilities register (1394) is enabled to write. The default after reset is zero. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
2	Reserved	This bit is reserved for future use, and read/write. Writing to this bit has no effect. The default after reset is zero.
1-0	INT Select	This field is used to select interrupt output pins for Card and 1394. The combinations are as follows. The default is 00b. SLOT 1394 0 0 INTA# INTB# (default) 0 1 INTA# INTB# 1 0 INTA# INTA# 1 1 INTA# INTA# Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.

5.5.22 Misc Control 7 register

Register Name: Misc Control 7 [1394]
Address offset: 9Eh (8bit)
Default: 00h
Access: R/W

The Misc Control 6 register indicates each kinds of control for the R5C551. This register is initialized by only GBRST#.

Register Name: Misc Control 7
Address Offset: 9Eh (8 bit)

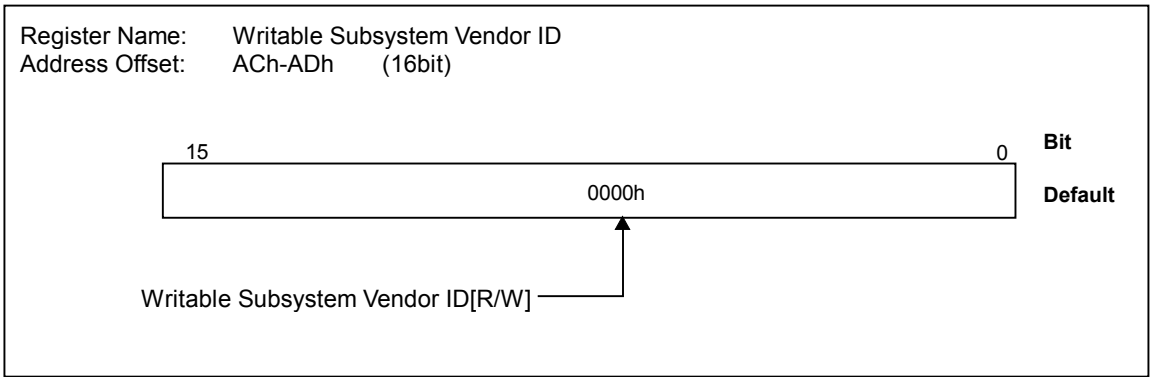


Bit	Field Name	Description
7-4	Reserved	This field is reserved for future use, and read/write. Writing to this field has no effect. The default after reset is zero.
3	LED to CB	When this bit is set to one, the LED signal of 1394 can be monitored on LED# of PC Card. Using the serial ROM enables to change the default value of this bit. Details see the serial ROM in Chapter 4.
2-0	Ricoh Purpose Register	This field is reserved for future use, and read/write. Do not write any value excepting "0" into this field. The default after reset is zero.

5.5.23 Writable Subsystem Vendor ID register

Register Name: Writable Subsystem Vendor ID [1394]
Address offset: ACh-ADh (16bit)
Default: 0000h
Access: R/W

Writable Subsystem Vendor ID register operates as same as 2Ch(Subsystem Vendor ID register). The value written in this register is enabled to read through 2Ch as Subsystem Vendor ID. This register is initialized by only GBRST#.



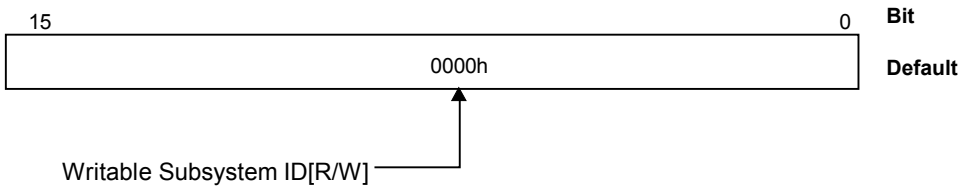
Bit	Field Name	Description
15-0	Writable Subsystem Vendor ID	Writable Subsystem Vendor ID register operates as same as 2Ch(Subsystem Vendor ID register). The value written in this register is enabled to read through 2Ch as Subsystem Vendor ID. The default after reset is 0000h.

5.5.24 Writable Subsystem ID register

Register Name: Writable Subsystem ID [Global]
Address Offset: AEh-AFh (16bit)
Default: 0000h
Access: R/W

Writable Subsystem ID register operates as same as 2Eh(Subsystem ID register). The value written in this register is enabled to read through 2Eh as Subsystem ID. This register is initialized by only GBRST#.

Register Name: Writable Subsystem ID
Address Offset: AEh-AFh (16bit)

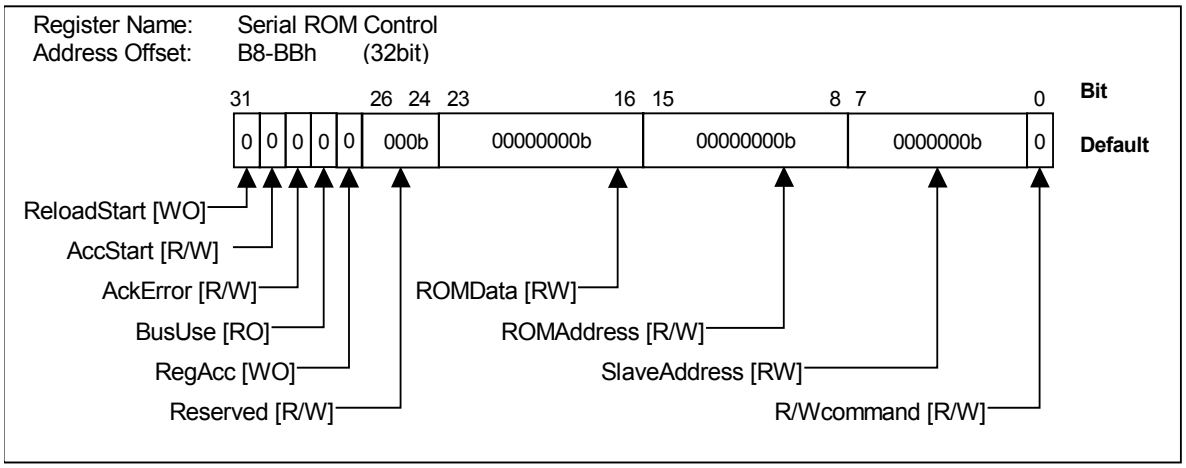


Bit	Field Name	Description
15-0	Writable Subsystem ID	Writable Subsystem ID register operates as same as 2Eh(Subsystem ID register). The value written in this register is enabled to read through 2Eh as Subsystem ID. The default after reset is 0000h.

5.5.25 Serial ROM Control register

Register Name: Serial ROM Control [1394]
Address offset: B8h-BBh (32bit)
Default: 0000h
Access: R/W

The Serial ROM Control register controls the Serial ROM.

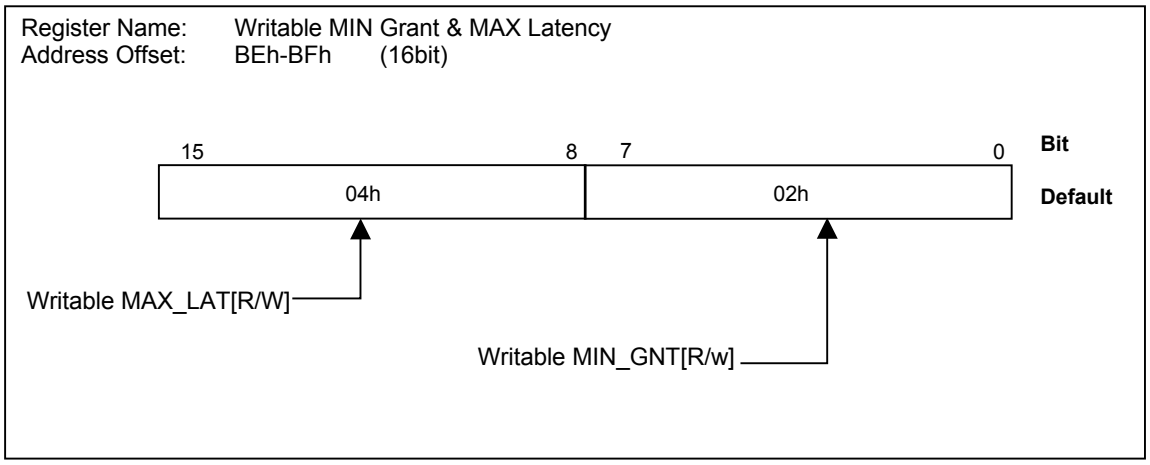


Bit	Field Name	Description
31	ReloadStart	When this bit is set, the sequencer starts to read Subsystem ID and GUID automatically. The PCI bus's accesses to Config Reg and OHCI Reg are retried during setting this bit.
30	AccStart	When this bit is set to one, Accesses to Serial ROM is started according to setting of ROM Data, ROM Address, Slave Address and R/W Command. This bit returns one during Serial ROM access, and returns zero when the access has completed. The PCI bus's access is not retried.
29	AckError	This bit indicates the judge of Ack output on write access to Serial ROM. Ack Error is detected by Ack output asserted. The R5C551 stops accesses to Serial ROM after detection of AckError. 0 : none of Ack Error 1 : Ack Error
28	BusUse	This bit indicates whether Serial ROM bus is in use or not. 0 : Serial ROM bus is not in use. 1 : Serial ROM bus is in use.
27	RegAcc	When this bit is set to one, the values of ROMData are written into the registers indicated on the ROM Address. This function means that the Serial ROM Control register can control setting of registers by Serial ROM (GUID mapped on the OHCI register etc.).
26-24	Reserved	This field is reserved for test, and is read/write. This field must be 000b when write. The default after reset is zero.
23-16	ROMData	This field is used to set the data of reading and writing from Serial ROM.
15-8	ROMAddress	This field indicates the address of Serial ROM.
7-1	SlaveAddress	This field indicates the Slave Address of Serial ROM.
0	R/WCommand	This bit indicates whether Serial ROM is on read or write. When this bit is set to one, Serial ROM is on read mode.

5.5.26 Writable MIN_GNT & MAX_LAT register

Register Name:	Writable MIN_Grant & MAX_Latency [1394]
Address offset:	BEh-BFh (16 bit)
Default:	0402h
Access:	RO

Writable MIN_GNT & MAX_LAT register operates as same as 3Eh(MIN_GNT & MAX_LAT register). The value written in this register is enabled to read through 3Eh as MIN_GNT & MAX_LAT. This register is initialized by only GBRST#.



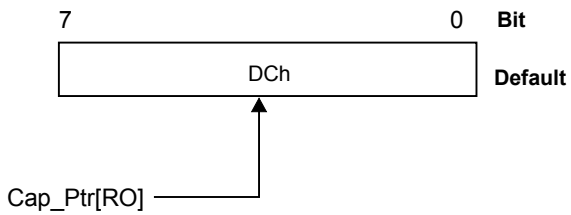
Bit	Field Name	Description
15-8	Writable MAX_LAT	Writable MIN_GNT & MAX_LAT register operates as same as 3Eh (MIN_GNT & MAX_LAT register). The value written in this register is enabled to read through 3Eh as MIN_GNT & MAX_LAT. The default after reset is 0402h.
7-0	Writable MIN_GNT	

5.5.27 Capabilities Pointer register

Register Name:	Capabilities Pointer [1394]
Address Offset:	34h (8 bit)
Default:	DCh
Access:	RO

The Capabilities Pointer register is read-only and provides an offset into the function's PCI Configuration Space for the location of the first item in the New Capabilities List. The R5C551 supports the PCI Power Management. This register is assigned a value of 0DCh for the PCI Power Management.

Register Name: Capabilities Pointer
Address Offset: 34h (8bit)



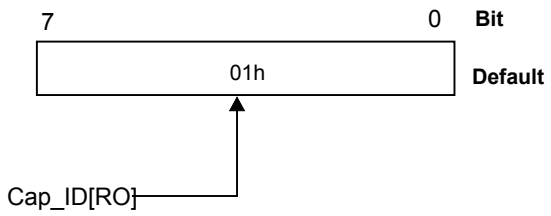
Bit	Field Name	Description
7-0	Capabilities Pointer	This field provides an offset into the function's PCI Configuration Space for the location of the first item in the New Capabilities Linked List. The R5C551 supports the PCI Power Management as a new function. This field is assigned a value of 0DCh for the PCI Power Management.

5.5.28 Capabilities Identifier register

Register Name:	Capabilities Identifier [1394]
Address Offset:	DCh (8 bit)
Default:	01h
Access:	RO

The Capabilities Identifier register is read-only and indicates only one item in the linked list is the register defined for the PCI Power Management. This register is assigned the ID of 01h.

Register Name: Capabilities Identifier register
Address Offset: DCh (8bit)



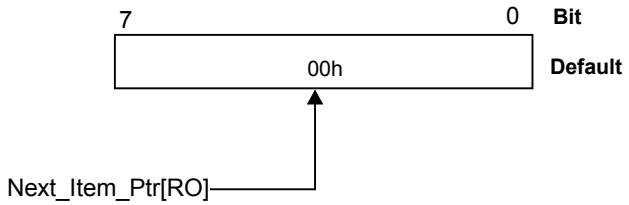
Bit	Field Name	Description
7-0	Capabilities Identifier	This field indicates the R5C551 support the PCI Power Management as a new function. This field is read-only and assigned the ID of 01h.

5.5.29 Next Item Pointer register

Register Name:	Next Item Pointer [1394]
Address Offset:	DDh (8 bit)
Default:	00h
Access:	RO

The Next Item Pointer register is read-only and indicates the location of the next item in the function's capability list. The R5C551 doesn't support items in the list except the PCI Power Management. So, this field is assigned a value of 00h.

Register Name: Next Item Pointer register
Address Offset: DDh (8bit)



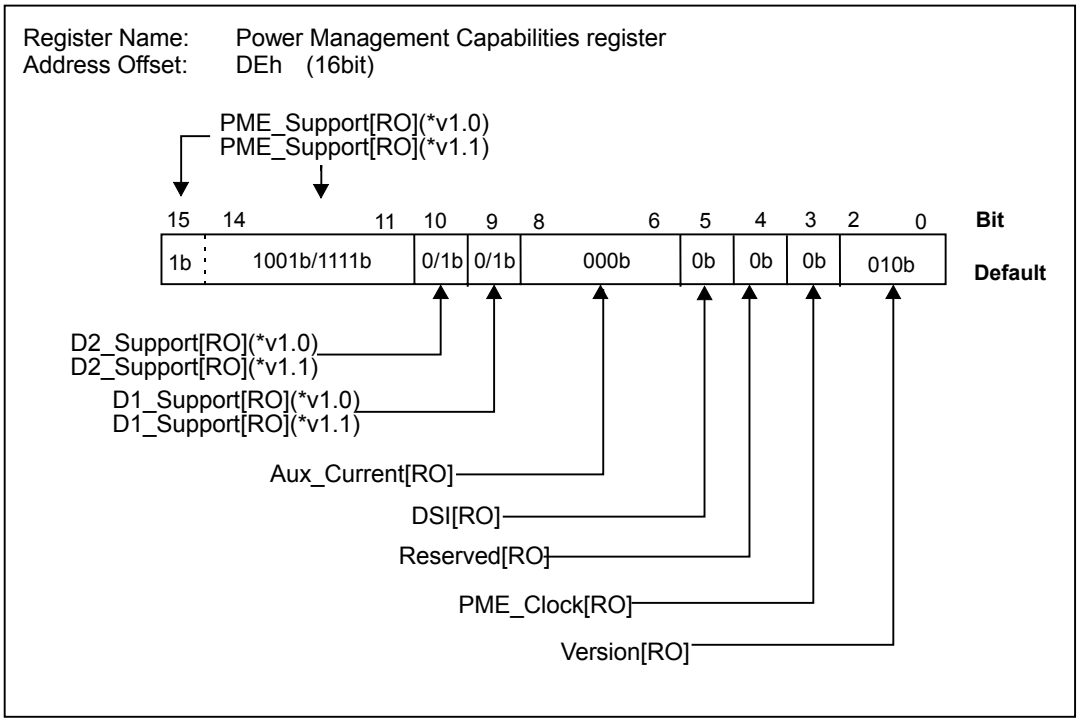
Bit	Field Name	Description
7-0	Next Item Pointer	This field indicates the location of the next item in the function's capability list. The R5C551 does not support items in the list except the PC Power Management. This field is read-only and assigned a value of 00h.

5.5.30 Power Management Capabilities register

Register Name:	Power Management Capabilities [1394]
Address Offset:	DEh (16 bit)
Default:	C802h
Access:	RO

The Power Management Capabilities register is read-only and provides information on the capabilities of the function related to the PCI Power Management. The R5C590 support the OHCI 1.0/1.1. Setting bit 7 of the Misc Control 5 register (the 1394 PCI Config.addr.81h) enables the R5C590 to switch a supporting version. If each bit of the OHCI register version1.0 or 1.1 has different function, each release is marked on the field name as follows.

*v1.0 : OHCI Release 1.0 *v1.1 : OHCI Release 1.1

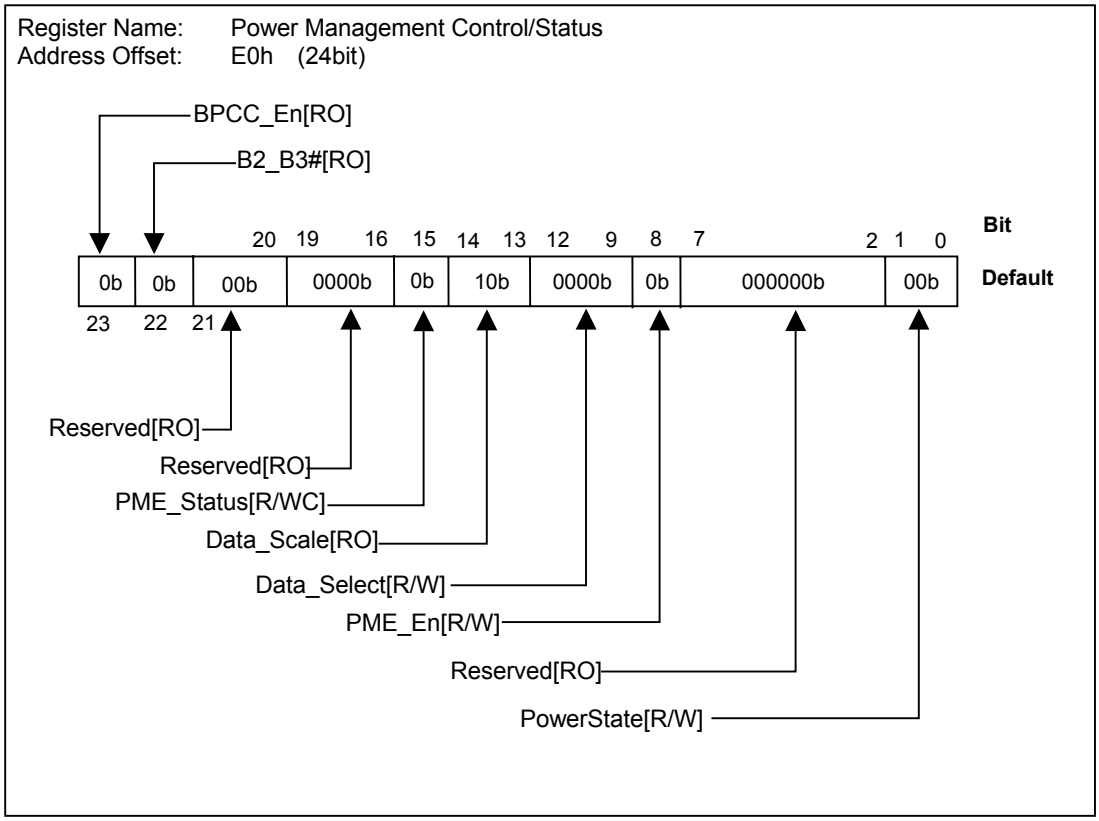


Bit	Field Name	Description
15 14-11	PME_Support	This 5-bit field indicates the power states that the device supports asserting PME#. A value of 0 for any bit indicates that the function is not capable of asserting the PME# signal from that power state. XXXX1b - PME# can be asserted from **D0** (bit 11) XXX1Xb - PME# can be asserted from **D1** (bit 12) XX1XXb - PME# can be asserted from **D2** (bit 13) X1XXXb - PME# can be asserted from **D3**hot (bit 14) 1XXXXb - PME# can be asserted from **D3cold** (bit 15) When an unmasked interrupt signal and the LinkOn signal of the PHY block are asserted, the PME# is kept at the state until Status bit (bit 15) is cleared or Enable bit (bit 8) is reset in the Power Management Control/Status register. When bit3 in Misc Control 6 register is set to one, bit15 is enabled to write.
10	D2_Support	Returns 1b on *v1.1 or 0b on *v1.0, because the R5C551 supports the D2 Power Management State.
9	D1_Support	Returns 1b on *v1.1 or 0b on *v1.0, because the R5C551 supports the D1 Power Management State.
8-6	Aux_Current	This 3-bit field indicates the 3.3Vaux auxiliary current requirements for the PCI function. Return zeros on read.
5	DSI	This Device Specific Initialization bit is set to one when a device specific device driver is required to reinitialize a device after it leaves the D3 state. Returns zero as it is not necessary to reinitialize in the R5C551.
4	Reserved	Reserved. Returns zero.
3	PME clock	When this bit is a “0” it indicates that no PCI clock is required for the function to generate PME#. This bit returns zero because the R5C551 does not need PCI clock to generate PME# when the power management event is caused by LINKON of 1394.
2-0	Version	The R5C551 has 4 bytes of general purpose Power Management registers implemented as described in PCI Bus Power Management specification Rev1.1. These bits usually return 010b.

5.5.31 Power Management Control/Status register

Register Name:	Power Management Control/Status [1394]
Address Offset:	E0h (24 bit)
Default:	004000h
Access:	R/W

The Power Management Control/Status register is used to control the current power state of the PCI function and inform the status information. The contents of this register are not affected by the internally generated reset caused by the transition from D3 to D0.



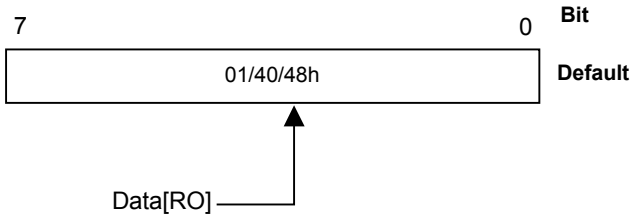
Bit	Field Name	Description
23	BPCC_En	Bus Power Clock Control Enable bit: Returns zero on the 1394.
22	B2_B3#	B2/B3 Support for D3hot: Returns zero on the 1394.
21-16	Reserved	Reserved. Return zeros when read.
15	PME_Status	This bit is set when the function normally asserts the PME# signal independent of the state of the PME_En bit (bit 8). Writing a one to this bit clears it and causes the function to stop asserting a PME# (if enabled). Writing a zero has no effect. The default after reset is zero.
14-13	Data_Scale	This 2-bits read-only field indicates the scaling factor to be used when interpreting the value of the Data register. Returns 10b as the R5C551 offers the information of power consumed in a 10mW step.
12-9	Data_Select	This 4-bits field is used to select which data is reported through the Data register and Data_Scale field. The default after reset is zero. 0000 D0 power consumed 0001 D1 power consumed 0010 D2 power consumed 0011 D3 power consumed 0100 D0 power dissipated 0101 D1 power dissipated 0110 D2 power dissipated 0111 D3 power dissipated 1xxx Reserved
8	PME_En	When this bit is set, the function is enabled to assert PME#. When this bit is cleared, assertion of PME# is disabled. The default after reset is zero.
7-2	Reserved	Reserved. Return zeros when read.
1-0	PowerState	This field is used to set the function into a new power state. The definition of the field values is: 00b - D0 01b - D1 10b - D2 11b - D3 The default after reset is zeros.

5.5.32 Data register

Register Name:	Data [1394]
Address Offset:	E3h (8 bit)
Default:	01h / 40h / 48h
Access:	RO

The Date register is read-only and provides a maximum value of the power consumed for each function from the PCI device by using with Data_Select bit fields and Data_Scale bit field.

Register Name: Data
Address Offset: E3h (8bit)



Bit	Field Name	Description
7-0	Data	This read-only bit field provides the maximum value of the power consumed by the R5C551 for each function from the PCI device. The maximum value of the power consumed is 10mW times the value of Data_Scale bit field. The R5C551 returns the following value. D0 power state : 0100 1000b (720mW) D1 power state : 0100 0000b (640mW) D2 power state : 0000 0001b (10mW) D3 power state : 0000 0001b (10mW)

6 CARDBUS (PC CARD-32) SOCKET STATUS CONTROL REGISTERS

6.1 Overview

CardBus Socket Status/Control registers manage changed events, remote wakeup events, PC Card insertion/removal, and status information about the PC Card in the socket. These registers are used for PC Card-32 as well as PC Card-16.

6.2 Register Space mapping

PC Card Control Register Base Address register points to the 4Kbyte memory mapped I/O space that contains both the PC Card-32 and PC Card-16 Status and Control registers. Socket Status/Control Registers for PC Card-32 are placed in the bottom 2KByte of the 4KByte and start at offset 000h. The registers for PC Card-16 are placed in the upper 2KByte and start at offset 800h.

6.3 Register Configuration

Each socket has CardBus Socket Status/Control register which consist of five DWORD registers. One set of registers is described in the following sections, with the address offset for each socket. Address offset 014h through 7FCh is assigned to the reserved registers. The reserved registers return 00000000h when read. Writing to the reserved registers has no effect.

Register Space Name: CardBus Socket Status / Control Register Space

31 24	23 16	15 8	7 0	Bit
Socket Event				000h
Socket Mask				004h
Socket Present State				008h
Socket Event Force				00Ch
Socket Control				010h
Reserved				014h ~ 7FCh

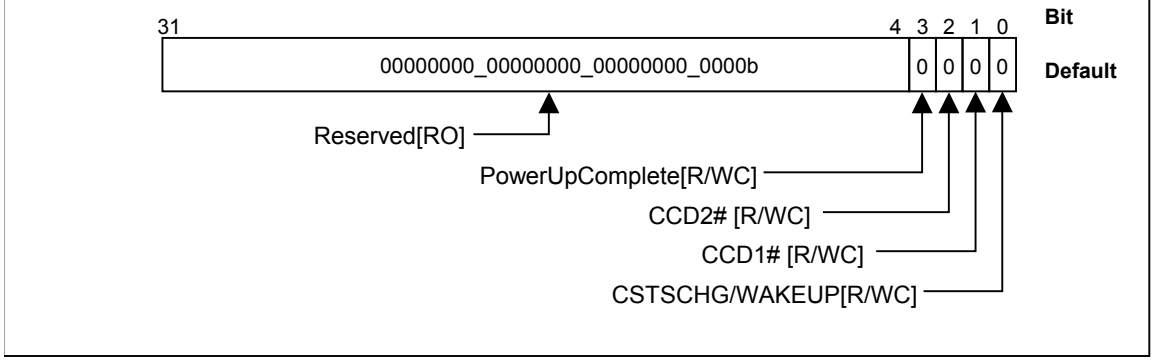
6.4 Register Description

CardBus Socket Status/Control registers manage status changed events, remote wakeup events, PC Card insertion/removal, and status information about the PC Card in the socket. These registers are used for PC Card-32 as well as PC Card-16.

6.4.1 Socket Event register

The Socket Event register indicates a change in socket status has occurred. These bits do not indicate what the change is, only that one has occurred. Software must read the Socket Present State register for current status. Writing a one to bit corresponding to each bits can clear each bits in this register. These bits can be set to a one by software through writing a one to the corresponding bit in the Socket Event Force register. All bits in this register are cleared by PCIRST#. They may be immediately set again, if when coming out of CRST# the bridge finds the status unchanged (i.e., CSTSCHG reasserted or Card Detects is still true). Software needs to clear this register before enabling interrupts. If it is not cleared, when interrupts are enabled an interrupt will be generated based on any bit set but not masked.

Register Name: Socket Event
Address Offset: 000-003h (32bit)

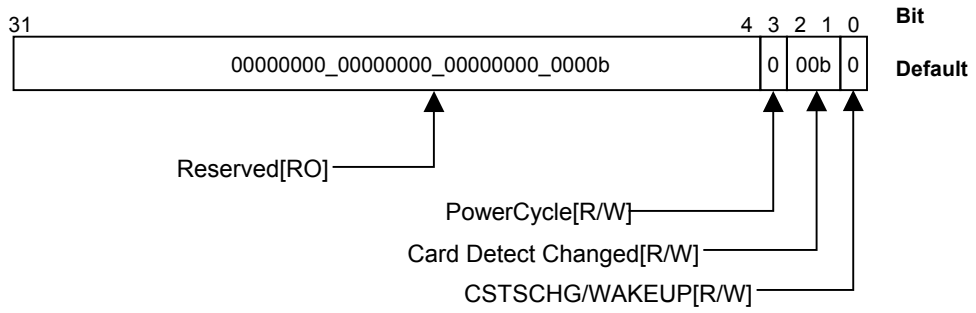


Bit	Field Name	Description
31-4	Reserved	These bits are reserved for future use. This field is read-only and returns zeros. Writing to this field has no effect.
3	PowerUpComplete	This bit is set when the R5C551 detected to complete powering up the PC Card-32 socket. The Socket Present State register should be read to determine whether or not the voltage requested was actually applied. This bit is cleared by writing a one. The default after reset is zero. This bit has no meaning when the 16-bit card is installed.
2	CCD2#	This bit is set whenever the CCD2# field in the Present State register changes state. Writing a one clears this bit. The default after reset is zero.
1	CCD1#	This bit is set whenever the CCD1# field in the Present State register changes state. Writing a one clears this bit. The default after reset is zero.
0	CSTSCHG/WAKEUP	This bit is set whenever the CSTSCHG/WAKEUP# was asserted, and indicates only the assertion event. However, this bit isn't directly reflected in a status change of the CSTSCHG/WAKEUP# in the Socket Present State register. And also, it isn't directly reflected in a status of the CSTSCHG bit from the card. This bit needs to be controlled by Software. Writing a one clears this bit. The default after reset is zero. This bit is meaningless when the 16-bit card is installed. If STSCHG# interrupt signal from the 16-bit card was occurred, this bit will be controlled by the 16-bit Card Status/Control register.

6.4.2 Socket Mask register

The Socket Mask register allows software to control the CardBus card events that generate a status change interrupt. If the Card Detect Changed bit is enabled at the time a card is removed, an interrupt is generated. After that, this bit is cleared automatically. This is to prevent spurious interrupts while cards are removed. If it is desired to have the bridge generate an interrupt at the time a new card is inserted, it is necessary that this bit is set again by software. This register is cleared by PCIRST#. The default after reset is zero.

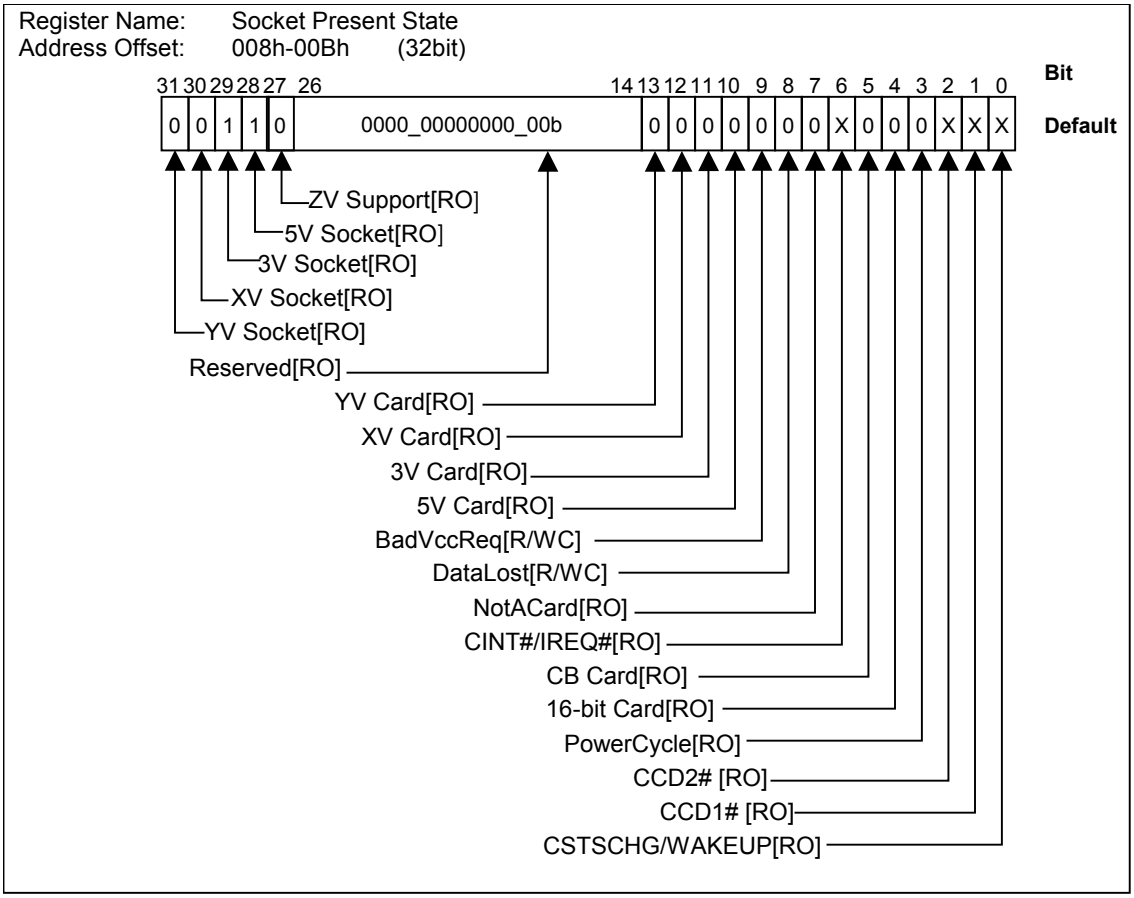
Register Name: Socket Mask
Address Offset: 004-007h (32bit)



Bit	Field Name	Description
31-4	Reserved	These bits are reserved for future use. This field is read-only and returns zeros. Writing to this field has no effect.
3	PowerCycle	This bit is masked a status changed interrupt caused by the event that indicates the end of power up process. When cleared (0), the status changed event signaling the power up process has completed is not generated, although the PowerCycle field in the Socket Event register is set. When this bit is set to one, an interrupt is generated after 256 cycles since a socket was finished powering up. The default after reset is zero.
2-1	Card Detect Changed	This field masks the CCD1# and CCD2# fields in the Socket Event register so that insertion and removal events will not cause a status changed interrupt to occur. The meaning of the bit is: 00 - Mask the CCD1# and CCD2# fields in the Socket Event register. Card insertion/removal events will not cause a status change interrupt. 01 - Undefined 10 - Undefined 11 - Unmask the CCD1# and CCD2# fields in the Socket Event register. Card insertion/removal events will cause a status change interrupt. The CCD1# and CCD2# fields in the Socket Event register are set in spite of setting of this field. The default after reset is zero.
0	CSTSCHG/WAKEUP	This bit masks a status changed interrupt of the CSTSCHG/WAKEUP#. When cleared (0), the assertion of CSTSCHG/WAKEUP# by the card is not cause a status changed interrupt to occur, although the CSTSCHG/WAKEUP field in the Socket Event register is set. This bit is set by writing a one. This bit is cleared when the socket PC card is removed, and also when the R5C551 is reset. This bit has no meaning when the 16-bit card is inserted.

6.4.3 Socket Present State register

The Socket Present State register reflects the current state of the socket. Some of the bits in this register are reflections of interface signals while others are flags set to indicate conditions associated with a status changed event. This register may be written by using the Force Event register.

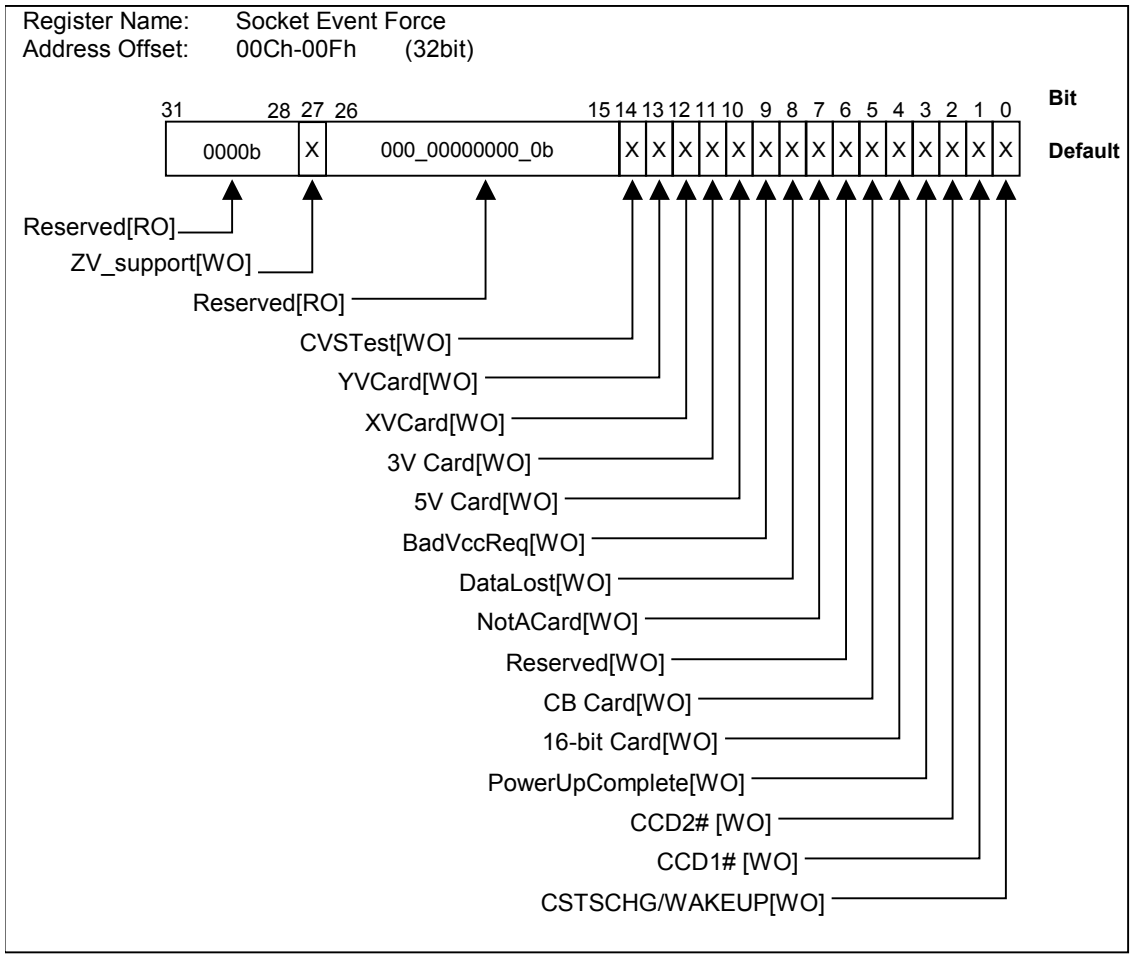


Bit	Field Name	Description
31	Yvsocket	When set (1), indicates that the socket can supply Vcc=Y.YV. When cleared (0), indicates that the socket cannot supply Vcc=Y.YV. R5C551 does not support this function. So they always return zero when read.
30	Xvsocket	When set (1), indicates that the socket can supply Vcc=X.XV. When cleared (0), indicates that the socket cannot supply Vcc=X.XV. R5C551 does not support this function. So they always return zero when read.
29	3Vsocket	When set (1), indicates that the socket can supply Vcc=3.3V. When cleared (0), indicates that the socket cannot supply Vcc=3.3V. R5C551 supports this function. So they always return one when read.
28	5Vsocket	When set (1), indicates that the socket can supply Vcc=5.0V. When cleared (0), indicates that the socket cannot supply Vcc=5.0V. R5C551 supports this function. So they always return one when read.
27	ZV_Support	This bit indicates whether the R5C551 supports the ZV port or not, and is read-only. The default after reset returns zero (= not support). Setting bit 27 of the Socket Event Force register to one enables to set this bit to one (= support).

Bit	Field Name	Description
26-14	Reserved	This field is reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.
13	YVCard	The R5C551 does not support this field. Return zero when read.
12	XVCard	The R5C551 does not support this field. Return zero when read.
11	3VCard	Writing to this field cause the 3V Card field in the Present State register to be written. Setting this field disable the socket's ability to power up Vcc until the CVStest field is set. To change the voltage of a card, after forcing this bit, the bridge must either receive a PCIRST# or retest the card's supported voltages. The latter can be accomplished by forcing the CVStest bit. This is necessary to prevent software from applying an incorrect voltage to the R5C551.
10	5VCard	Writing to this field cause the 5V Card field in the Present State register to be written. Setting this field disable the socket's ability to power up Vcc until the CVStest field is set in the Force register. To change the voltage of a card, after forcing this bit, the bridge must either receive a PCIRST# or retest the card's supported voltages. The latter can be accomplished by forcing the CVStest bit. This is necessary to prevent software from applying an incorrect voltage to the R5C551.
9	BadVccReq	When set (1), indicates that software attempted to apply a Vcc voltage to a socket that was outside the range detected using the CVS [2:1] and CCD [2:1]# pins.
8	DataLost	When set (1), indicates that a PC card removal event may have caused data to be lost either because a transaction was not completed properly or data was left in the R5C551's buffers. It must be cleared by Card Services when the removal event status changed interrupt is serviced. Writing back a one to this field clears it.
7	NotACard	When set (1), indicates that the type of card inserted could not be determined, the R5C551 does not supply the power to the card. This value does not have to be updated until a recognizable card (e.g. 16-bit PC Card or CardBus PC Card) is inserted.
6	CINT#/IREQ#	When set (1), indicates that the inserted card is driving its interrupt pin true. This bit is not a registered bit and its assertion/deassertion must follow the interrupt pin from the card. This bit reflects the inverted state of CINT#/IREQ# pin as these signals are low true.
5	CBcard	When set (1), indicates that the card inserted was a CardBus PC Card. This value is not updated until a non-CardBus PC Card (e.g. 16-bit PC Card or unrecognized) is inserted. When set, the R5C551 must configure the socket interface for CardBus PC Card.
4	16-bit Card	When set (1), indicates that the card inserted was a 16-bit PC Card. This value is not updated until a non-16-bit PC Card (e.g. CardBus PC Card or unrecognized card) is inserted. When set, the R5C551 configures the socket interface for 16-bit PC Card. Setting this field disables the R5C551's voltage checking hardware so extreme care must be taken when writing the Control register or the hardware could be damaged.
3	PowerCycle	When set (1), indicates that the interface is powered up, i.e. the power up process was successful. When cleared (0), indicates that the interface is powered down, i.e. the power up process was not successful. This field is updated by the R5C551 to communicate the status of each power up/power down request.
2	CCD2#	This field reflects the current state of the CCD2# pin on the interface. 1 indicates CCD2# is High (card is not present), 0 indicates CCD2# is low (card is present). Since the CCD2# pin could be shorted to either CVS1 or CVS2, the value stored here is for when the CVS [2:1] pins are held low.
1	CCD1#	This field reflects the current state of the CCD1# pin on the interface. 1 indicates CCD1# is High (card is not present), 0 indicates CCD1# is low (card is present). Since the CCD1# pin could be shorted to either CVS1 or CVS2, the value stored here is for when the CVS [2:1] pins are held low.
0	CSTSCHG/ WAKEUP	This field reflects the current state of the CSTSCHG/WAKEUP# pin on the interface. 1 indicates CSTSCHG/WAKEUP# is asserted, 0 indicates it is deasserted. This bit is meaningless when a 16-bit PC Card is installed. CSTSCHG/WAKEUP# interrupts generated by 16-bit PC Cards are controlled via registers in that interface register space.

6.4.4 Socket Event Force register

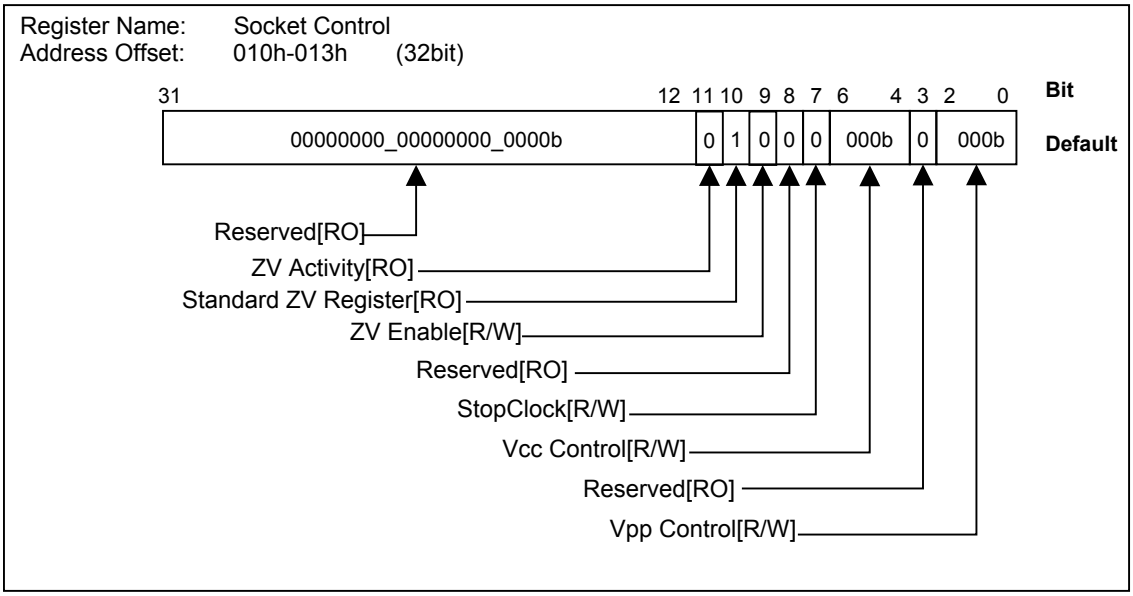
The Socket Event Force register is a phantom register. This register provides software the ability to simulate events by forcing values in the socket's Event and Present State registers. And also, this register provides software the ability to test and restore status. Writing a one to a bit in this register sets the corresponding bit in the socket's Event and Preset State registers.



Bit	Field Name	Description
31-28	Reserved	This field is reserved for future use. Writing to this field has no meaning.
27	ZV_support	Setting this bit to one enables to set the ZV Support bit of the Socket Present State register. When the socket supports the ZV port, the R5C551 must write this bit to one.
26-15	Reserved	This field is reserved for future use. Writing to this field has no meaning.
14	CVStest	When written to a 1, causes the R5C551 to interrogate the CVS [2:1] and CCD# pins and update the xVCard fields in the Present State register. This action also re-enables the socket to power up Vcc if the xVCard fields had been previously forced.
13	YVCard	The R5C551 doesn't support this function. Writing to this field has no meaning.
12	XVCard	The R5C551 doesn't support this function. Writing to this field has no meaning.
11	3VCard	Writing to this field cause the 3V Card field in the Present State register to be written. Setting this field disable the socket's ability to power up Vcc until the CVStest field is set. To change the voltage of a card, after forcing this bit, the bridge must either receive a PCIRST# or retest the card's supported voltages. The latter can be accomplished by forcing the CVStest bit. This is necessary to prevent software from applying an incorrect voltage to the R5C551.
10	5VCard	Writing to this field cause the 5V Card field in the Present State register to be written. Setting this field disable the socket's ability to power up Vcc until the CVStest field is set in the Force register. To change the voltage of a card, after forcing this bit, the bridge must either receive a PCIRST# or retest the card's supported voltages. The latter can be accomplished by forcing the CVStest bit. This is necessary to prevent software from applying an incorrect voltage to the R5C551.
9	BadVccReq	Writing to this field cause the BadVccReq field in the Present State register to be written.
8	DataLost	Writing to this field cause the DataLost field in the Present State register to be written.
7	NotACard	Writing to this field cause the NotACard field in the Present State register to be written. If a card is present in the socket (i.e. CCD1# and CCD2# are asserted), writing to this field is ignored.
6	Reserved	This field is reserved for future use. Writing to this field has no meaning.
5	CB Card	Writing to this field cause the CB Card field in the Present State register to be written. If a card is present in the socket (i.e. CCD1# and CCD2# are asserted), writing to this field is ignored.
4	16-bit Card	Writing to this field cause the 16-bit PC Card field in the Present State register to be written. If a card is present in the socket (i.e. CCD1# and CCD2# are asserted), writing to this field is ignored.
3	PowerUpComplete	Writing a 1 to this field simulates the successful completion of a power cycle event by causing the PowerCycle field in the Event register to be set. Note that the PowerCycle field in the Present State register is not affected and continues to reflect the present state of the interface power. Writing a 0 has no meaning.
2	CCD2#	Writing a 1 to this field causes the CCD2# field in the Event register to be set. Note that the CCD2# field in the Present State register is not affected and continues to reflect the present state of the CCD2# pin. Writing a 0 has no meaning.
1	CCD1#	Writing a 1 to this field causes the CCD1# field in the Event register to be set. Note that the CCD1# field in the Present State register is not affected and continues to reflect the present state of the CCD1# pin. Writing a 0 has no meaning.
0	CSTSCHG	Writing a 1 to this field simulates the assertion of the CSTSCHG pin. This results in the Event register's CSTSCHG field being set. Note that the CSTSCHG field in the Present State register is not affected and continues to reflect the present state of the CSTSCHG pin. Writing a 0 has no meaning.

6.4.5 Socket Control register

The Socket Control Register provides control of the socket's Vcc and Vpp. All bits in this register is cleared to zero and the power is removed from the socket when PCITST# is asserted. The supply voltage to the PC card is determined by the interrogation of CCD1#, CCD2#, CVS1, and CVS2 according to the card type detection mechanism described in the CardBus specification. The R5C551 do not supply a Vcc voltage that is not indicated by the VS decode.



Bit	Field Name	Description
31-12	Reserved	This field is reserved for future use. This field is read-only and returns zero when read. Writing to this field has no meaning.
11	ZV_Actibity	When the ZV port on either socket is enabled, this bit is set to one.
10	Standard ZV Register	This bit indicates whether register's set for the standard ZV port is supported. The R5C551 returns one because the R5C551 supports.
9	ZV Enable	Setting this bit to one enables the ZV port of the socket.
8	Reserved	This field is reserved for future use. This field is read-only and returns zero when read. Writing to this field has no meaning.
7	StopClock	Setting this bit to one, stops the CardBus clock complying CCLKRUN# protocol. If the card does not support this protocol, the CardBus clock will be stopped regardless of the card status. The default after reset is zero.
6-4	Vcc Control	This field is used to control the Vcc power to the PC Card via external control logic. The bridge determines the voltages that can be applied by decoding the CD and VS signals per the CardBus specification. Those bits and the voltages available in the system determine the correct Vcc options. The value written to this register must agree with the value needed to apply the correct value of Vcc. The bridge must not allow an incorrect Vcc voltage to be applied to a socket. The voltages available are shown in the Status Register. Bit 654 — VCC3EN# — VCC5EN#* 000 Requested Vcc voltage = power off — H — H 001 Reserved — H — H 010 Requested Vcc voltage = 5.0V — H — L 011 Requested Vcc voltage = 3.3V — L — H 100 Reserved — H — H 101 Reserved — H — H 110 Reserved — H — H 111 Reserved — H — H * if permitted
3	Reserved	This bit is reserved for future use. This bit is read-only and returns zero. Writing to this field has no meaning.
2-0	Vpp Control	This field is used to switch the Vpp power using external Vpp control logic. The bridge has no knowledge of a card's Vpp voltage requirement. Software must determine the needed voltage from the card's CIS. Bit 210 — VPPEN0 — VPPEN1* 000 Requested Vpp voltage = power off — L — L 001 Requested Vpp voltage = 12.0V — L — H 010 Requested Vpp voltage = 5.0V — H — L 011 Requested Vpp voltage = 3.3V — H — L 100 Reserved — L — L 101 Reserved — L — L 110 Reserved — L — L 111 Reserved — L — L * if permitted

7 16-BIT (PC CARD-16) SOCKET STATUS/CONTROL REGISTERS

7.1 Overview

The PC Card-16 Socket Status/Control Register set manages status changed events, remote wakeup events, PC Card insertion/removal, and status information about the PC Card in the socket. These registers are used only for PC Card-16.

7.2 Register Space mapping

The Socket Status/Control Register set for PC Card-16 is placed in the top 2Kbyte of the memory mapped I/O space of 4Kbyte pointed by the PC Card Control Register Base Address Register and start at offset 800h. (The bottom 2Kbyte is assigned to PC Card-32 Socket Status/Control Register set.) These registers can be also accessed through INDEX/DATA port residing I/O address 3E0/3E2, and maintain the backward compatibility with ISA-PCMCIA controllers.

7.3 Register Configuration

A socket has the PC Card-16 Socket Status/Control Register set that consist of 64 BYTE registers. One set of registers is described in the following sections, with the address offset for each socket. Address offset 845h through FFCh is assigned to reserved register. The reserved registers return 00000000h when read. Writing to the reserved registers has no effect.

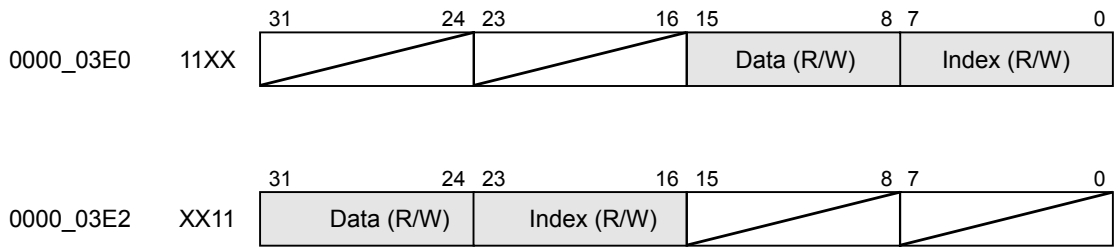
Mapping Offset	Legacy Index A	Register Name	Mnemonic	Note
800h	00h	Identification and Revision	IDREVS	
801h	01h	Interface Status	IFSTAT	
802h	02h	Power Control	PWCTRL	
803h	03h	Interrupt and General Control	IGCTRL	
804h	04h	Card Status Change	CSCHG	
805h	05h	Card Status Change Interrupt Configuration	CSCINT	
806h	06h	Address Window Enable	AWINEN	
807h	07h	I/O control	IOCTRL	
808h	08h	I/O address 0 Start Low Byte	IOSTL0	
809h	09h	I/O address 0 Start High Byte	IOSTH0	
80Ah	0Ah	I/O address 0 Stop Low Byte	IOSPL0	
80Bh	0Bh	I/O address 0 Stop High Byte	IOSPH0	
80Ch	0Ch	I/O address 1 Start Low Byte	IOSTL1	
80Dh	0Dh	I/O address 1 Start High Byte	IOSTH1	
80Eh	0Eh	I/O address 1 Stop Low Byte	IOSPL1	
80Fh	0Fh	I/O address 1 Stop High Byte	IOSPH1	
810h	10h	System Memory Address 0 Mapping Start Low Byte	SMSTL0	
811h	11h	System Memory Address 0 Mapping Start High Byte	SMSTH0	
812h	12h	System Memory Address 0 Mapping Stop Low Byte	SMSPL0	
813h	13h	System Memory Address 0 Mapping Stop High Byte	SMSPH0	
814h	14h	Card Memory Offset Address 0 Low Byte	MOFFL0	
815h	15h	Card Memory Offset Address 0 High Byte	MOFFH0	
816h	16h	Card Detect and General Control	CDGENC	
817h	17h	Reserved	RSRVD	
818h	18h	System Memory Address 1 Mapping Start Low Byte	SMSTL1	

Mapping Offset	Legacy Index A	Register Name	Mnemonic	Note
819h	19h	System Memory Address 1 Mapping Start High Byte	SMSTH1	
81Ah	1Ah	System Memory Address 1 Mapping Stop Low Byte	SMSPL1	
81Bh	1Bh	System Memory Address 1 Mapping Stop High Byte	SMSPH1	
81Ch	1Ch	Card Memory Offset Address 1 Low Byte	MOFFL1	
81Dh	1Dh	Card Memory Offset Address 1 High Byte	MOFFH1	
81Eh	1Eh	16 bit Global Control	GLCTRL	
81Fh	1Fh	ATA Control	ATCTRL	
820h	20h	System Memory Address 2 Mapping Start Low Byte	SMSTL2	
821h	21h	System Memory Address 2 Mapping Start High Byte	SMSTH2	
822h	22h	System Memory Address 2 Mapping Stop Low Byte	SMSPL2	
823h	23h	System Memory Address 2 Mapping Stop High Byte	SMSPH2	
824h	24h	Card Memory Offset Address 2 Low Byte	MOFFL2	
825h	25h	Card Memory Offset Address 2 High Byte	MOFFH2	
826h	26h	Reserved	RSRVD	
827h	27h	Reserved	RSRVD	
828h	28h	System Memory Address 3 Mapping Start Low Byte	SMSTL3	
829h	29h	System Memory Address 3 Mapping Start High Byte	SMSTH3	
82Ah	2Ah	System Memory Address 3 Mapping Stop Low Byte	SMSPL3	
82Bh	2Bh	System Memory Address 3 Mapping Stop High Byte	SMSPH3	
82Ch	2Ch	Card Memory Offset Address 3 Low Byte	MOFFL3	
82Dh	2Dh	Card Memory Offset Address 3 High Byte	MOFFH3	
82Eh	2Eh	Reserved	RSRVD	
82Fh	2Fh	Misc Control 1	MISCC1	
830h	30h	System Memory Address 4 Mapping Start Low Byte	SMSTL4	
831h	31h	System Memory Address 4 Mapping Start High Byte	SMSTH4	
832h	32h	System Memory Address 4 Mapping Stop Low Byte	SMSPL4	
833h	33h	System Memory Address 4 Mapping Stop High Byte	SMSPH4	
834h	34h	Card Memory Offset Address 4 Low Byte	MOFFL4	
835h	35h	Card Memory Offset Address 4 High Byte	MOFFH4	
836h	36h	Card I/O Offset Address 0 Low Byte	IOFFL0	
837h	37h	Card I/O Offset Address 0 High Byte	IOFFH0	
838h	38h	Card I/O Offset Address 1 Low Byte	IOFFL1	
839h	39h	Card I/O Offset Address 1 High Byte	IOFFH1	
83Ah	3Ah	General Purpose I/O	GPIO	
83Bh	3Bh	Reserved	RSRVD	
83Ch	3Ch	Reserved	RSRVD	
83Dh	3Dh	Reserved	RSRVD	
83Eh	3Eh	Reserved	RSRVD	
83Fh	3Fh	Reserved	RSRVD	
840h	NA	System Memory Page Address 0	SMPGA0	
841h	NA	System Memory Page Address 1	SMPGA1	
842h	NA	System Memory Page Address 2	SMPGA2	
843h	NA	System Memory Page Address 3	SMPGA3	
844h	NA	System Memory Page Address 4	SMPGA4	

7.4 PCIC Compatible Mode (Legacy Mode)

The R5C551 supports the PCIC compatible mode, i.e. Legacy mode, that all 16-bit Card Sockets Status/Control registers can be accessed through INDEX/DATA ports which is located at I/O address 03E0h or 03E2h. PCIC compatible mode is enabled by writing a non-zero address to 16-bit Legacy Mode Base Address register. The index register and data register are contiguous in the I/O address space so that a single 16-bit instruction can simultaneously write to the index and data registers. The below figure shows the status of INDEX/DATA ports when the Legacy Base Address register is set to either 03E0h or 03E2h.

Register Name: Legacy Index/Data Port
PCI I/O Address : 03E0h (or 03E2h)

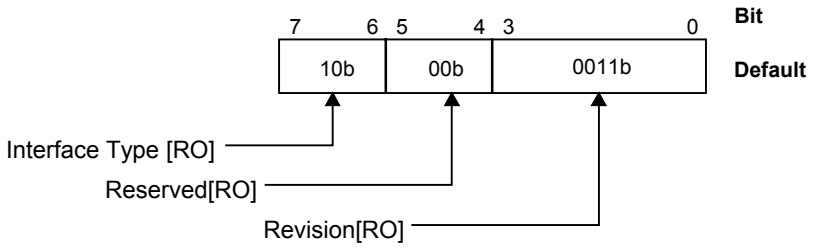


7.5 General Setup Registers

7.5.1 Identification and Revision register

This register provides the software with information on PC Card-16.

Register Name: Identification and Revision
Address Offset: 800h

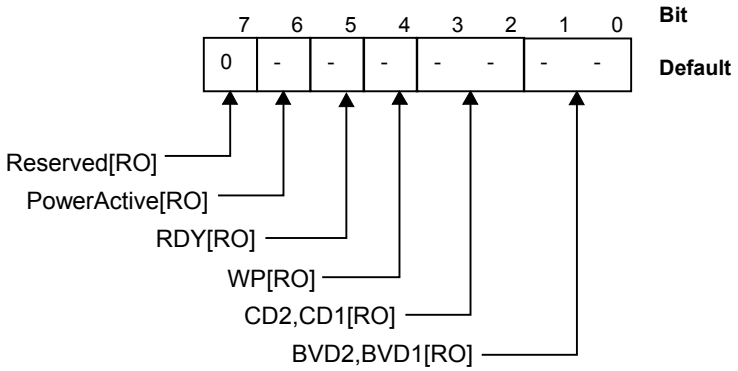


Bit	Field Name	Description
7-6	InterfaceType	This field indicates the type of PC Card-16 supported by the R5C551. The R5C551 supports the 16-bit card on the Memory and I/O interface and return 10b when read. 00 I/O only 01 Memory 10 Memory & I/O 11 Reserved
5-4	Reserved	These bits are reserved for future use. This field is read-only and returns zero when read.
3-0	Revision	This field indicates PCIC revision number. This filed is read-only and returns 0011b when read.

7.5.2 Interface Status register

This register provides information on the status of the PC Card interface.

Register Name: Interface Status
Address Offset: 801h

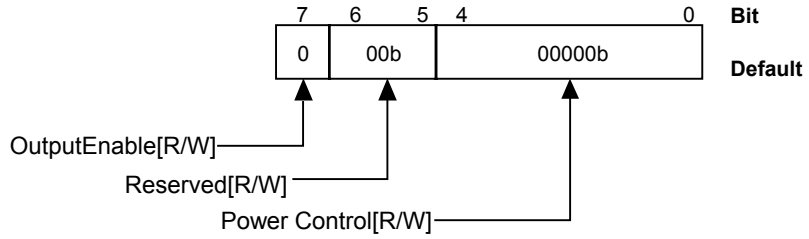


Bit	Field Name	Description
7	Reserved	This bit is reserved for future use. This bit is read-only and returns zero when read. Writing to this field has no effect.
6	PowerActive	This bit indicates whether or not the socket power is on (3.3V or 5V). This bit is set to one when either VCC3EN# or VCC5EN# is turned on, and set to zero when the socket power is turned off.
5	RDY	This bit indicates the state of the READY/IREQ# input signal. This bit is available only on the PC Card-16 memory interface, and has no meaning on the I/O interface. 0 : memory card is busy. 1 : memory card is ready.
4	WP	This bit indicates the state of the WP/IOIS16# input signal. The memory card will not be write protected unless the WriteProtect bit in the Card Memory Offset High Byte register is set to one, even if the WP signal is a one to maintain the compatibility with 82365SL B-Step. This bit is available only on the PC Card-16 memory interface.
3-2	CD2, CD1	This field returns the inverse state of CD2# and CD1# when read.
1-0	BVD2, BVD1	These bits have meanings that depend on the type of the PC Card-16 inserted in the socket. When a 16-bit memory card is inserted, this field indicates the state of the battery voltage detect signals (BVD1, BVD2) as follows: BVD2 BVD1 bit1 bit0 Card Battery Low Low 0 0 Battery Dead Low High 0 1 Warning High Low 1 0 Battery Dead High High 1 1 Battery Good When a 16-bit I/O card is inserted, Bit 0 in this field indicates the state of the BVD1#/STSCHG#/RI# input signal when the Ring Indicate Enable bit in the Interrupt and General Control register is a zero.

7.5.3 Power Control register

This register controls the output of the R5C551 to the PC Card-16 socket. This register can also control the socket power to maintain the compatibility with the PCIC.

Register Name: Power Control
Address Offset: 802h



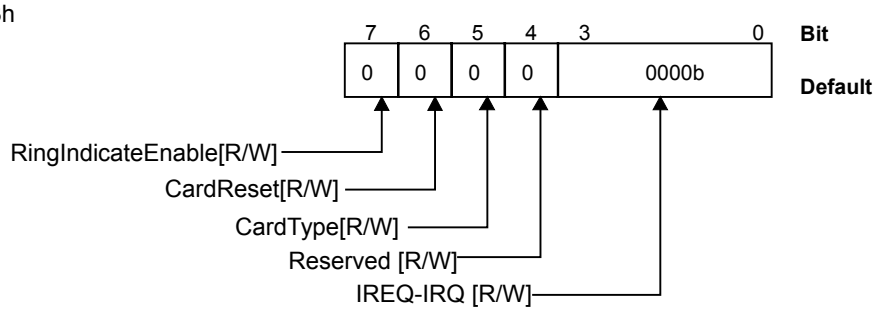
Bit	Field Name	Description
7	OutputEnable	When the R5C551 is on the 16-bit card mode, the output signals listed below are tri-stated when this bit is set to zero, and they are not tri-stated when this bit is set to one. The following output signals are the object: CE1#, CE0#,IORD#,IOWR#, OE#, WE#, RESET, ADR[25:0], DATA[15:0], REG#
6-5	Reserved(R/W)	This read/write bit is reserved for future use. Writing to this bit has no effect. The default after reset is zero.
4-0	Power Control	This bit field is used with Bit 0 in the Misc Control 1 register to control VCC3EN#, VCC5EN#, VPPEN0 and VPPEN1. Writing to these bits is enabled only either when the power is on or when the voltage is changed. The following table shows the relation between power control signals and this bit field.

Bit4	Bit3	Bit2	Bit1	Bit0	Misc Control 1 Bit0	VCC3EN#	VCC5EN#	VPPEN1	VPPEN0
1	X	X	0	0	0	1	0	0	0
1	X	X	0	0	1	0	1	0	0
1	X	X	0	1	0	1	0	0	1
1	X	X	0	1	1	0	1	0	1
1	X	X	1	0	0	1	0	1	0
1	X	X	1	0	1	0	1	1	0
1	X	X	1	1	0	1	0	1	1
1	X	X	1	1	1	0	1	1	1
0	X	X	X	X	X	1	1	0	0

7.5.4 Interrupt and General Control register

This register controls Ring Indicate Enable, Card Reset, Card Type and Interrupt Steering of IRQs from I/O PC Card-16.

Register Name: Interrupt and General Control
Address Offset: 803h



Bit	Field Name	Description
7	RingIndicateEnable	On the I/O card interface mode, when this bit is set to one, the STSCHG#/RI# from the PC Card-16 signal is used as a Ring Indicator signal and is passed through to the RI_OUT# pin. When this bit is set to zero, the STSCHG#/RI# from the I/O PC Card-16 signal is used as the status change signal STSCHG#. The current status of the signal is then available to the read from the Interface Status register and this signal can be configured as a source for the card status change interrupt. This bit has no meaning on the memory card interface mode.
6	CardReset	When this bit is set to zero, the Reset signal to the PC Card-16 is activates. This signal will be active until this bit is set to one,
5	CardType	This bit indicates the PC Card type. When this bit is set to zero, a memory card interface is selected. When this bit is set to one, an I/O card interface is selected.
4	Reserved(R/W)	This read/write bit is reserved for future use.
3-0	IREQ-IRQ	This field selects the interrupt routing for the IREQ#/CINT# signal from I/O PC Card-16. These bits are available only when the IREQ-ISA Enable bit in the Bridge control register is set bit3 bit2 bit1 bit0 IRQ selection 0 0 0 0 IRQ disabled 0 0 0 1 Reserved 0 0 1 0 Reserved 0 0 1 1 IRQ3 0 1 0 0 IRQ4 0 1 0 1 IRQ5 0 1 1 0 Reserved 0 1 1 1 IRQ7 1 0 0 0 Reserved 1 0 0 1 IRQ9 1 0 1 0 IRQ10 1 0 1 1 IRQ11 1 1 0 0 IRQ12 1 1 0 1 Reserved 1 1 1 0 IRQ14 1 1 1 1 IRQ15

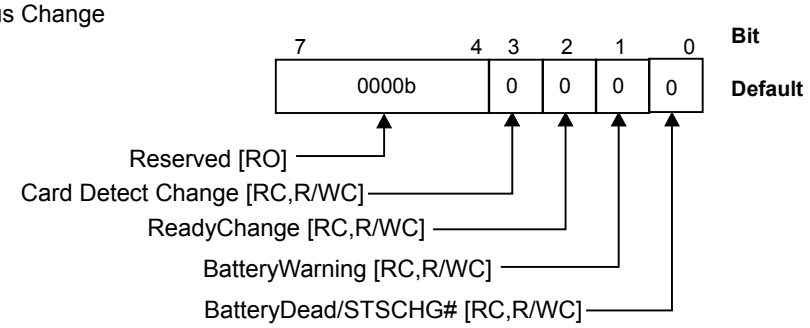
7.5.5 Card Status Change register

This register contains the status for sources of the card status change interrupts. These sources can be enabled to generate a card status change interrupt by setting the corresponding bit in the Card Status Change Interrupt Configuration register. Each bits in this register read back 0 when the corresponding status enable bits in the Card Status change Interrupt Configuration are set to 0.

When the Card Status Change Acknowledge mode bit in the 16-bit Global Control register is set to 1, the acknowledgment of sources for the Card Status Change Interrupt is performed by writing back 1 to the appropriate bit in the Cad Status Change Register that was read as 1b. Once the internal source is acknowledged by writing a 1 to the bit, the bit reads back as 0. The interrupt signal INTA# or IRQx responding to the card status change maintains to be active, if enabled on a system IRQ line, until all of the bits in this register are zero. When the Card Status Change Acknowledge mode bit in the 16-bit Global Control register is not set, the Card Status Change Interrupt signal maintains to be active, if enabled on a system IRQ line, until the Card Status Change register is read. The read operation to the Card Status Change register resets all bits in the register.

If two or more Card Status Change Interrupt is pending or a Card Status Change Interrupt condition occurs while another is being serviced, the R5C551 does not generate a second interrupt. The interrupt service routing must read the Card Status Change register to ensure that all interrupt requests is serviced before exiting the service routines.

Register Name: Card Status Change
Address Offset: 804h

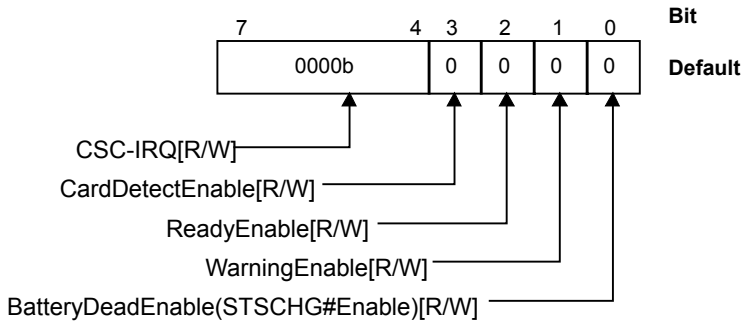


Bit	Field Name	Description
7-4	Reserved	This field is reserved for future use. This field is read-only and returns zeros when read.
3	Card Detect Change	This bit is set to 1 when a change on either CD1# or CD2# signals occurs. This bit is not set unless the Card Detect Enable bit in the Card Status Change Interrupt Configuration register is set. Both CCD1# and CCD2# bits in the Socket Event register are cleared by a read clear or a write back clear. And also, this bit is cleared when either CCD1# or CCD2#, or both of CCD1# and CCD2# are cleared by a write back clear.
2	ReadyChange	This bit is set to 1 when a low-to-high transition occurs on the RDY/BSY# signal, indicating that the memory PC Card-16 is ready to accept a new data transfer. This bit is not set unless the Ready Enable bit in the Card Status Change Interrupt Configuration register is set. This bit is always zero on I/O PC Card-16.
1	BatteryWarning	This bit is set to 1 when a battery warning condition is detected. This bit is not set unless the Battery Warning Enable bit in the Card Status Change Interrupt Configuration register is set. This bit is always zero on I/O PC Card-16.
0	BatteryDead /STSCHG#	On the memory PC Card-16 interface mode, this bit is set to 1 when a battery dead condition is detected. On the I/O PC Card-16 interface mode, this bit is set to 1 when the BVD1/STSCHG# signal is asserted “low”, but then, this bit reads back as 0 if the Ring Indicate Enable bit in the Interrupt and General Control register is set to 1. This bit is not set unless the Battery Enable bit in the Card Status Change Interrupt Configuration register is set.

7.5.6 Card Status Change Interrupt Configuration register

This register controls the steering of Card Status Change Interrupt and the enabling of Card Status Change Interrupt.

Register Name: Card Status Change InterruptConfiguration
Address Offset: 805h

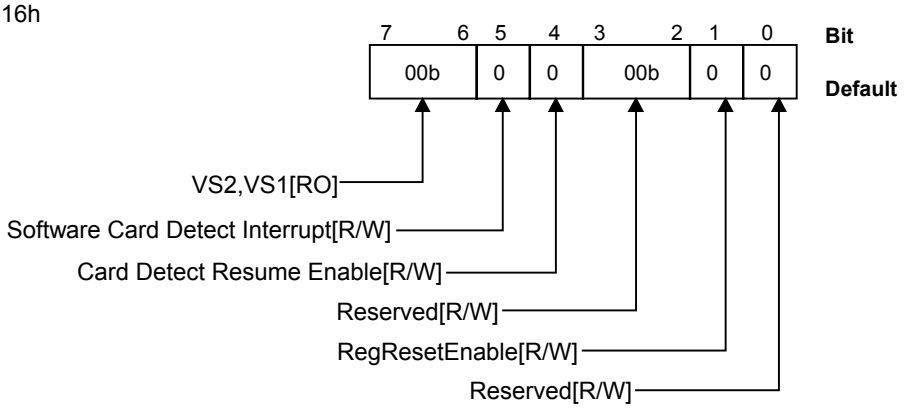


Bit	Field Name	Description
7-4	CSC-IRQ	This field selects the interrupt routing for card status change interrupts. When this field is set to the reserved value or 0000b, the card status change interrupt is routed to INTA#. The default after reset is 0000b. This field is reset when the RegResetEnable bit in the Card Detect and General Control register is set and the card is removed. bit7 bit6 bit5 bit4 IRQ selection 0 0 0 0 IRQ disabled 0 0 0 1 Reserved 0 0 1 0 Reserved 0 0 1 1 IRQ3 0 1 0 0 IRQ4 0 1 0 1 IRQ5 0 1 1 0 Reserved 0 1 1 1 IRQ7 1 0 0 0 Reserved 1 0 0 1 IRQ9 1 0 1 0 IRQ10 1 0 1 1 IRQ11 1 1 0 0 IRQ12 1 1 0 1 Reserved 1 1 1 0 IRQ14 1 1 1 1 IRQ15
3	CardDetectEnable	When this bit is set to 1, the interrupt is generated when a change is detected on either CD1# or CD2#.
2	ReadyEnable	Setting this bit to 1 enables the card status change interrupt when a low-to-high transaction occurs on the RDY/BSY# signal. This bit has no meaning on the I/O PC Card-16 interface.
1	BatteryWarningEnable	Setting this bit to 1 enables the card status change interrupt when a battery warning conditions is detected. This bit has no meaning on the I/O PC-Card-16 interface.
0	BatteryDeadEnable (STSCHG#Enable)	Setting this bit to 1 enables a Card Status Change Interrupt when a battery dead condition is detected in a memory PC Card-16. In an I/O PC Card-16, setting this bit to 1 enables a Card Status Change Interrupt when the BVD1/STSCHG# signal is pulled “Low”. Setting this bit to 0 disables the interrupt.

7.5.7 Card Detect and General Control register

This register is used to reset the configuration registers and report the selected status of voltage stored to the card.

Register Name: Card Detect and General Control
Address Offset: 816h

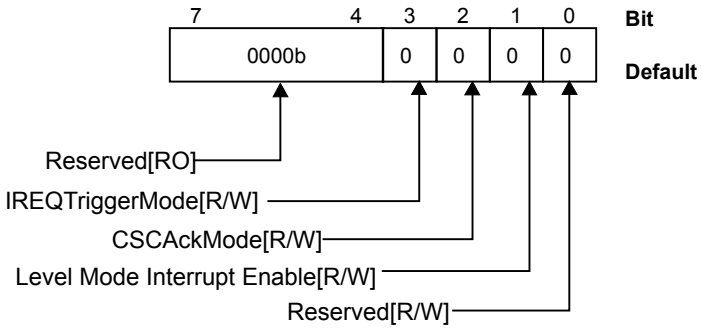


Bit	Field Name	Description
7-6	VS2, VS1	These bits indicate the state of VS2 and VS1. The default after reset is zero.
5	Software Card Detect Interrupt	Setting this bit to 1 enables to generate the Card Detected Interrupt, and then one should note that both CCD1# and CCD2# bits in the Socket Event register are set by writing to this bit. This bit is a phantom bit and returns zero when read.
4	Card Detect Resume Enable	When this bit is set to1, then once a card detect change is detected on the CD1# or CD2# inputs, RI_OUT# output goes from “high” to “low”.
3-2	Reserved(R/W)	This read/write field is reserved for future use. The default after reset is zero.
1	RegResetEnable	When this bit is set to 1, a reset pulse is generated to reset the following configuration registers for the socket to their default state (zero’s) when both the CD1# and CD2# inputs for the socket go “high”. Interrupt and General Control Card Detect Interrupt Configuration (CSC-IRQ bits only*) Address Window Enable I/O Control I/O Address {0,1} Start Low Byte I/O Address {0,1} Start High Byte I/O Address {0,1} Stop Low Byte I/O Address {0,1} Stop High Byte System Memory Address {0,1,2,3,4} Start Low Byte System Memory Address {0,1,2,3,4} Start High Byte System Memory Address {0,1,2,3,4} Stop Low Byte System Memory Address {0,1,2,3,4} Stop High Byte Card Memory Offset Address {0,1,2,3,4} Start Low Byte Card Memory Offset Address {0,1,2,3,4} Start High Byte Card Memory Offset Address {0,1,2,3,4} Stop Low Byte Card Memory Offset Address {0,1,2,3,4} Stop High Byte
0	Reserved(R/W)	This read/write bit is reserved for future use. The default after reset is zero.

7.5.8 16 bit Global Control register

This register controls both PC Card sockets, and is not duplicated for each socket. PCI reset clears all bits in this register.

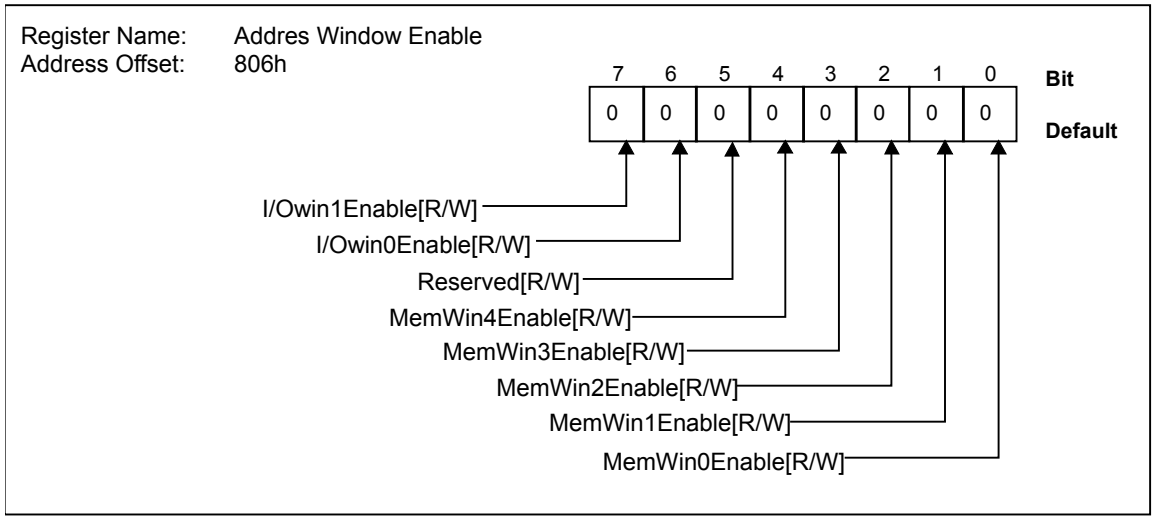
Register Name: 16 bit Global Control
Address Offset: 81Eh



Bit	Field Name	Description
7-4	Reserved	This field is reserved for future use. This field is read-only and returns zero when read.
3	IREQTriggerMode	This bit selects level mode interrupts for IRQx generated by the particular PC card interrupts. When this bit is set to 1, it selects level mode. And also when this bit is set to 0, it selects edge mode. The default is zero.
2	CSCAckMode	When this bit is set to 1, each Card Status Change Interrupt is acknowledged with an explicit write of 1 to the Card Status Change register bit that identifies the interrupt. - A corresponding bit is reset to 0. When this bit to 0, each Card Status Change Interrupt is acknowledged by reading the Card Status Change register. - All of bits are reset to 0.
1	Level Mode Interrupt Enable	When this bit is set to1, level mode is selected. And IRQx goes from tri-stated to low whenever the interrupt is active. When this bit is set to 0, edge mode is selected. Moreover, IRQx goes from tri-stated to low when the interrupt is enabled, and go from low to high when the interrupt is active, and go to low when the interrupt is inactive. This bit is tri-stated when the interrupt is disabled.
0	Reserved(R/W)	This read/write bit is reserved for future use.

7.5.9 Address Window Enable register

This register controls enabling of the memory and I/O mapping windows to the PC Card memory or I/O space. All bits in this register are cleared after reset.



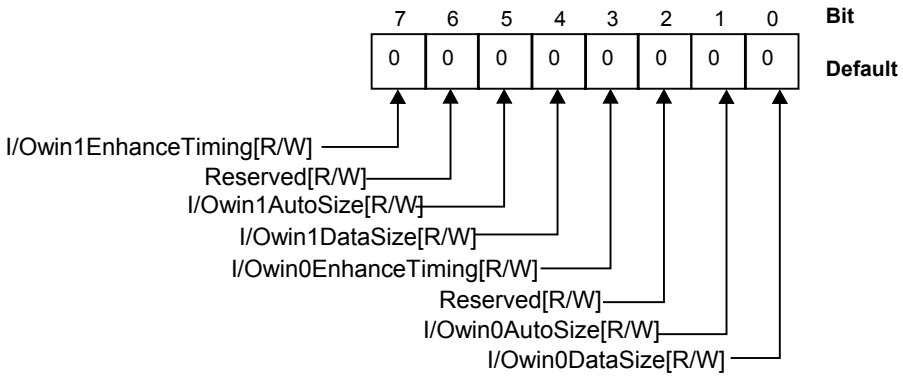
Bit	Field Name	Description
7	I/Owin1Enable	This bit controls whether or not the I/O window 1 is enabled. When this bit is set to 0, the card enable signal is inhibited to access to the PC Cards through the I/O window 1. When this bit is set to 1, the card enable signal is not inhibited when access addresses to the PC Cards are passed to the I/O window 1. Start and Stop registers in the corresponding window must be set to the proper value before setting this bit.
6	I/Owin0Enable	This bit controls whether or not the I/O window 0 is enabled. When this bit is set to 0, the card enable signal is inhibited to access to the PC Cards through the I/O window 0. When this bit is set to 1, the card enable signal is not inhibited when access addresses to the PC Cards are passed to the I/O window 0. Start and Stop registers in the corresponding window must be set to the proper value before setting this bit.
5	Reserved(R/W)	This read/write bit is reserved for future use. The default after reset is zero.
4	MemWin4Enable	This bit controls whether or not the memory window 4 is enabled. When this bit is set to 0, the card enable signal is inhibited to access to the PC Cards through the memory window 4. When this bit is set to 1, the card enable signal is not inhibited when access addresses to the PC Cards are passed to the memory window 4. Start and Stop registers in the corresponding window must be set to the proper value before setting this bit.
3	MemWin3Enable	This bit controls whether or not the memory window 3 is enabled. When this bit is set to 0, the card enable signal is inhibited to access to the PC Cards through the memory window 3. When this bit is set to 1, the card enable signal is not inhibited when access addresses to the PC Cards are passed to the memory window 4. Start and Stop registers in the corresponding window must be set to the proper value before setting this bit.
2	MemWin2Enable	This bit controls whether or not the memory window 2 is enabled. When this bit is set to 0, the card enable signal is inhibited to access to the PC Cards through the memory window 2. When this bit is set to 1, the card enable signal is not inhibited when access addresses to the PC Cards are passed to the memory window 4. Start and Stop registers in the corresponding window must be set to the proper value before setting this bit.
1	MemWin1Enable	This bit controls whether or not the memory window 1 is enabled. When this bit is set to 0, the card enable signal is inhibited to access to the PC Cards through the memory window 1. When this bit is set to 1, the card enable signal is not inhibited when access addresses to the PC Cards are passed to the memory window 4. Start and Stop registers in the corresponding window must be set to the proper value before setting this bit.
0	MemWin0Enable	This bit controls whether or not the memory window 0 is enabled. When this bit is set to 0, the card enable signal is inhibited to access to the PC Cards through the memory window 0. When this bit is set to 1, the card enable signal is not inhibited when access addresses to the PC Cards are passed to the memory window 4. Start and Stop registers in the corresponding window must be set to the proper value before setting this bit.

7.6 I/O Window Control Registers

7.6.1 I/O Control register

This register controls the I/O data path size and the access timing specification for the I/O windows 0 and 1. All bits in this register are cleared after reset.

Register Name: I/O Control
Address Offset: 807h

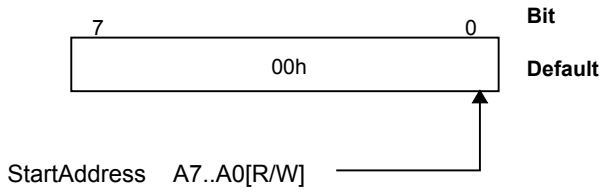


Bit	Field Name	Description
7	I/Owin1Enhance Timing	When this bit is set to 1, 16-bit I/O card access timing for I/O window 1 is determined by user defined timing in the 16-bit I/O timing 0 register. When this bit is set to 0, the default timing is selected. The default after reset is zero. User defined timing is valid when 16-bit I/O Enhance Timing bit in the 16-bit Interface Control register is set to 1 regardless of this bit being set to 0.
6	Reserved(R/W)	This read/write bit is reserved for future use. The default after reset is zero.
5	I/Owin1AutoSize	This bit indicates how to select the I/O data path size to the PC Card-16. When this bit is set to 1, the data path size for I/O window 1 is determined by the IOIS16# signal from PC Card-16. When this bit is set to 0, it is determined by the I/Owin1DataSize bit.
4	I/Owin1DataSize	This bit selects the I/O data path size to the PC Card-16. When this bit is set to 1, 16-bit data path is selected. When this bit is set to 0, 8-bit data path is selected. This bit is ignored when I/Owin1AutoSize is 1b. This bit takes precedence of PCI command.
3	I/Owin0Enhance Timing	When this bit is set to 1, 16-bit I/O card access timing for I/O window 0 is determined by user defined timing in the 16-bit I/O timing 0 register. When this bit is set to 0, the default timing is selected. The default after reset is zero. User defined timing is valid when 16-bit I/O Enhance Timing bit in the 16-bit Interface Control register is set to 1 regardless of this bit being set to 0.
2	Reserved(R/W)	This read/write bit is reserved for future use. The default after reset is zero.
1	I/Owin0AutoSize	This bit indicates how to select the I/O data path size to the PC Card-16. When this bit is set to 1, the data path size for I/O window 0 is determined by the IOIS16# signal from PC Card-16. When this bit is set to 0, it is determined by the I/Owin0DataSize bit.
0	I/Owin0DataSize	This bit selects the I/O data path size to the PC Card-16. When this bit is set to 1, 16-bit data path is selected. When this bit is set to 0, 8-bit data path is selected. This bit is ignored when I/Owin0AutoSize is 1b. This bit has priority over the PCI command.

7.6.2 I/O Address 0-1 Start Low Byte register

These two registers contain the lower address bits that are used to determine the start address of the corresponding I/O address windows 0 and 1. This provides a minimum 1 byte window for the corresponding I/O address window if the start address and stop address are the same.

Register Name: I/O Address 0-1 Start Low Byte
Address Offset: 808h,80Ch



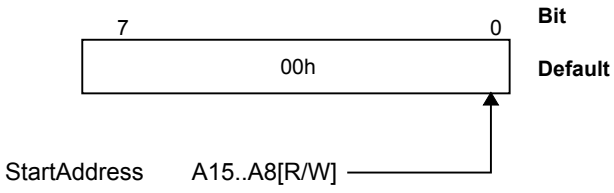
	Window 0	*Window 1*
Offset	808h	80Ch

Bit	Field Name	Description
7-0	StartAddress A7..A0	I/O Window 0-1 Start Address A7 .. A0:

7.6.3 I/O Address 0-1 Start High Byte register

These two registers contain the upper address bits that are used to determine the start address of the corresponding I/O address windows 0 and 1.

Register Name: I/O Address 0-1 Start High Byte
Address Offset: 809h,80Dh



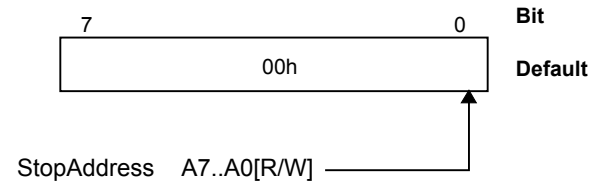
	Window 0	*Window 1*
Offset	809h	80Dh

Bit	Field Name	Description
7-0	StartAddress A15..A8	I/O Window 0-1 Start Address A15..A8:

7.6.4 I/O Address 0-1 Stop Low Byte register

These two registers contain the lower address bits that are used to determine the top address of the corresponding I/O address windows 0 and 1. This provides a minimum 1 byte window for the corresponding I/O address window if the start address and stop address are the same.

Register Name: I/O Address 0-1 Stop Low Byte
Address Offset: 80Ah,80Eh



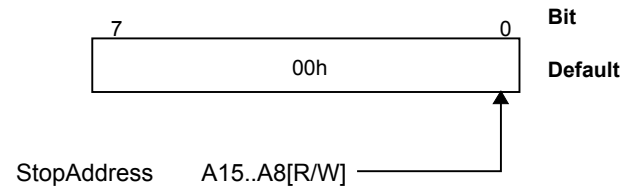
	Window 0	*Window 1*
Offset	80Ah	80Eh

Bit	Field Name	Description
7-0	StopAddress A7..A0	I/O Window 0-1 Stop Address A7 .. A0:

7.6.5 I/O Address 0-1 Stop High Byte register

These two registers contain the upper address bits that are used to determine the stop address of the corresponding I/O address windows 0 and 1.

Register Name: I/O Address 0-1 Stop High Byte
Address Offset: 80Bh,80Fh



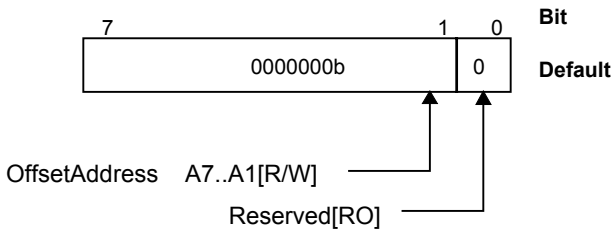
	Window 0	*Window 1*
Offset	80Bh	80Fh

Bit	Field Name	Description
7-0	StopAddress A15..A8	I/O Window 0-1 Stop Address A15..A8:

7.6.6 Card I/O Offset Address 0-1 Low Byte register

These two registers contain the lower offset address bits that are added to system address bits A [7:1] to generate the PC Card-16 I/O address for I/O address windows 0 and 1.

Register Name: Card I/O Offset Address 0-1 Low Byte
Address Offset: 836h,838h



	Window 0	*Window 1*
Offset	836h	838h

Bit	Field Name	Description
7-1	Offset Address A7..A1	I/O Window 0-1 Card I/O Offset Address A7..A1:
0	Reserved	This bit is reserved and returns zero when read.

7.6.7 Card I/O Offset Address 0-1 High Byte register

These two registers contain the upper offset address bits that are added to the system address bits A [15:8] to generate the PC Card-16 I/O address for I/O address windows 0 and 1.

Register Name: Card I/O Offset Address 0-1 High Byte
Address Offset: 837h,839h

	Window 0	*Window 1*
Offset	837h	839h

Bit	Field Name	Description
7-0	OffsetAddress A15..A8	I/O Window 0-1Offset Address A15..A8:

7.7 Memory Window Control Registers

7.7.1 System Memory Address 0-4 Mapping Start Low Byte register

These five registers contain the lower address bits that indicate the start address of the system memory address mapping windows 0,1,2,3 and 4. The register's contents correspond to PCI memory address bits A [19:12], and are used to determine whether memory accesses are valid. Therefore mapping of each system memory can start and stop on any 4Kbyte boundary of the system memory.

Register Name: System Memory Address 0-4 Mapping Start Low Byte
Address Offset: 810h,818h,820h,828h,830h

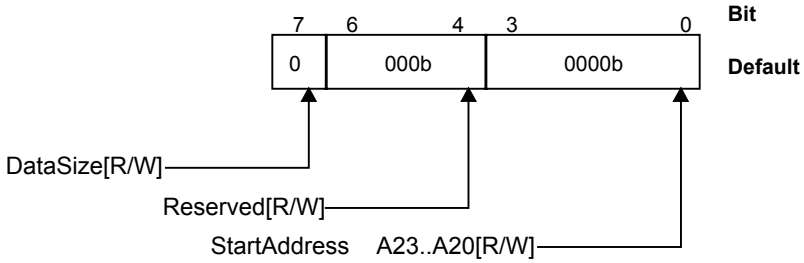
	Window0	*Window1*	*Window2*	*Window3*	*Window4*
Offset	810h	818h	820h	828h	830h

Bit	Field Name	Description
7-0	StartAddress A19..A12	System Memory Address Mapping Window 0-4 Start Address A19 .. A12:

7.7.2 System Memory Address 0-4 Mapping Start High Byte register

These five registers contain the upper address bits that indicate the start address of the system memory address mapping windows 0,1,2,3 and 4. The register's contents correspond to PCI memory address bits A [23:20], and are used to determine whether memory accesses are valid. And also, the data path size for each window is controlled by a bit of corresponding register.

Register Name: System Memory Address 0-4 Mapping Start High Byte
Address Offset: 811h,819h,821h,829h,831h



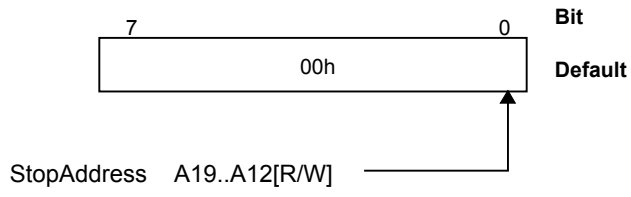
	Window0	*Window1*	*Window2*	*Window3*	*Window4*
Offset	811h	819h	821h	829h	831h

Bit	Field Name	Description
7	DataSize	This bit selects the memory data path size to the PC Card-16. When this bit is set to 1, 16-bit data path is selected. When this bit is set to 0, 8-bit data path is selected. This bit has priority over the PCI command.
6-4	Reserved(R/W)	This read/write bit field is reserved.
3-0	StartAddress A23..A20	System Memory Address Mapping Window 0-4 Start Address A23 .. A20:

7.7.3 System Memory Address 0-4 Mapping Stop Low Byte register

These five registers contain the lower address bits that indicate the stop address of the corresponding system memory address mapping windows 0,1,2,3 and 4. The register's contents correspond to PCI memory address bits A [19:12], and are used to determine whether memory accesses are valid.

Register Name: System Memory Address 0-4 Mapping Stop Low Byte
Address Offset: 812h,81Ah,822h,82Ah,832h



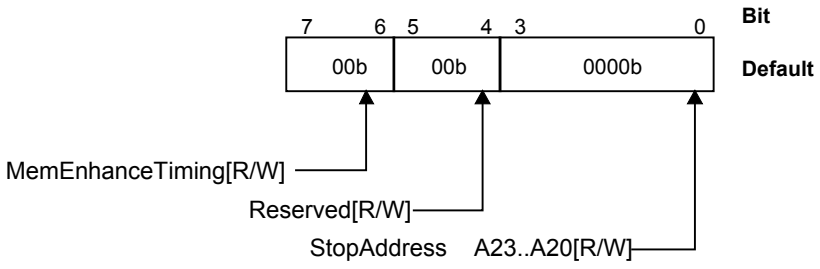
	Window0	*Window1*	*Window2*	*Window3*	*Window4*
Offset	812h	81Ah	822h	82Ah	832h

Bit	Field Name	Description
7-0	StopAddress A19..A12	System Memory Address Mapping Window 0-4 Stop Address A19 .. A12:

7.7.4 System Memory Address 0-4 Mapping Stop High Byte register

These five registers contain the upper address bits that indicate the stop address of the corresponding system memory address mapping windows 0,1,2,3 and 4. The register's contents correspond to PCI memory address bits A [23:20], and are used to determine whether memory accesses are valid. Two bits in each of the registers select the PC Card-16 access timing for the corresponding system memory window.

Register Name: System Memory Address 0-4 Mapping Stop High Byte
Address Offset: 813h,81Bh,823h,82Bh,833h



	Window0	*Window1*	*Window2*	*Window3*	*Window4*
Offset	813h	81Bh	823h	82Bh	833h

Bit	Field Name	Description
7-6	MemEnhanceTiming	Timing parameters for memory PC Card-16 are independently configured for each Common Memory Window by programming these timing bits. The default timing mode is 00b, and only the default timing is used for Attribute memory. User defined timing is valid when 16-bit Memory Enhance Timing bit in the 16-bit Interface Control register is set to 1 regardless of this bit being set to 0. 00b = Default Timing 01b = Enhance Timing 10b = Enhance Timing 11b = Enhance Timing
5-4	Reserved(R/W)	This read/write bit field is reserved.
3-0	StopAddress A23..A20	System Memory Address Mapping Window 0-4 Stop Address A23 .. A20:

7.7.5 Card Memory Offset Address 0-4 Low Byte register

These five registers contain the lower offset address bits that are added to system address bits A [19:12] to generate the PC Card-16 memory address for I/O windows 0,1,2,3 and 4.

Register Name: Card Memory Offset Address 0-4 Low Byte
Address Offset: 814h,81Ch,824h,82Ch,834h

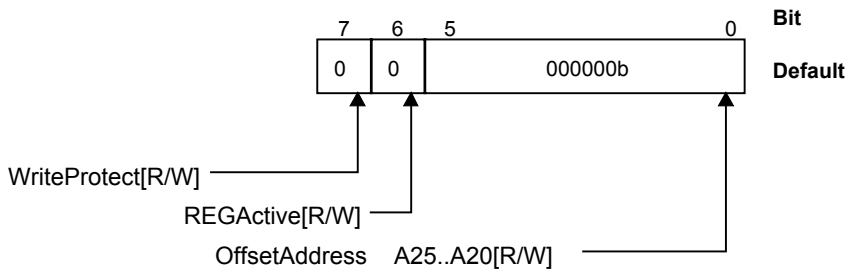
	Window0	*Window1*	*Window2*	*Window3*	*Window4*
Offset	814h	81Ch	824h	82Ch	834h

Bit	Field Name	Description
7-0	OffsetAddress A19..A12	Card Memory Offset Address A19 .. A12:

7.7.6 Card Memory Offset Address 0-4 High Byte register

These five registers contain the upper offset address bits that are added to system address bits A [23:20] to generate the PC Card-16 memory address for I/O windows 0,1,2,3 and 4. These register also control PC Card-16 memory software write protect for the corresponding system memory windows, and select whether the memory windows are mapped to attribute memory, or to common memory on the PC Card-16.

Register Name: Card Memory Offset Address 0-4 High Byte
Address Offset: 815h,81Dh,825h,82Dh,835h (8 bit)



	Window0	*Window1*	*Window2*	*Window3*	*Window4*
Offset	815h	81Dh	825h	82Dh	835h

Bit	Field Name	Description
7	WriteProtect (WP)	When this bit is set to 1, write transactions to the PC Card-16 through the corresponding system memory window are inhibited. When this bit is set to 0, write transactions are allowed. The WP switch on the memory card sets the Memory Write Protect bit in the Interface Status register, but setting it can block the memory write cycles.
6	REGActive	When this bit is set to 1, accesses to the system memory window are changed over accesses to the attribute memory on the PC Card by asserting REG# “low”. When this bit is set to 0, accesses to the system memory window are changed over accesses to the common memory on the PC Card by asserting REG# “high”.
5-0	OffsetAddress A25..A20	Card Memory Offset Address A25 .. A20:

7.7.7 System Memory Page Address 0-4 register

This register contains an eight bit page address that allows selection of a 16 Mbyte window page in the four Gbyte memory address space in which socket memory window are mapped. Access to a window is allowed only when the page address in the corresponding Card Memory Page Address register matches PCI memory address bits A [31:24], indicating a page hit. Reset clears all bits in this register, so that the default page is the first page (i.e., 0-16 Mbyte address range). This register cannot be accessed through I/O address 3E0h/3E2h ports.

Register Name: System Memory Page Address 0-4
Address Offset: 840, 841, 842, 843, 844h (8bit)

	Window0	*Window1*	*Window2*	*Window3*	*Window4*
Offset	840h	841h	842h	843h	844h

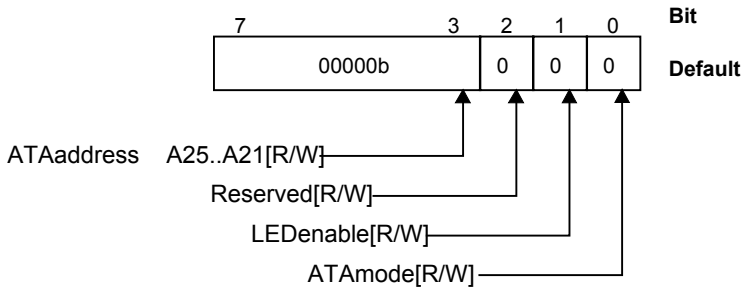
Bit	Field Name	Description
7-0	PageAddress A31..A24	System Memory Page Address A31 .. A24:

7.8 Special Function Registers

7.8.1 ATA Control register

This register contains the information is used for PCMCIA-ATA mode.

Register Name: ATA Control
Address Offset: 81Fh (8 bit)

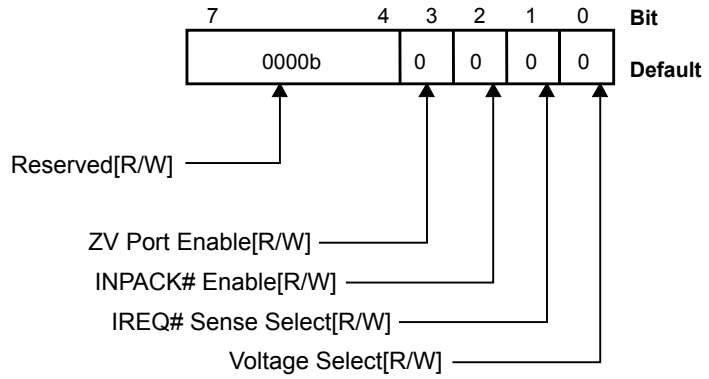


Bit	Field Name	Description
7-3	ATAaddressA25..A21	This field contains the card address 25-21 in PCMCIA-ATA mode. This field has no effect excepting this meaning.
2	Reserved(R/W)	This read/write bit is reserved.
1	LEDenable	When this bit is set to1, IRQ12 becomes open drain output suitable for driving an LED (driven whenever the card-SPKR output is turned on, and corresponding SPKR# is LED input bit is set). This bit works independent of Bit 0 (ATA mode).
0	ATAmode	When this bit is set to 1, PCMCIA-ATA mode is selected.

7.8.2 Misc Control 1 register

This register controls the miscellaneous signals like INPACK# and IREQ# for the PC Card-16.

Register Name: Miscellaneous Control 1
Address Offset: 82Fh (8 bit)

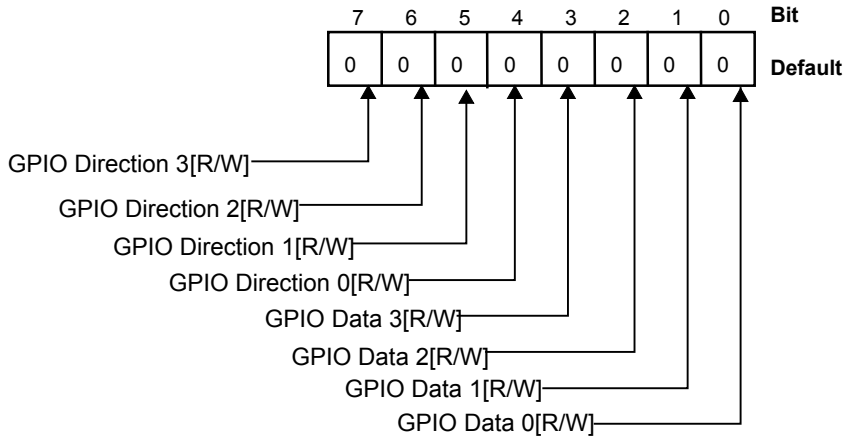


Bit	Field Name	Description
7-4	Reserved(R/W)	This read/write bit is reserved for future use.
3	ZV Port Enable	When this bit is set to 1, the PC Card-16 interface is Zoomed Video Port mode. Therefore, the card address lines CADR [25:4] are put in tri-state, and then replaced by Zoomed Video Port signals, with BVD2/SPKR# and INPACK#, which carry video/audio data from the PC Card-16 to the ZV port. The default is zero.
2	INPACK# Enable	When this bit is set to 1, the INPACK# signal is enabled on the PC Card-16 interface. The R5C551 returns ones on I/O read unless INPACK# is asserted, and ends normally. When this bit is set to 0, the INPACK# signal is disabled.
1	IREQ Sense Select	When this bit is set to 1, the IREQ# signal is “high” active. When this bit is set to 0, the IREQ# signal is “low” active.
0	Voltage Select	This bit is used with Bit4-0 in the Power Control register in order to control the Socket voltage. The setting is described in Power Control Register section.

7.8.3 General Purpose I/O register

The R5C551 assigns IRQ [3,4,5,7] pins to GPIO (General Purpose I/O) pins when Serialized IRQ mode is selected and the Misc Control 4 register is set. User can be free to use these I/O pins. When GPIO Enale bit is set to one, the default of GPIO is Input mode. And Bit [3:0] indicates the state of mode. In Output mode, GPIO [3:0] output the contents written in each bit. This register linking to the General Purpose I/O 1 register reflects the General Purpose I/O 1 register (AAh). On the other hand, the General Purpose I/O 1 register also reflects this register.

Register Name: General Purpose I/O
Address Offset: 83Ah (8 bit)



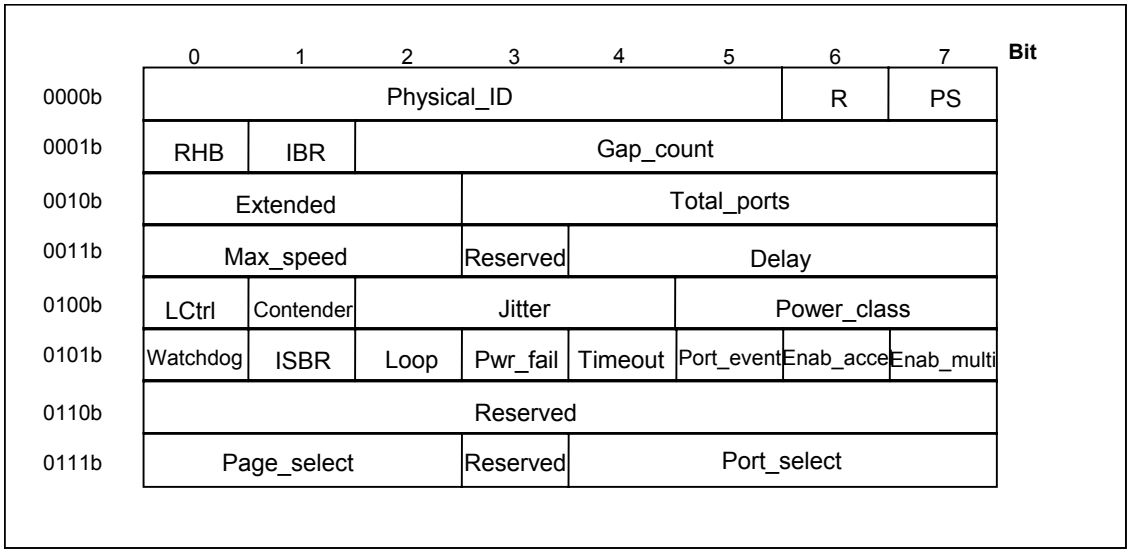
Bit	Field Name	Description
7	GPIO Direction 3	GPIO Data 3 I/O change signal. When this bit is set to 0, GPIO Data 3 is input. When this bit is set to 1, CPIO Data 3 is output. The default is zero.
6	GPIO Direction 2	GPIO Data 2 I/O change signal. When this bit is set to 0, GPIO Data 2 is input. When this bit is set to 1, CPIO Data 2 is output. The default is zero.
5	GPIO Direction 1	GPIO Data 1 I/O change signal. When this bit is set to 0, GPIO Data 1 is input. When this bit is set to 1, CPIO Data 1 is output. The default is zero.
4	GPIO Direction 0	GPIO Data 0 I/O change signal. When this bit is set to 0, GPIO Data 0 is input. When this bit is set to 1, CPIO Data 0 is output. The default is zero.
3	GPIO Data 3	General Purpose I/O bit 3. The default is input.
2	GPIO Data 2	General Purpose I/O bit 2. The default is input.
1	GPIO Data 1	General Purpose I/O bit 1. The default is input.
0	GPIO Data 0	General Purpose I/O bit 0. The default is input.

8 1394 PHY REGISTERS

8.1 Access

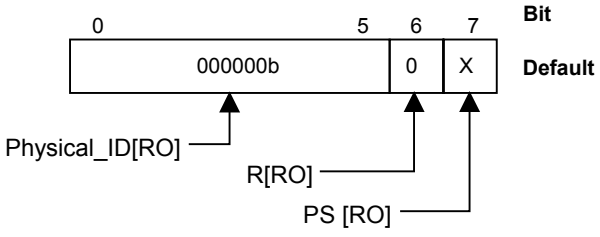
Each 1394 PHY register is usually accessible from the PHY Control register of 1394 OHCI. The Contender bit, the Power_class field and the Disabled bits of Port0/1 can be accessible through the Phy shadow register on the PCI Configuration register. Please refer to the PHY Control registers chapter for details.

8.2 Register Map



8.2.1 Register0

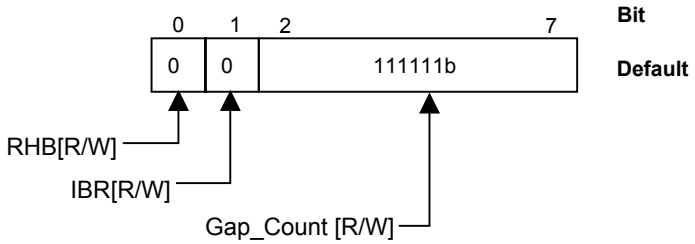
Register Name: Register0
Address Offset: 00h



Bit	Field Name	Description
0-5	Physical_ID	**Physical_ID:** Physical Node ID This bit indicates an ID decided on transmission of Self-ID packet during the Self-ID period. This bit is initialized by Bus Reset.
6	R	**R:** root indicator This bit indicates that this node is the root, is decided during the Tree-ID period, when this bit is set to '1'.
7	PS	**PS:** Cable Power Status This bit indicates a state of power supplying from the cable when this bit is set to '1'. This bit reflects the value of CPS.

8.2.2 Register1

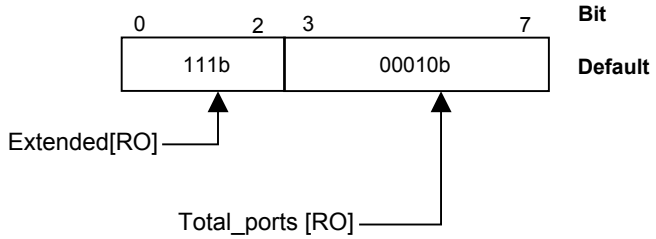
Register Name: Register1
Address Offset: 01h



Bit	Field Name	Description
0	RHB	**RHB:** Root Hold Bit This bit requests that this node becomes root during the next bus reset, when this bit is set to '1'. The occurrence of the bus reset with no active port make this bit clear. This bit is automatically set according to the PHY configuration packet send/receive condition.
1	IBR	**IBR:** Initiate Bus Reset Bus reset is started immediately when this bit is set to '1'. This bit is initialized by bus reset.
2-7	Gap_Count	**Gap_Count:** Gap Count This bit is automatically set according to the PHY configuration packet send/receive condition. This bit value is held on the first bus reset occurring. But, the next bus reset initializes this bit.

8.2.3 Register2

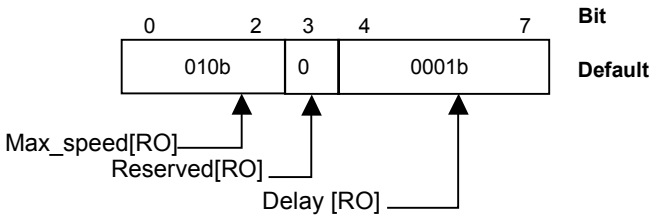
Register Name: Register2
Address Offset: 02h



Bit	Field Name	Description
0-2	Extended	**Extended:** This field is Register Map, which the R5C551 supports. Return '111b' when read.
3-7	Total_ports	**Total_ports:** Total of Port This field indicates the number of ports, which the R5C551 has. Returns 00010b when read.

8.2.4 Register3

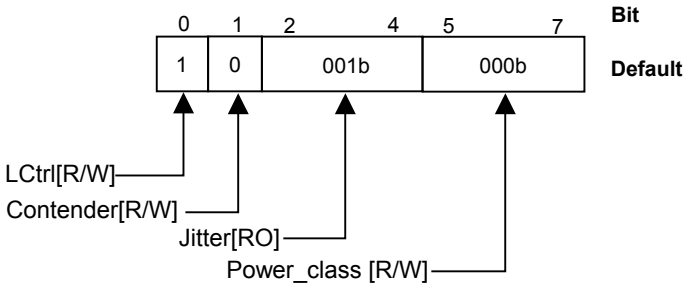
Register Name: Register3
Address Offset: 03h



Bit	Field Name	Description
0-2	Max_Speed	**Max_Speed:** Speed This field indicates the maximum transfer speed, which the R5C551 supports. Usually, return 2('010b') when read.
3	Reserved	**Reserved:** Usually, return 0 ('0b') when read.
4-7	Delay	**Delay:** This field indicates the worst case time of Delay when the R5C551 repeats. Usually, return 1 ('0001b') when read. The maximum repeat delay time of the R5C551 is 164ns.

8.2.5 Register4

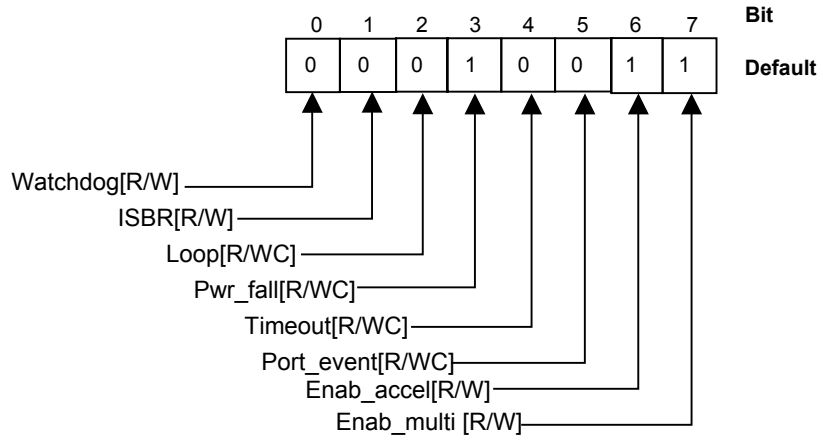
Register Name: Register4
Address Offset: 04h



Bit	Field Name	Description
0	LCtrl	**LCtrl:** LCtrl This bit controls the L (L Ctrl) field value of Self-ID packet. The value that the logic product of the Link active signal detected by this bit and LPS was taken in the Self-ID packet L (L Ctrl) field is reflected. This bit is initialized to '1' by GBRST#.
1	Contender	**Contender:** CMC This bit is reflected on the c (CONTERNDER) field of the Self-ID packet. This bit is initialized to 0b by GBRST#. And also, this bit enables the Phy Shadow register of the PCI configuration register space to read/write directly.
2-4	Jitter	**Jitter:** This bit indicates the difference in the maximum of Delay and the minimum time when the R5C551 repeats. Usually, return 1('001b') when read. Jitter is 40ns when the R5C551 repeats.
5-7	Power_class	**Power_class:** Power Class This field is reflected on the pwr (POWER_CLASS) field of the Self-ID packet. This field is initialized to 000b by GBRST#. And also, this bit enables the Phy Shadow register of the PCI configuration register space to read/write directly.

8.2.6 Register5

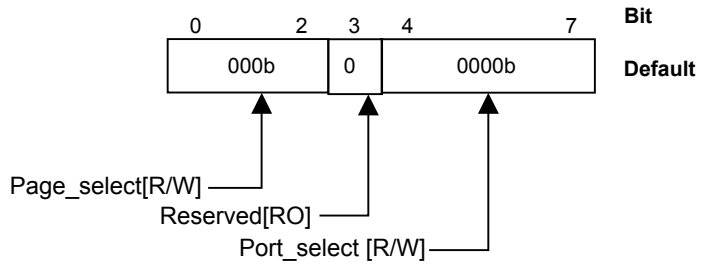
Register Name: Register5
Address Offset: 05h



Bit	Field Name	Description
0	Watchdog	**Watchdog:** Watchdog enable When this bit is set to '1', this bit controls events of loop, power fail and timeout and PME# is asserted when the Power State is the D3 state. And also, the Port_event bit is set when Port Resume happens and this bit is set to '1'.
1	ISBR	**ISBR:** Initiate Short (Arbitrated) Bus Reset Arbitrated short bus reset is started when this is set to '1'. This bit is initialized by bus reset.
2	Loop	**Loop:** Loop detect This bit indicated the bus is loop when this bit is set to '1'. This bit is cleared by GBRST# or by writing to '1'.
3	Pwr_fail	**Pwr_fail:** Cable power failure detect This bit indicates a PS bit changed in '0' from '1' when this bit is set to '1'. This bit is cleared by GBRST# or by writing to '1'.
4	Timeout	**Timeout:** Arbitration state machine timeout This bit indicates that this node didn't come beyond the MAX_ARB_STATE_TIME time out of state with Idle, the one except for T0: Tree_IDStart. This bit is cleared by GBRST# or by writing to '1'.
5	Port_event	**Port_event:** Port_event detect The R5C551 sets this bit to '1' when a change of Connected, Bias, Disabled and Fault bits is detected. And also, sets this bit to '1' when Watchdog is set to '1' and Resume happends. This bit is cleared by GBRST# or by writing to '1'.
6	Enab_accel	**Enab_accel:** Enable arbitration acceleration The R5C551 performs Ack-acceleration arbitration and Fly-by arbitration when this bit is set to '1'. The R5C551 does not perform acceleration arbitration when this bit is set to '0'. This bit is initialized by GBRST#.
7	Enab_multi	**Enab_multi:** Enable multi-speed packet concatenation The R5C551 detects transfer speed of the packet at the same time the Concatenated packet transfer is detected when this bit is set to '1'. The R5C551 performs Concatenated packet transfer at the same speed as that of the initial packet when this bit is set to '0'. This bit is initialized by GBRST#.

8.2.7 Register7

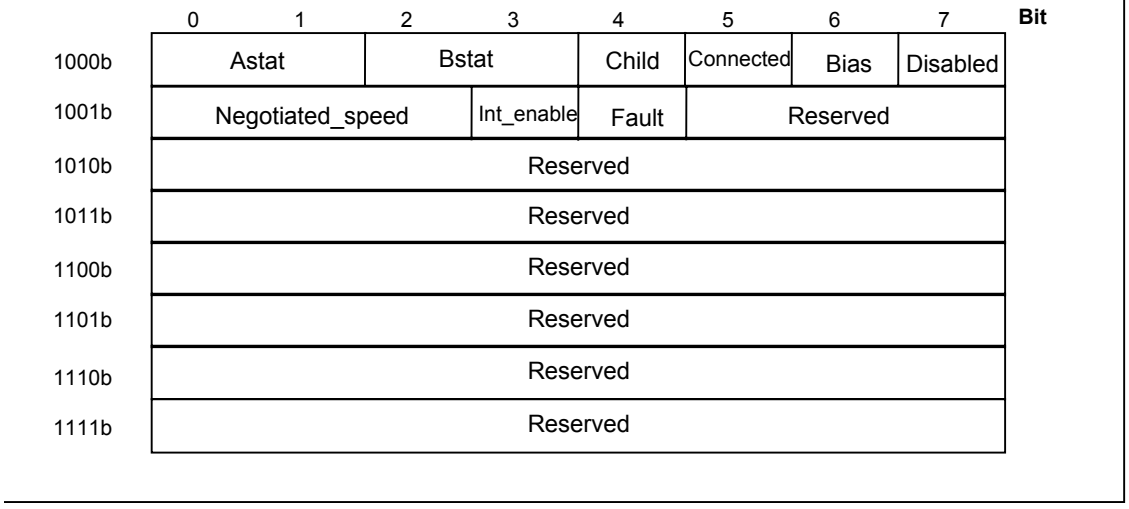
Register Name: Register7
Address Offset: 07h



Bit	Field Name	Description
0-2	Page_select	**Page_select:** This field defines what page is to be access when PHY registers 08h through 0Fh are referenced.
3	Reserved	**Reserved:**
4-7	Port_select	**Port_select:** This field determines the port whose data is accessible to PHY register 08h through 0Fh when Page_select bit selects Port Status Page.

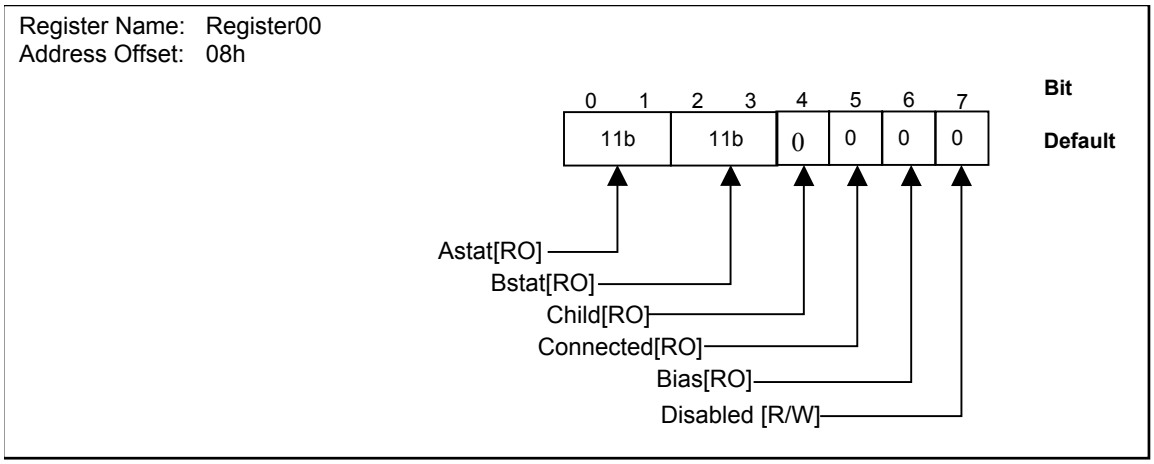
8.3 Page_select=0 (Port Status page)

This register reflects the condition of each port. The Port_select bit enables to choose a port.



8.3.1 Register00

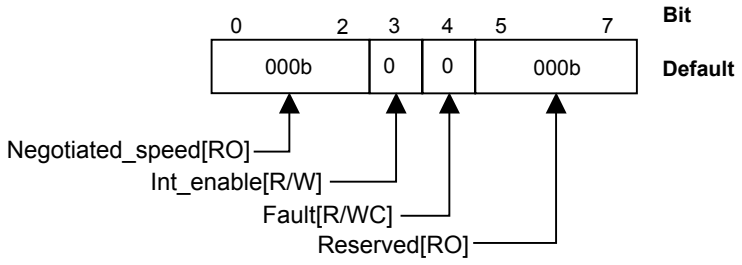
Register Name: Register00
Address Offset: 08h



Bit	Field Name	Description
0-1	Astat	**stat :** Status of TPA This bit indicates the condition of TPA. 11b Z 01b 1 10b 0 00b invalid
2-3	Bstat	**Bstat:** Status of TPB This bit indicates the condition of TPB. 11b Z 01b 1 10b 0 00b invalid
4	Child	**Child:** Child This bit indicates that the port is Child when this bit is set to '1' and it is Parent when this bit is set to '0'. This bit is initialized by bus reset, and decided during the Tree-ID period.
5	Connected	**Connected:** Connected This bit indicates that the port is connected to a peer PHY device when this bit is set to '1'.
6	Bias	**Bias:** Cable Bias This bit reflects Cable Bias detected by the port. This bit indicates the port has detected TpBias when this bit is set to '1'.
7	Disabled	**Disabled:** Port Disabled The port is Disabled state when this bit is set to '1'. This bit is initialized to '0' by GBRST#. And also, this bit enables the Phy Shadow register of the PCI configuration register space to read/write directly.

8.3.2 Register01

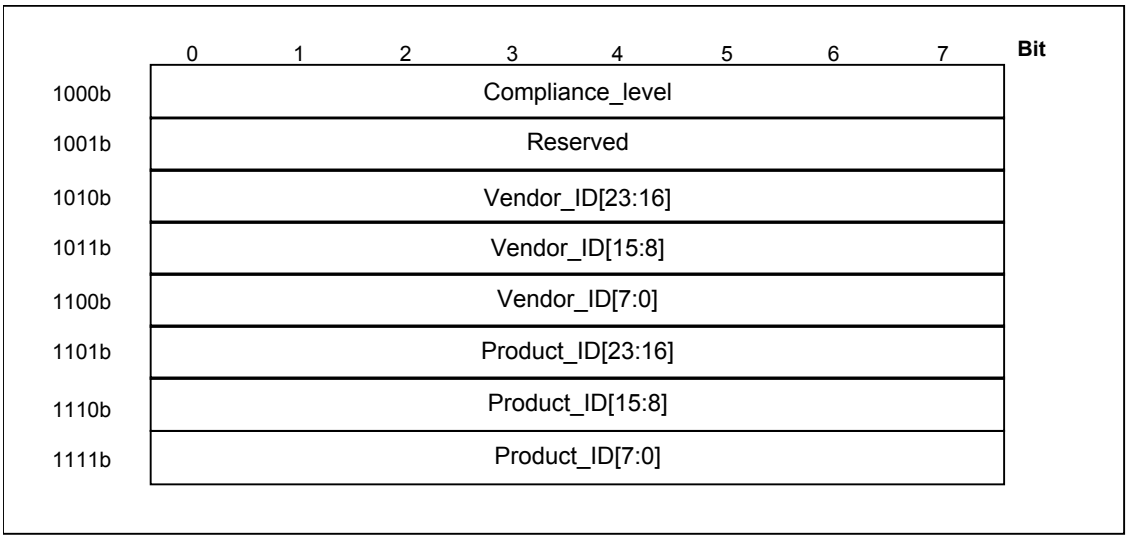
Register Name: Register01
Address Offset: 09h



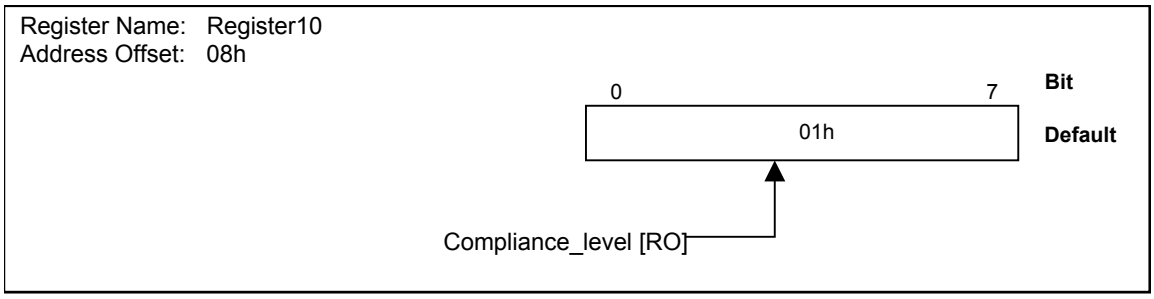
Bit	Field Name	Description
0-2	Negotiated_speed	**Negotiated_speed:** Negotiate speed This field indicates the max speed of the peer port connect to this port. This field is initialized by bus reset, and decided during the Self-ID period. 000b It indicates that the maximum transfer speed of confrontation node is 100Mbps. 001b It indicates that the maximum transfer speed of confrontation node is 200Mbps. 010b It indicates that the maximum transfer speed of confrontation node is 400Mbps.
3	Int_enable	**Int_enable:** Enable port event interrupt When the state of Connected, Bias, Disabled, Fault bits are changed while this bit is set to '1', the Port_event bit is set to '1'. This bit is initialized by GBRST#.
4	Fault	**Fault:** Fault This bit indicates an error happened during the port Suspend/Resume action. This bit is cleared by GBRST# or writing this bit to '1'.
5-7	Reserved	**Reserved:**

8.4 Page_select=1 (Vendor Identification page)

This register reflects the condition of each port. The Port_select bit enables to choose a port.



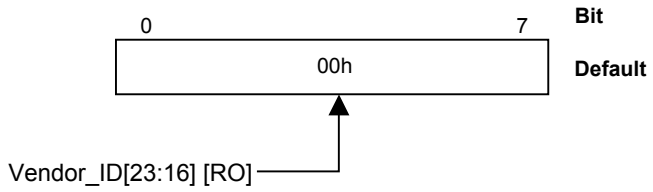
8.4.1 Register10



Bit	Field Name	Description
0-7	Compliance_level	**Compliance_level:** Return 01h when read. Writing has no effect.

8.4.2 Register12

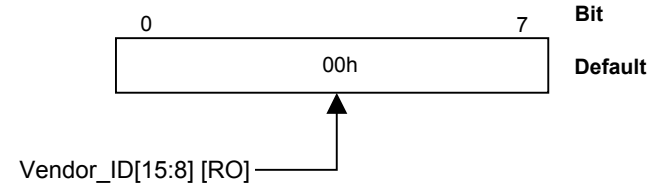
Register Name: Register12
Address Offset: 0Ah



Bit	Field Name	Description
0-7	Vendor_ID [23:16]	**Vendor_ID [23:16]:** Return '00h' when read.

8.4.3 Register13

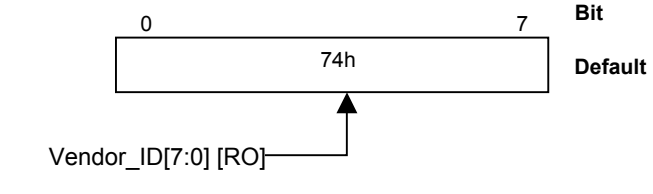
Register Name: Register13
Address Offset: 0Bh



Bit	Field Name	Description
0-7	Vendor_ID [15:8]	**Vendor_ID [15:8]:** Return '00h' when read.

8.4.4 Register14

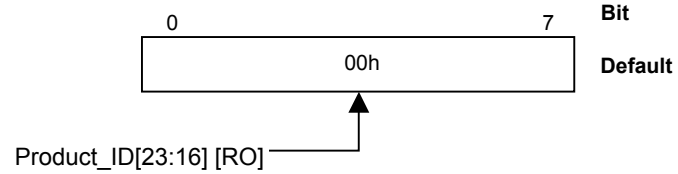
Register Name: Register14
Address Offset: 0Ch



Bit	Field Name	Description
0-7	Vendor_ID [7:0]	**Vendor_ID [7:0]:** Return '74h' when read.

8.4.5 Register15

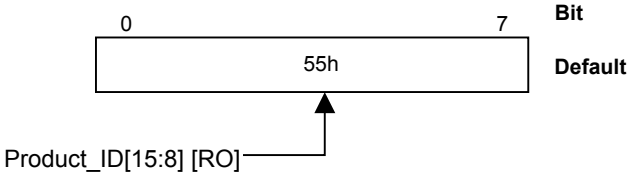
Register Name: Register15
Address Offset: 0Dh



Bit	Field Name	Description
0-7	Product_ID [23:16]	**Product_ID [23:16]:** Return '00h' when read.

8.4.6 Register16

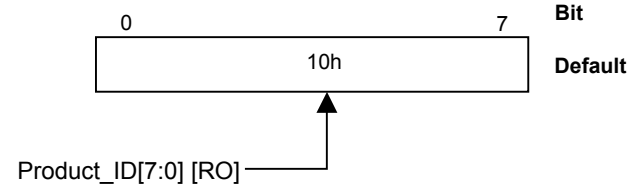
Register Name: Register16
Address Offset: 0Eh



Bit	Field Name	Description
0-7	Product_ID [15:8]	**Product_ID [15:8]:** Return '55h' when read.

8.4.7 Register17

Register Name: Register17
Address Offset: 0Fh



Bit	Field Name	Description
0-7	Product_ID [7:0]	**Product_ID [7:0]:** Return '10h' when read.

9 1394 OHCI REGISTERS

9.1 Overview

The 1394 OHCI registers include control registers, common DMA controller registers and individual DMA context registers.

9.2 Register Space

The 1394 OHCI registers occupy a 2048 byte address space, and are memory mapped into PCI memory address space and pointed to by OHCI Register Base Address register in the PCI configuration space.

9.3 Register Configuration

There are two types of registers in this OHCI register; read/write registers and set and clear registers.

9.3.1 Read/Write Register

Read/write registers are registers for which a single address is defined and for which fields may be defined with the following attributes:

Access tag (rwu)	Name	Meaning
r	read	field may be read
w	write	field may be written from PCI bus
u	update	field may be autonomously updated by hardware

9.3.2 Set/Clear Register

Set and Clear registers have the property of having two addresses by which they may be referenced by the host. When the host writes to the Set address the value written is taken as a bit mask indicating which bits in the register are to be set to one. A one bit in the value written indicates that the corresponding bit in the register is to be set to one, while a zero bit indicates that the corresponding bit in the register is not to be changed. Similarly, host writes to the Clear address specify a value that is a bit mask of bits to clear to zero in the register, a one bit means to clear the corresponding bit while a zero bit means to leave the corresponding bit unchanged.

Access tag (rscu)	Name	Meaning
r	read	field may be read
s	set	field may be set from PCI bus
c	clear	field may be cleared from PCI bus
u	update	field may be autonomously updated by hardware

9.3.3 OHCI 1.0/1.1 support

The R5C551 support the OHCI 1.0/1.1. Setting bit 7 of the Misc Control 5 register (the 1394 PCI Config.addr.81h) enables the R5C551 to switch a supporting version. If each bit of the OHCI register version1.0 or 1.1 has different function, each release is marked on the field name as follows.

*v1.0: OHCI Release 1.0
*v1.1: OHCI Release 1.1

9.3.4 Register Map

1394 OHCI Register addresses

Offset	DMA Context	Read value	Write value
000h		Version	-
004h		GUID_ROM	GUID_ROM
008h		ATRetries	ATRetries
00Ch		CSRReadData	CSRWriteData
010h		CSRCompareData	CSRCompareData
014h		CSRControl	CSRControl
018h		ConfigROMhdr	ConfigROMhdr
01Ch		BusID	-
020h		BusOptions	BusOptions
024h		GUIDHi	GUIDHi
028h		GUIDLo	GUIDLo
02Ch		*Reserved*	*Reserved*
030h		*Reserved*	*Reserved*
034h		ConfigROMmap	ConfigROMmap
038h		PostedWriteAddressLo	PostedWriteAddressLo
03Ch		PostedWriteAddressHi	PostedWriteAddressHi
040h		VendorID	-
044h~04Ch		*Reserved*	*Reserved*
050h		HCControl	HCControlSet
054h			HCControlClear
058h~05Ch		*Reserved*	*Reserved*
060h	Self ID	*Reserved*	*Reserved*
064h		SelfIDBuffer	SelfIDBuffer
068h		SelfIDCount	-
06Ch		*Reserved*	*Reserved*
070h		IRChanMaskHi	IRChanMaskHiSet
074h			IRChanMaskHiClear
078h		IRChanMaskLo	IRChanMaskLoSet
07Ch			IRChanMaskLoClear
080h		IntEvent	IntEventSet
084h		(IntEvent & IntMask)	IntEventClear
088h		IntMask	IntMaskSet
08Ch			IntMaskClear
090h		IsoXmitIntEvent	IsoXmitIntEventSet
094h		(IsoXmitIntEvent & IsoXmitIntMask)	IsoXmitIntEventClear
098h		IsoXmitIntMask	IsoXmitIntMaskSet
09Ch			IsoXmitIntMaskClear
0A0h		IsoRecvIntEvent	IsoRecvIntEventSet
0A4h		(IsoRecvIntEvent & IsoRecvIntMask)	IsoRecvIntEventClear
0A8h		IsoRecvIntMask	IsoRecvIntMaskSet
0ACh			IsoRecvIntMaskClear

Offset	DMA Context	Read value	Write value
0B0h		Initial Bandwidth Available	Initial Bandwidth Available
0B4h		Initial Channels Available Hi	Initial Channels Available Hi
0B8h		Initial Channels Available Lo	Initial Channels Available Lo
0BCh~0D8h		*Reserved*	*Reserved*
0DCh		FairnessControl	FairnessControl
0E0h		LinkControl	LinkControlSet
0E4h			LinkControlClear
0E8h		NodeID	NodeID
0ECh		PhyControl	PhyControl
0F0h		IsoCycleTimer	IsoCycleTimer
0F4h~0FCh		*Reserved*	*Reserved*
100h		AsynReqFilterHi	AsynReqFilterHiSet
104h			AsynReqFilterHiClear
108h		AsynReqFilterLo	AsynReqFilterLoSet
10Ch			AsynReqFilterLoClear
110h		PhyReqFilterHi	PhyReqFilterHiSet
114h			PhyReqFilterHiClear
118h		PhyReqFilterLo	PhyReqFilterLoSet
11Ch			PhyReqFilterLoClear
120h		PhyUpperBound	-
124h~17Ch		*Reserved*	*Reserved*
180h	Asynchronous Request Transmit	ContextControl	ContextControlSet
184h			ContextControlClear
188h		*Reserved*	*Reserved*
18Ch		CommandPtr	CommandPtr
190h~19Ch		*Reserved*	*Reserved*
1A0h	Asynchronous Response Transmit	ContextControl	ContextControlSet
1A4h			ContextControlClear
1A8h		*Reserved*	*Reserved*
1ACh		CommandPtr	CommandPtr
1B0h~1BFh		*Reserved*	*Reserved*
1C0h	Asynchronous Request Receive	ContextControl	ContextControlSet
1C4h			ContextControlClear
1C8h		*Reserved*	*Reserved*
1CCh		CommandPtr	CommandPtr
1D0h~1DFh		*Reserved*	*Reserved*
1E0h	Asynchronous Response Receive	ContextControl	ContextControlSet
1E4h			ContextControlClear
1E8h		*Reserved*	*Reserved*
1ECh		CommandPtr	CommandPtr
1F0h~1FFh		*Reserved*	*Reserved*
200h+16*n	Isochronous Transmit context n, (n=0,1,2,3)	ContextControl	ContextControlSet
204h+16*n			ContextControlClear
208h+16*n		*Reserved*	*Reserved*
20Ch+16*n		CommandPtr	CommandPtr

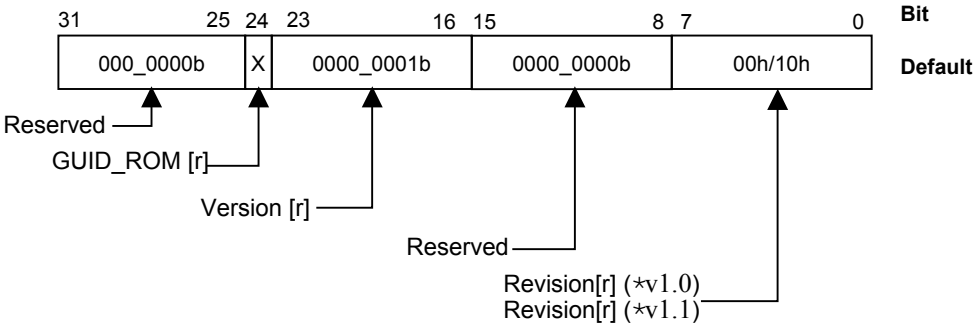
Offset	DMA Context	Read value	Write value
400h+32*n	Isochronous Receive context n, (n=0,1,2,3)	ContextControl	ContextControlSet
404h+32*n			ContextControlClear
408h+32*n		*Reserved*	*Reserved*
40Ch+32*n		CommandPtr	CommandPtr
410h+32*n		ContextMatch	ContextMatch
414h+32*n		*Reserved*	*Reserved*
418h+32*n		*Reserved*	*Reserved*
41Ch+32*n		*Reserved*	*Reserved*

9.4 Register Description

9.4.1 Version Register

This register contains a 32-bit value that indicates the version and capabilities of the interface. The register is used to indicate the level of functionality present in the 1394 OHCI. This register is read only.

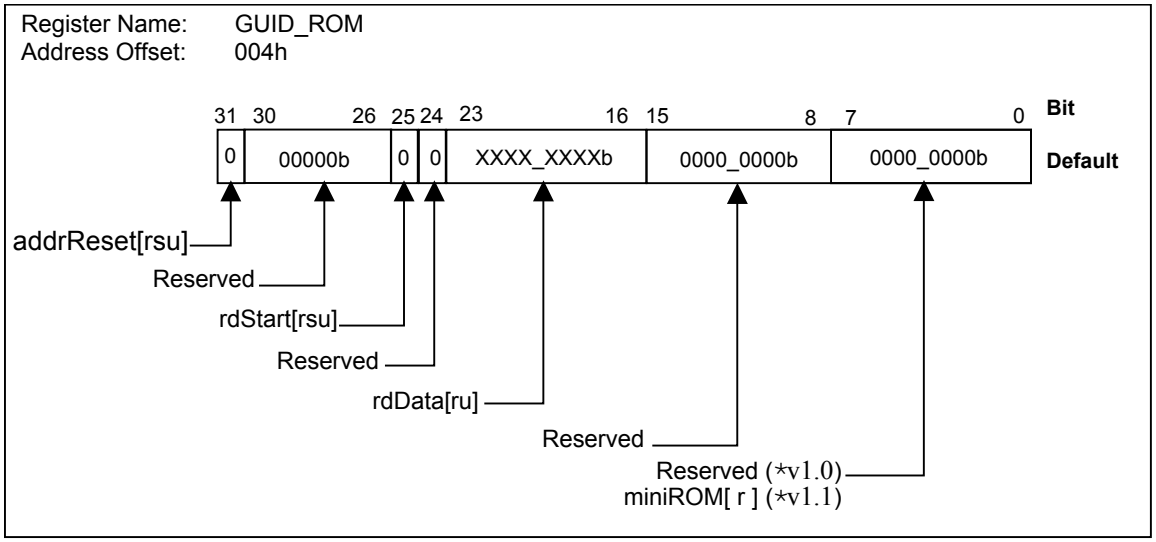
Register Name: Version
Address Offset: 000h



Bit	Field Name	Description
31-25	Reserved	This field is read-only and hardwired to zeros. Writing to this field has no effect.
24	GUID_ROM	This bit returns '1' when the serial ROM is detected. Moreover, the third and fourth quadlets of the bus_info_block are automatically loaded by PCIRST#.
23-16	Version	Major version of the OHCI. This field contains the BCD encoded value representing the major version of the highest numbered 1394 OHCI specification. The R5C551 implements to the 1394 OHCI Release 1.00, then have a version value of 01h.
15-8	Reserved	This field is read-only and hardwired to zeros. Writing to this field has no effect.
7-0	Revision (*v1.0)	Minor version of the OHCI. This field contains the BCD encoded value representing the minor version of the highest numbered 1394 OHCI specification. The R5C551 implements to the 1394 OHCI Release 1.00, then have a version value of 00h.
	Revision (*v1.1)	Minor version of the OHCI. This field contains the BCD encoded value representing the minor version of the highest numbered 1394 OHCI specification. The R5C551 implements to the 1394 OHCI Release 1.10, then have a version value of 10h.

9.4.2 GUID ROM Register

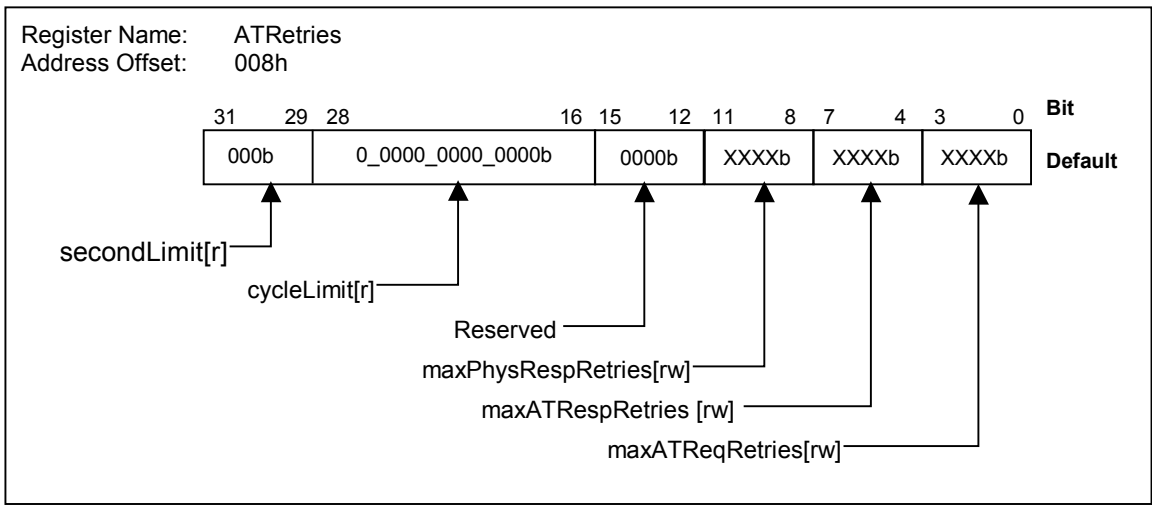
The GUID_ROM register is used to access the GUID_ROM, and is only present if the Version.GUID_ROM bit is set. To initialize the GUID_ROM read address, software sets GUIDROM.addrReset to one. Once software detects that GUIDROM.addrReset is zero, indicating that the reset has completed, and then software may set GUIDROM.rdStart to read a byte. Upon the completion of each read, the R5C551 places the read byte into GUIDROM.rdData, advances the GUID_ ROM address by one byte to set up for the next read, and clears GUIDROM.rdStart to 0 to indicate to software that the requested byte has been read.



Bit	Field Name	Description
31	addrReset	Software sets this bit to one in order to reset the GUID ROM address to 00h. When the R5C551 completes the reset, it clears addrReset to zero. Upon resetting the GUID ROM address, R5C551 does not automatically fill rdData with the data from byte address 00h.
30-26	Reserved	This field is read-only and hardwired to zeros. Writing to this field has no effect.
25	rdStart	A read of the currently addressed GUID ROM byte is started on the transition of this bit from a zero to a one. When R5C551 completes the read, it clears rdStart to zero and advances the GUID ROM byte address by one byte.
24	Reserved	This bit is read-only and hardwired to zeros. Writing to this bit has no effect.
23-16	rdData	The data read from the GUID ROM.
15-8	Reserved	This field is read-only and hardwired to zeros. Writing to this field has no effect.
7-0	Reserved (*v1.0)	This field is read-only and hardwired to zeros. Writing to this field has no effect.
	miniROM (*v1.1)	The Host Controller indicates the first byte location of the miniROM image in the GUID_ROM through this field. The Host Controller read the data of the serial ROM (address 27h), if supports the miniROM. Using the serial ROM enables to change the default value of this bit. Details see the Serialized ROM in Chapter 4.

9.4.3 Asynchronous Transmit Retries Register

The AT retries register holds the number of times the 1394 OHCI will attempt to do a retry for asynchronous request and response transmit and for physical response transmit. On the OHCI 1.0 mode, a packet may be retried only when a “busy” acknowledge or ack_data_error is received from the target node, including ack_data_error’s resulting from FIFO underflows. On the OHCI 1.1 mode, a packet may be retried only when a “busy” acknowledge is received. A packet shall not be retried under any other circumstance, including receipt of evt_missing_ack.

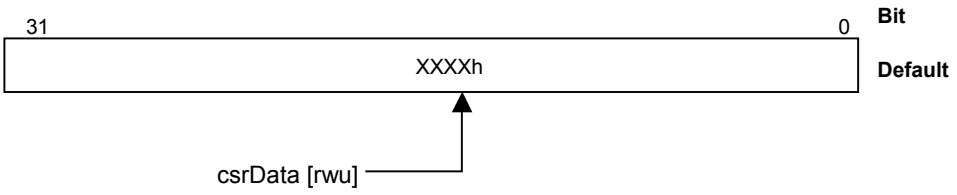


Bit	Field Name	Description
31-29	SecondLimit	Together the secondLimit and cycleLimit fields define a time limit for retry attempts when the outbound dual-phase retry protocol is in use. R5C551 is hardwired to zeros because R5C551 does not support the dual-phase retry.
28-16	cycleLimit	
15-12	Reserved	This field is read-only and hardwired to zeros. Writing to this field has no effect
11-8	maxPhysRespRetries	This field tells the Physical Response Unit how many times to attempt to retry the transmit operation for the response packet. Note that this value is used only for responses to physical requests. If the retry count expires for a physical response, the packet is discarded by R5C551. Software is not notified.
7-4	maxATRespRetries	This field tells the Asynchronous Transmit Response Unit how many times to attempt to retry the transmit operation for a software transmitted (non-physical) asynchronous response packet.
3-0	maxATReqRetries	This field tells the Asynchronous Transmit Request Unit how many times to attempt to retry the transmit operation for an asynchronous request packet.

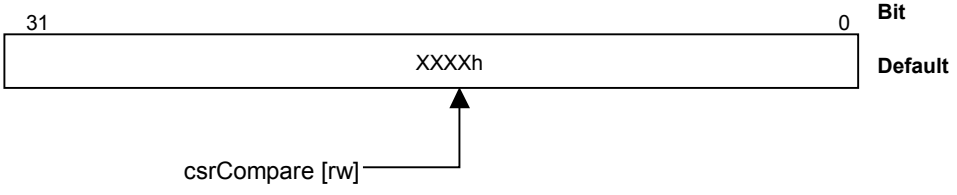
9.4.4 Bus Management CSR Register

1394 requires certain 1394 bus management resource registers be accessible only via "quadlet read" and “quadlet lock" (compare-and-swap) transactions, otherwise ack_type_error shall be sent. When these bus management resource registers are accessed from the 1394 bus, the atomic compare-and-swap transaction is autonomous, without software intervention. If ack_complete is not received to end the transaction for the generated lock response, IntEvent.lockRespErr shall be triggered.
To access these bus management resource registers from PCI bus, first load the CSRData register with the new data value to be loaded into the appropriate resource. Then load the CSRCompare register with the expected value. Finally, write the CSRControl register with the selector value of the resource. A write to the CSRControl register initiates a compare-and-swap operation on the selected resource. When the compare-and-swap operation is complete, the CSRControl register csrDone bit will be set, and the CSRData register will contain the value of the selected resource prior to the host initiated compare-and-swap operation. On the OHCI 1.1, the csrControl register isn’t affected by a write access when the 1394 bus reset is generated and the IntEvent.busReset is set to one.

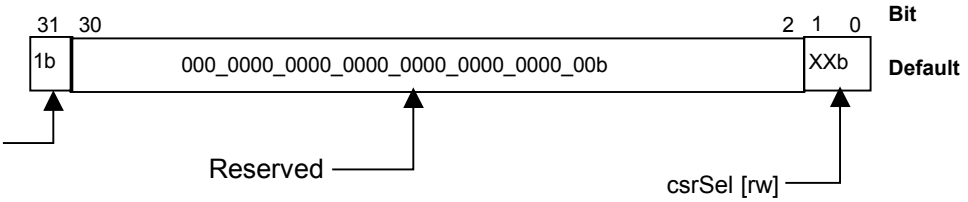
Register Name: csrData
Address Offset: 00Ch



Register Name: csrCompare
Address Offset: 010h



Register Name: csrControl
Address Offset: 014h

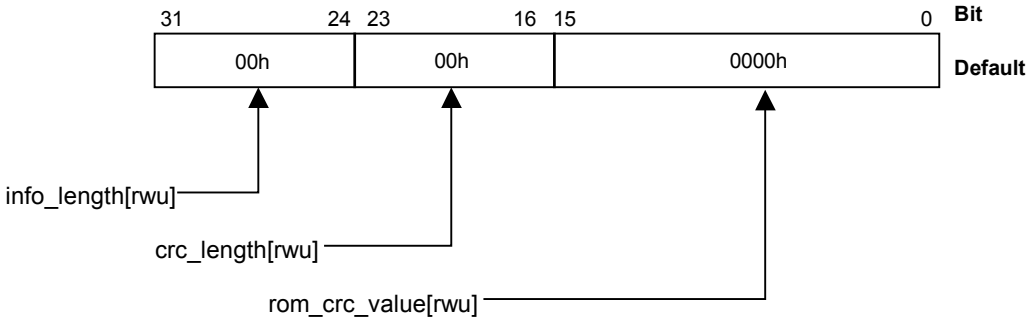


Bit	Field Name	Description
31-0	csrData	At start of operation, the data to be stored if the compare is successful.
31-0	csrCompare	The data to be compared with the existing value of the CSR resource.
31	csrDone	This bit is set when a compare-swap operation is completed. It is reset whenever this register is written.
30-2	Reserved	This field is read-only and hardwired to zeros. Writing to this field has no effect
1-0	csrSel	This field selects the CSR resource: 00b - BUS_MANAGER_ID 01b - BANDWIDTH_AVAILABLE 10b - CHANNELS_AVAILABLE_HI 11b - CHANNELS_AVAILABLE_LO

9.4.5 Config ROM Header Register

The config ROM header register is a 32-bit number that externally maps to the first quadlet of the 1394 configuration ROM (offset 48'hFFFF_F000_0400). This register is written locally at the following register (the field names match the IEEE1394 names).
Software must ensure that the Config ROM header register is valid whenever the HCControl.link Enable bit is set. After a value of theConfig ROM map register is changed, the R5C551 updates the value of this register while the HCControl.linkEnable bit is set. And, the value of this register is loaded from the serial ROM. Details of the renewal see the Configuration ROM Mapping register in Chapter 8, and details of the mapped serial ROM see the Serialized ROM in Chapter 4.

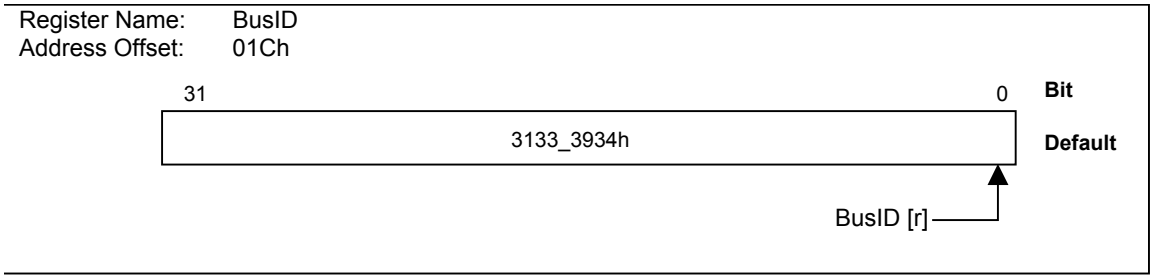
Register Name: ConfigROMhdr
Address Offset: 018h



Bit	Field Name	Description
31-24	info_length	IEEE 1394 bus management field. Must be valid at any time the HCControl.linkEnable bit is set.
23-16	crc_length	IEEE 1394 bus management field. Must be valid at any time the HCControl.linkEnable bit is set.
15-0	rom_crc_value	IEEE 1394 bus management field. Must be valid at any time the HCControl.linkEnable bit is set.

9.4.6 Bus Identification Register

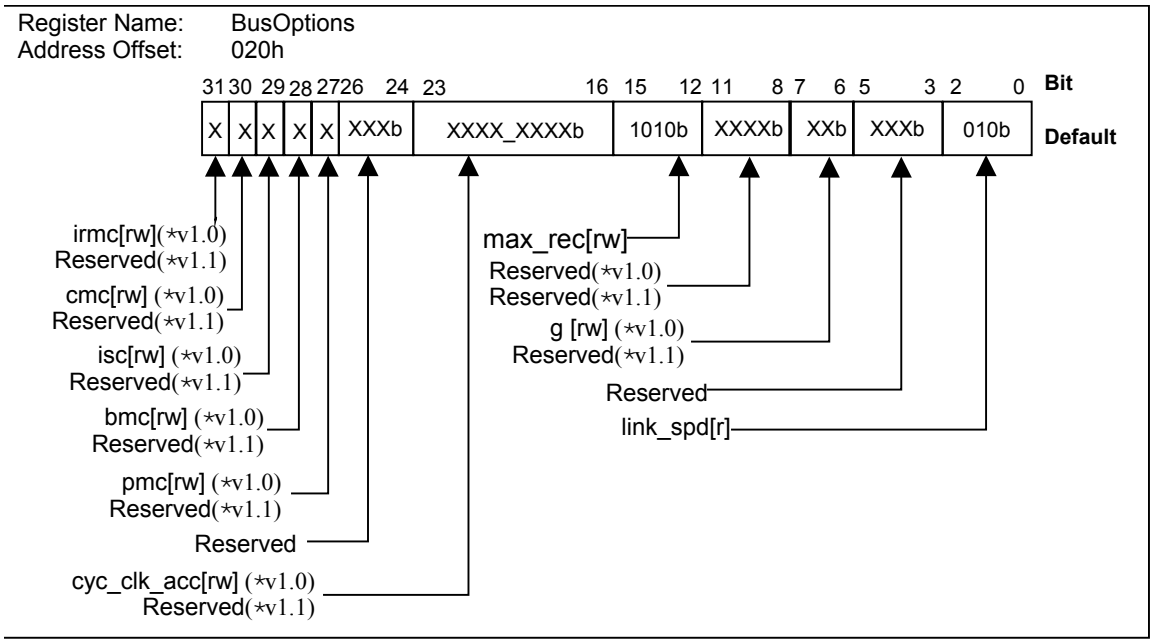
The bus identification register is a 32-bit number that externally maps to the first quadlet of the Bus_Info_Block. This register is read locally at the following register:



Bit	Field Name	Description
31-0	busID	Contains the constant 32'h31333934, which is the ASCII value for "1394".

9.4.7 Bus Options Register

The bus options register is a 32-bit number that externally maps to the second quadlet of the Bus_Info_Block. This register is written locally at the following register (the field names match the IEEE 1394 names).
Software must ensure that the Config ROM header register is valid whenever the HCControl.link Enable bit is set. After a value of theConfig ROM map register is changed, the R5C551 updates the value of this register while the HCControl.linkEnable bit is set. And, the value of this register is loaded from the serial ROM. Details of the renewal see the Configuration ROM Mapping register in Chapter 8, and details of the mapped serial ROM see the Serialized ROM in Chapter 4.



Bit	Field Name	Description
31	irmc (*v1.0)	Isochronous Resource Manager Capable: IEEE 1394 bus management bit.
	Reserved (*v1.1)	This bit is read/write and hardwired to zeros. Writing to this bit has no effect to the R5C551.
30	cmc (*v1.0)	Cycle Master Capable: IEEE 1394 bus management bit.
	Reserved (*v1.1)	This bit is read/write and hardwired to zeros. Writing to this bit has no effect to the R5C551.
29	isc (*v1.0)	Isochronous Support Capable: IEEE 1394 bus management bit.
	Reserved (*v1.1)	This bit is read/write and hardwired to zeros. Writing to this bit has no effect to the R5C551.
28	bmc (*v1.0)	Bus Manager Capable: IEEE 1394 bus management bit.
	Reserved (*v1.1)	This bit is read/write and hardwired to zeros. Writing to this bit has no effect to the R5C551.
27	pmc (*v1.0)	Power Manager Capable: IEEE 1394 bus management bit.
	Reserved (*v1.1)	This bit is read/write and hardwired to zeros. Writing to this bit has no effect to the R5C551.
26-24	Reserved	This field is reserved for future use and read/write.
23-16	cyc_clk_acc (*v1.0)	Cycle Master Clock Accuracy: IEEE 1394 bus management field.
	Reserved (*v1.1)	This field is read/write and hardwired to zeros. Writing to this field has no effect to the R5C551.
15-12	max_rec	IEEE 1394 bus management field. Hardware shall initialize max_rec to the maximum value supported by R5C551. Software may change max_rec, however this field must be valid at any time the HCControl.linkEnable bit is set to 1. Note that received block write request packets with a length greater than max_rec shall generate an ack_type_error if the request is not handled by the physical response unit, and may generate an ack_type_error otherwise. For a soft reset, max_rec is not changed.
11-8	Reserved (*v1.0)	This field is reserved for future use and read/write.
	Reserved (*v1.1)	This field is read/write and hardwired to zeros. Writing to this field has no effect to the R5C551.
7-6	g (*v1.0)	Generation counter. This field shall be incremented if any portion of configuration ROM has changed since the prior bus reset.
	Reserved (*v1.1)	This field is read/write and hardwired to zeros. Writing to this field has no effect to the R5C551.
5-3	Reserved	This field is reserved for future use and read/write.
2-0	link_spd	This field indicates the maximum speed the link can send and receive and returns 010b.

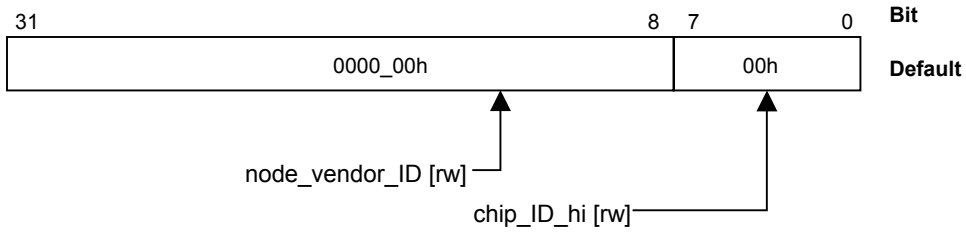
9.4.8 Global Unique ID Register

The global unique ID (GUID) is a 64-bit number that externally maps to the third and fourth quadlet of the Bus_Info_Block. These registers are written locally at the following registers.
The Global Unique ID (GUID) Registers are reset to 0 (illegal value) after GBRST#. These registers are not affected by software reset. These GUID registers shall be written only once after GBRST#, by either

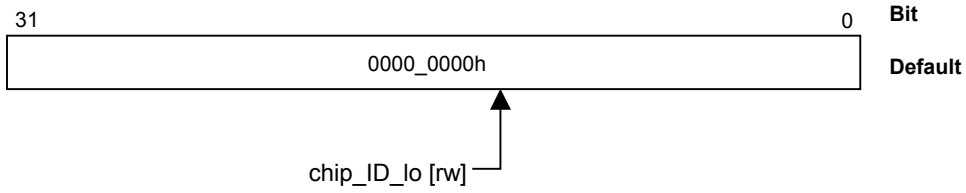
1) Data is read from the serial ROM on use of the serial ROM (SPKROUT is pull-down by an external resistor), or
2) A single host writes to each register performed only by firmware that is always executed on GBRST#. This firmware, as well as the GUID value that is loaded, may not be modifiable by any user action.

After one of these load mechanisms has executed, the GUID registers are read-only.

Register Name: GUIDHi
Address Offset: 024h



Register Name: GUIDLo
Address Offset: 028h



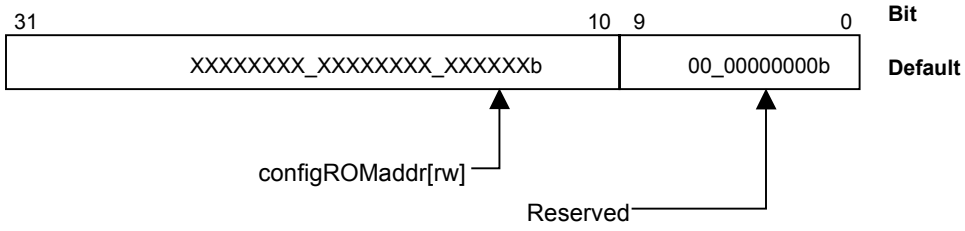
Bit	Field Name	Description
31-8	node_vendor_ID	IEEE 1394 bus management fields. Must be set by firmware or hardware before the HCControl.linkEnable bit is set.
7-0	chip_ID_hi	
31-0	chip_ID_lo	

9.4.9 Configuration ROM Mapping register

The configuration ROM mapping register contains the start address within system bus space that will map to the start address of the 1394 configuration ROM for this node. Only quadlet read corresponding to the first 1K bytes of the configuration ROM is mapped to system bus space, all other transactions to this space is rejected with a 1394 “ack_type_error”. Since the low order 10 bits of this address are reserved and assumed to be zero, the system address for the config ROM must start on a 1K byte boundary. Note that the first five quadlets of the 1394 config ROM space are mapped to the config ROM header and the bus_info_block, and so are handled directly by R5C551. This means that the first five quadlets addressed by the config ROM mapping register are not used.
Software should ensure this address is valid before setting HCControl.linkEnable to one.
On the default of the OHCI1.0/1.1, Access to the config ROM space is done by the quadlet read. Another access except the quadlet read request is returned “ack_type_error”. On the OHCI1.1, setting the HCControl.BIBimageValid bit enables to accede by the block read request.
The following procedure enables to update the config ROM when the BIBimageValid bit is set.

a) Get the data of the bus_info_block on the R5C551, and prepare the new cofig ROM.
b) Write the start address of the new config ROM into the configROMmap register.
c) Be occurred the bus reset. After that, the R5C551 automatically updates the configROMmap register, also the configROMheader register and the Bus Option register are updated.

Register Name: ConfigROMmap
Address Offset: 034h



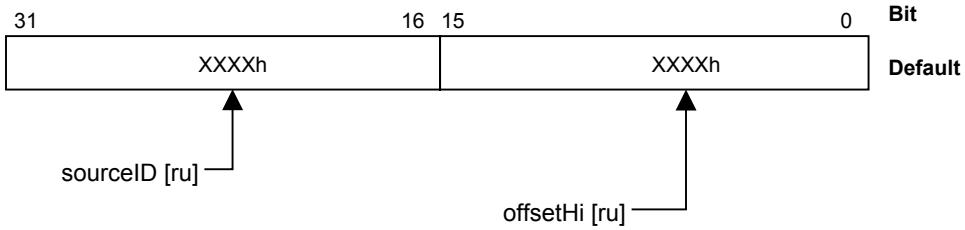
Bit	Field Name	Description
31-10	conifgROMaddr	If a quadlet read request to 1394 offset 48’hFFFF_F000_0400 through offset 48’FFFF_F000_07FF is received, then the low order 10 bits of the offset are added to this register to determine the host memory address of the returned quadlet.
9-0	Reserved	This field is read-only and hardwired to zeros. Writing to this field has no effect

9.4.10 PostedWriteAddress Register

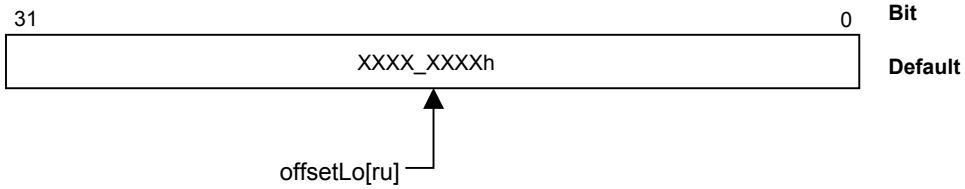
The PostedWriteAddress register is a 64-bit register, which indicates the bus, and node numbers (source ID) have the node that issued the write that failed, and the address that node attempted to access. The IntEvent.PostedWriteErr bit allows hardware to generate an interrupt when a write fails.

On the OHCI 1.0, this register is valid to the Physical Posted Write packet and the Asynch Posted Write packet. On the OHCI 1.1, this register is valid to only the Physical Posted Write packet.

Register Name: PostedWriteAddressHi
Address Offset: 03Ch



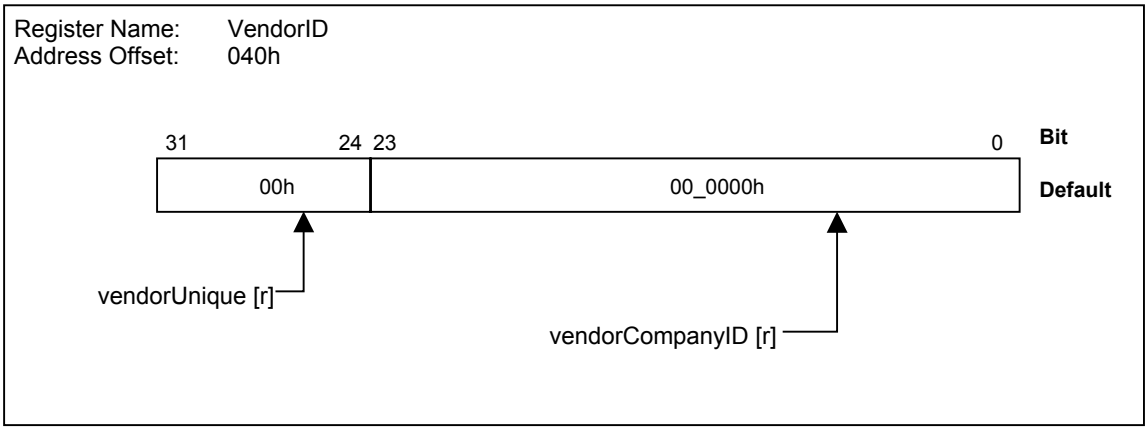
Register Name: PostedWriteAddressLo
Address Offset: 038h



Bit	Field Name	Description
Hi 31-16	sourceID	The busNumber and nodeNumber of the node that issued the write request that failed.
Hi 15-0	offsetHi	The upper 16-bits of the 1394 destination offset of the write request that failed.
Lo 31-0	offsetLo	The low 32-bits of the 1394 destination offset of the write request that failed.

9.4.11 Vendor ID Register

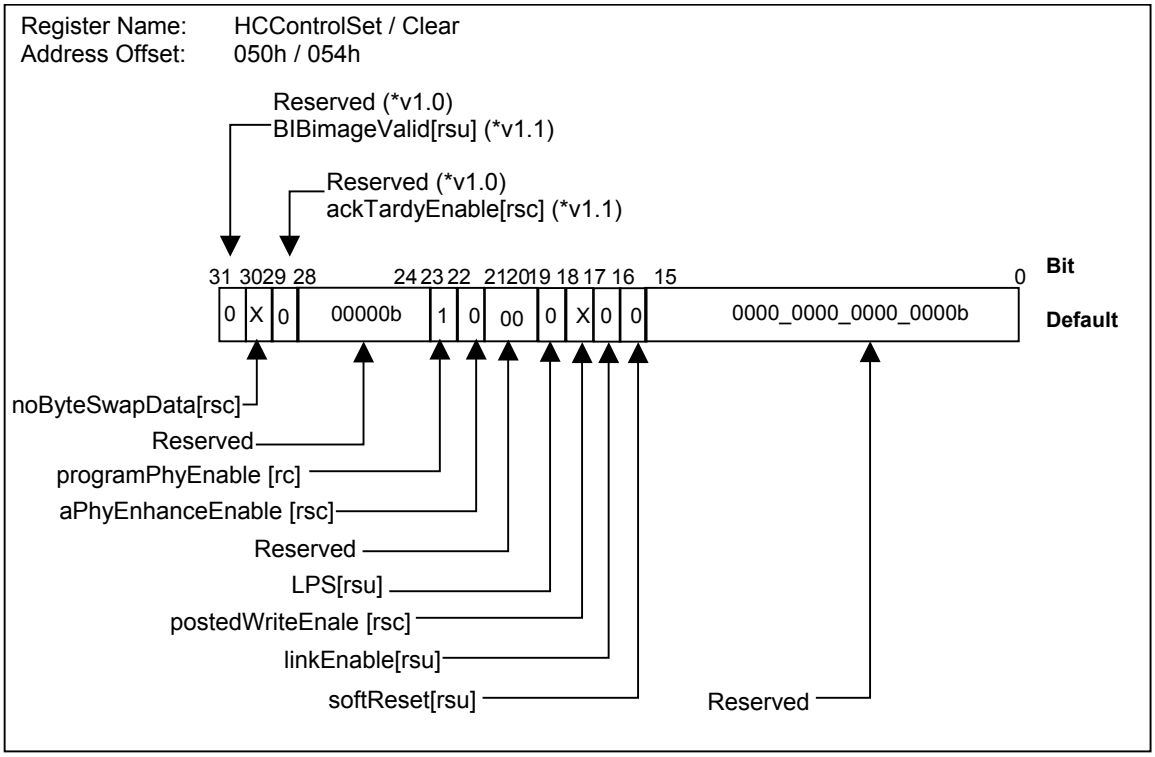
The vendor ID register holds the company ID of an organization that specified any vendor-unique registers.



Bit	Field Name	Description
31-24	vendorUnique	No additional features are implemented. Thus this field shall be 32'h0.
23-0	vendorCompanyID	

9.4.12 Host Controller Control Registers (set and clear)

This register provides flags for controlling R5C551. There are two addresses for this register: HCControlSet and HCControlClear. On read, both addresses return the contents of the control register. For writes, the two addresses have different behavior: a one bit written to HCControlSet causes the corresponding bit in the HCControl register to be set, while a zero bit leaves the corresponding bit in the HCControl register unaffected. On the other hand, a one bit written to HCControlClear causes the corresponding bit in the HCControl register to be cleared, while a zero bit leaves the corresponding bit in the HCControl register unaffected.

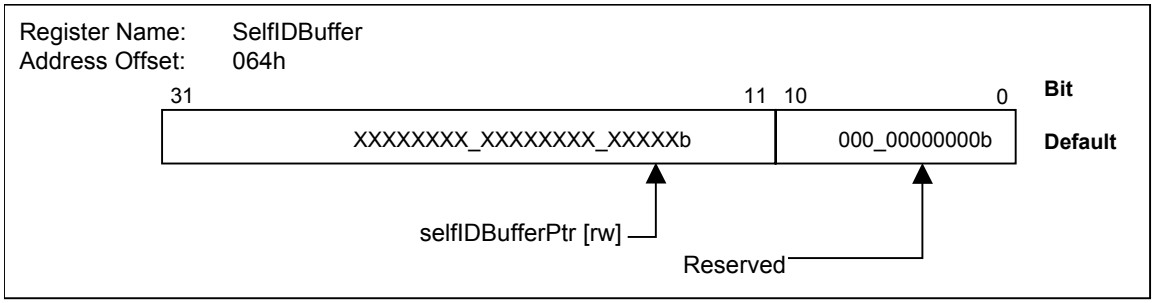


Bit	Field Name	Description
31	Reserved (*v1.0)	This bit is reserved for future use and read-only.
	BIBimageValid (*v1.1)	When this bit is set to one, the block read request to the config ROM is valid. And also, the data of the config ROM is updated automatically when the 1394 bus reset is occurred. Software must set the bus_info_block in the configuration ROM of host memory to a valid value before setting this bit. When this bit is set to zero, the block read request to the config ROM is invalid and returned the ack_type_error. And also, the configROMmap, the configROMheader and the Bus Option registers are not updated when the 1394 bus reset is occurred. Software can set this bit only when the HCControl.linkEnable is zero. Once set, this bit is cleared by hardware reset, a soft reset or a fetch error occurs when the R5C551 loads the bus_info_block from host memory.
30	noByteSwapData	This bit is used to control whether physical accesses to locations outside R5C551 itself as well as any other DMA data accesses should be swapped or not. When 0, data quadlet is sent/received in little endian order. When 1, data quadlets are sent/received in big endian order. Software should change this bit only when linkEnable is 0.

Bit	Field Name	Description
29	Reserved (*v1.0)	This bit is reserved for future use and read-only.
	ackTardyEnable (*v1.1)	When this bit is set to one, ack_tardy is returned as an acknowledgment to all asynchronous packets. IntEvent.ack_tardy is set when the host controller sends ack_tardy. Software is not set this bit when the node is the 1394 bus manager.
28-24	Reserved	This field is reserved for future use and read-only.
23	programPhyEnable	This bit informs upper-level generic software (e.g., OHCI device driver) if lower-level implementation specific software (e.g., BIOS) has consistently configured IEEE1394a-2000 enhancements in the Link and PHY. When 1 and while linkEnable is 0, generic software is responsible for configuring the IEEE1394a-2000 enhancements within the PHY and the aPhyEnhanceEnable bit within R5C551 Link in a consistent manner. When 0, generic software may not modify the IEEE1394a-2000 enhancement configuration in either the Link or PHY and cannot interpret the setting of aPhyEnhanceEnable. A soft reset and a bus reset shall not affect this bit. Using the serial ROM enables to change the default value of this bit. Details see the Serialized ROM in Chapter 4.
22	aPhyEnhanceEnable	When the programPhyEnable bit is 1, this bit is used by generic, implementation independent software (e.g., OHCI device driver) to enable R5C551 Link to use all of IEEE1394a-2000 enhancements. Generic software can only modify this bit when the programPhyEnable bit is 1 and the linkEnable bit is 0. This bit is meaningless to software when the programPhyEnable bit is 0. When 0, none of the IEEE1394a-2000 enhancements are enabled within the Link. When 1, the set of all IEEE1394a-2000 enhancements is enabled within the Link. A soft reset and a bus reset shall not affect this bit. Using the serial ROM enables to change the default value of this bit. Details see the Serialized ROM in Chapter 4.
21-20	Reserved	This field is read-only and hardwired to zeros. Writing to this field has no effect
19	LPS	This bit is used to control the Link Power Status. Software must set LPS to 1 to permit Link-PHY communication. Once set, the link can use LREQs to perform PHY reads and writes. An LPS value of 0 prevents Link-PHY communication.
18	posteddWriteEnable	This bit is used to enable (1) or disable (0) physical posted writes. When disabled physical writes shall be handled but shall not be posted and instead are ack'ed with ack_pending. Software should change this bit only when linkEnable is 0.
17	linkEnable	Software must set this bit to 1 when the system is ready to begin operation and then force a bus reset. This bit is necessary to keep other nodes from sending transactions before the local system is ready. When this bit is clear R5C551 is logically and immediately disconnected from the 1394 bus. The link shall not process or interpret any packets received from the PHY, nor shall the link generate any *bus* requests. However, the link may access PHY registers via the PHY control register.
16	softReset	When set to 1, all 1394 state is reset, all FIFO's are flushed and all OHCI registers except some registers are set to their hardware reset values unless otherwise specified. Registers outside of the OHCI realm, i.e., registers for PCI or CardBus, are not affected. The read value of this bit is 1 while a soft reset or a hard reset is in progress. The read value of this bit is 0 when neither a soft reset nor hard reset are in progress. Software can use the value of this bit to determine when a reset has completed and R5C551 is safe to operate.
15-0	Reserved	This field is read-only and hardwired to zeros. Writing to this field has no effect

9.4.13 Self ID Buffer Pointer Register

This register indicates the buffer the SelfID packets will be DMA'ed into during the bus initialization.

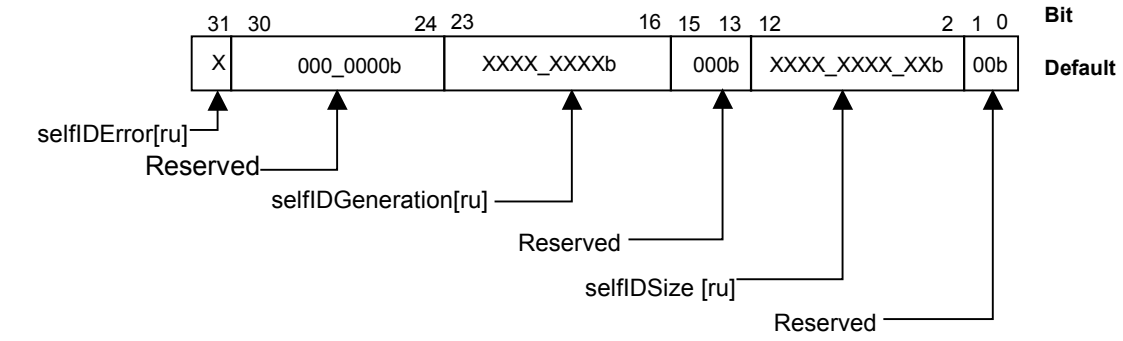


Bit	Field Name	Description
31-11	selfIDBufferPtr	Contains the 2K-byte aligned base address of the buffer in host memory where received self-ID packets are stored. The contents of this field are undefined after a chip reset.
10-0	Reserved	This field is read-only and hardwired to zeros. Writing to this field has no effect

9.4.14 Self ID Count Register

This register keeps a count of the number of times the bus self ID process has occurred, flags self ID packet errors and keeps a count of the amount of self ID data in the Self ID buffer.

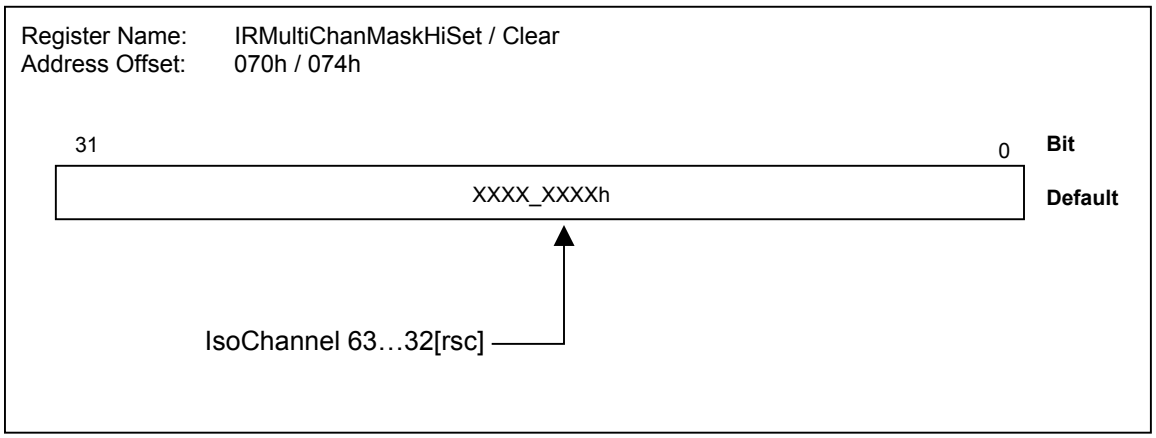
Register Name: SelfIDCount
Address Offset: 068h

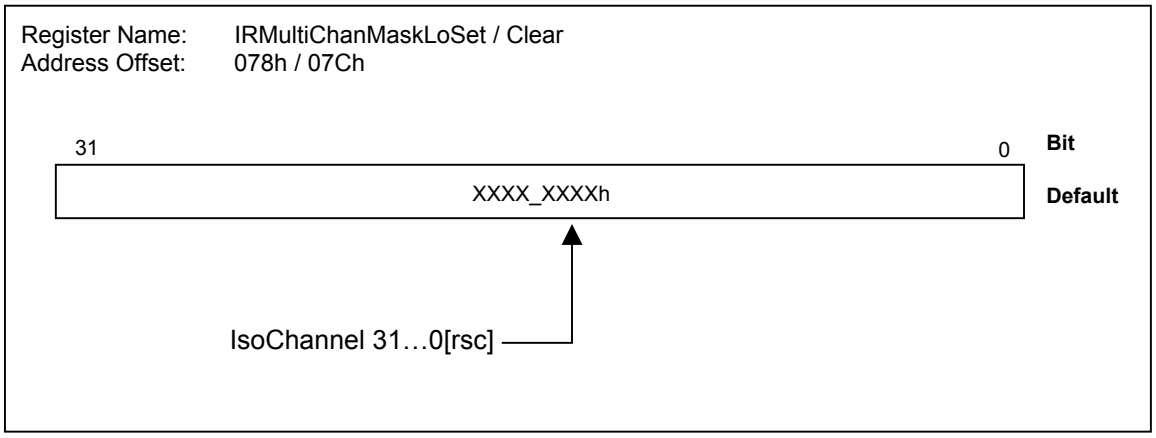


Bit	Field Name	Description
31	selfIDError	When this bit is one, an error is detected during the most recent self ID packet reception. The contents of the self ID buffer are undefined. This bit is cleared after a self ID reception in which no errors are detected. Note that an error can be a hardware error or a host bus write error.
30-24	Reserved	This field is read-only and hardwired to zeros. Writing to this field has no effect
23-16	selfIDGeneration	The value in this field increments each time a bus reset is detected. This field rolls over to 0 after reaching 255.
15-13	Reserved	This field is read-only and hardwired to zeros. Writing to this field has no effect
12-2	selfIDSize	This field indicates the number of quadlet that has been written into the self ID buffer for the current selfIDGeneration. This includes the header quadlet and the self ID data. This field is cleared to zero as soon as a bus reset is detected.
1-0	Reserved	This field is read-only and hardwired to zeros. Writing to this field has no effect

9.4.15 Isochronous Receive Multi-Channel Mask Register (set and clear)

The Isochronous Multi-Channel Mask is used to enable packet receives from up to 64 specified isochronous data channels. Software enables receives for any number of isochronous channels by writing ones to the corresponding bits in the IRMultiChanMaskHiSet and IRMultiChanMaskLoSet addresses. To disable receives for any isochronous channels, software writes ones to the corresponding bits in the IRMultiChanMaskHiClear and IRMultiChanMaskLoClear addresses. A read of each IRMultiChanMask register shows that channels are enabled; a one for enabled and a zero for disabled.

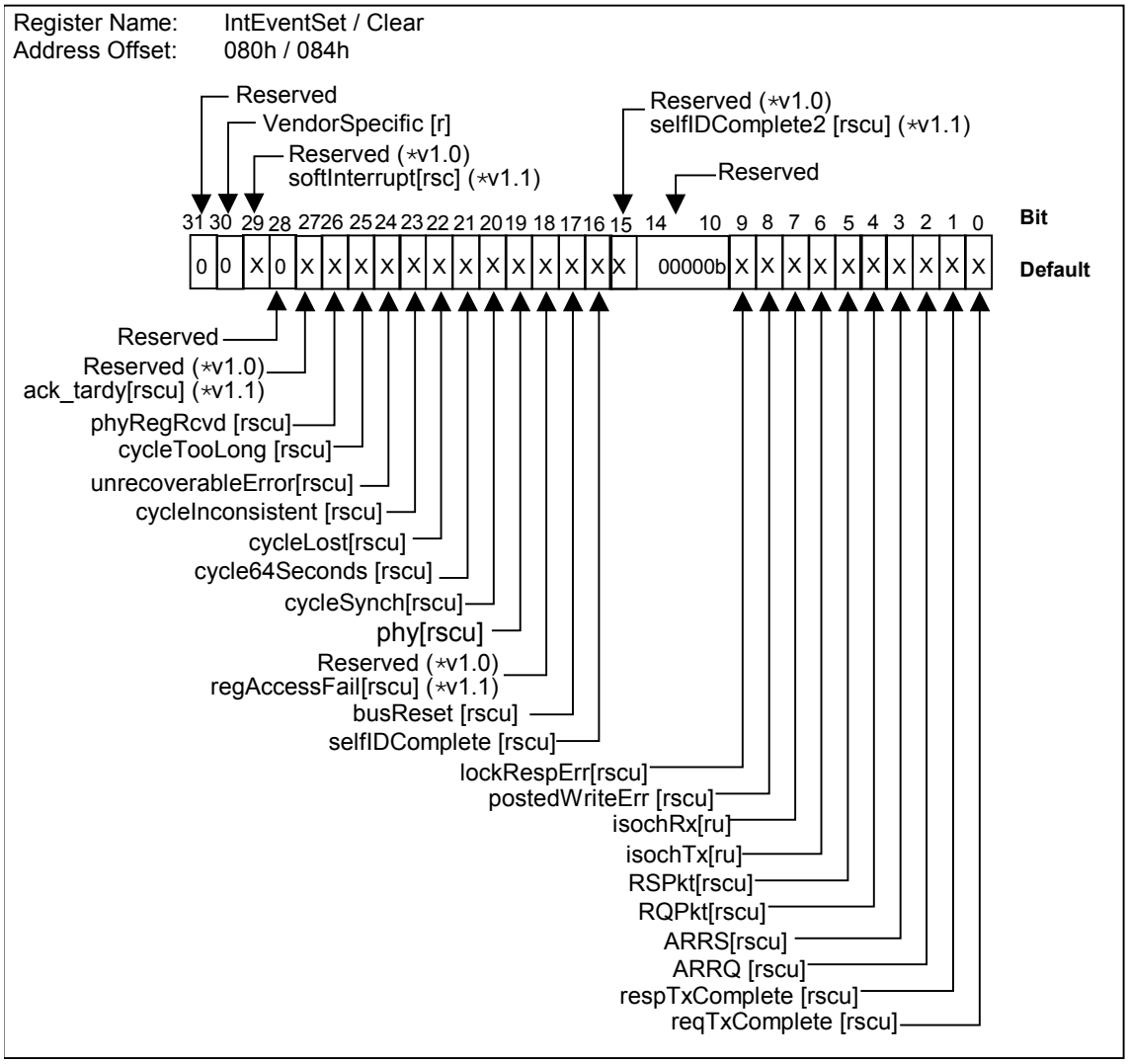




Bit	Field Name	Description
31-0	IsoChannel"N"	When set, R5C551 is enabled to receive from ISO channel number "N".

9.4.16 Interrupt Event Register (set and clear)

This register reflects the state of the various interrupt sources from the 1394 OHCI. The interrupt bits are set by an asserting edge of the corresponding interrupt signal, or by software by writing a one to the corresponding bit in the IntEventSet address. They are cleared by writing a one to the corresponding bit in the IntEventClear address. Reading the IntEventSet register returns the current state of the IntEvent register. Reading the IntEventClear register returns the masked version of the IntEvent register (IntEvent & IntMask).

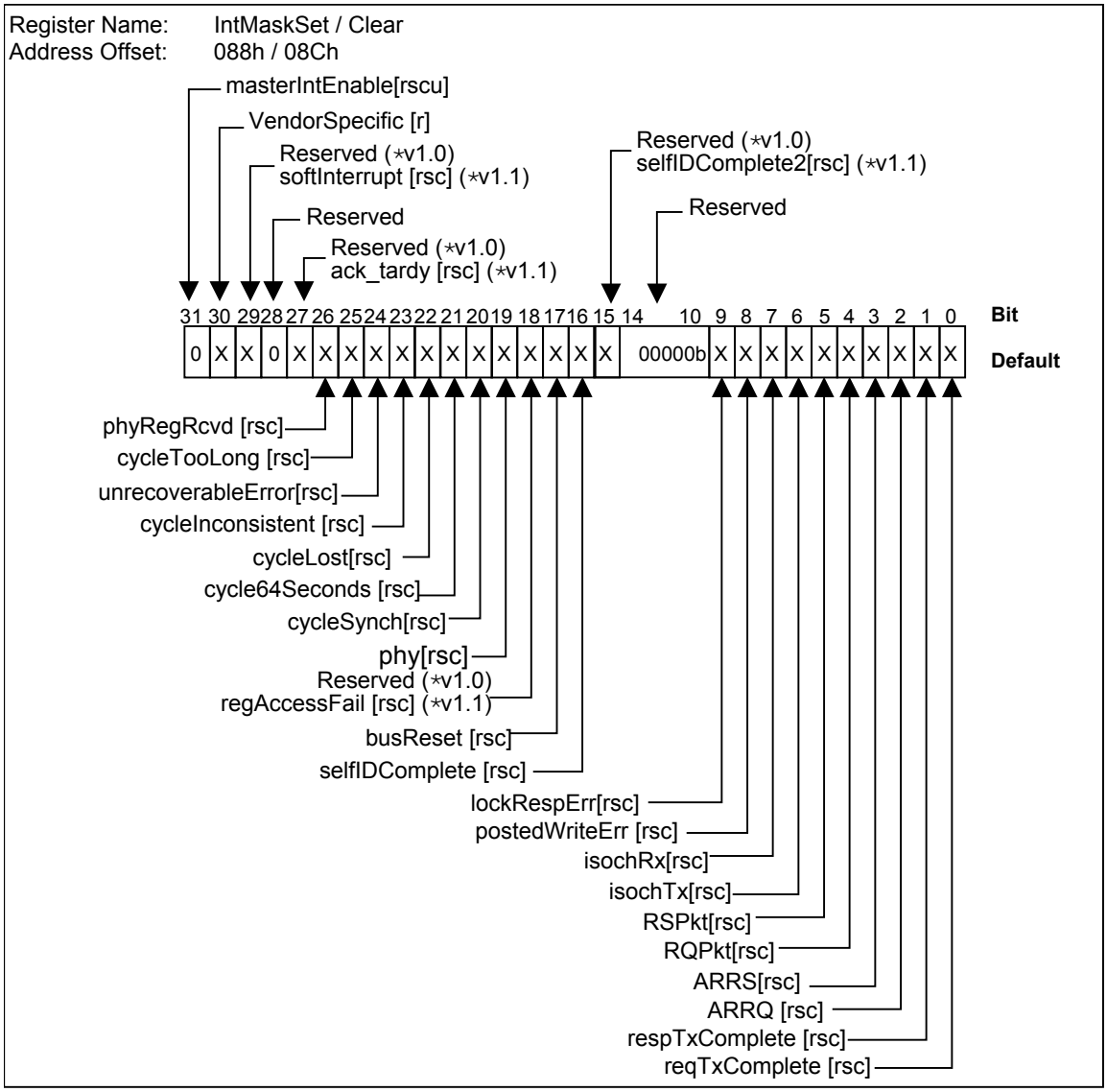


Bit	Field Name	Description
31	Reserved	This bit is reserved for future use and read-only. The default after reset is zero.
30	vendorSpecific	Vendor defined. This bit is read-only and hardwired to zero.
29	Reserved (*v1.0)	This bit is reserved for future use and read-only. The default after reset is zero.
	softInterrupt (*v1.1)	This bit is used software to occur an interrupt.
28	Reserved	This bit is reserved for future use and read-only. The default after reset is zero.
27	Reserved (*v1.0)	This bit is reserved for future use and read-only. The default after reset is zero.
	ack_tardy (*v1.1)	This bit indicates the following state when the HCControl.ackTardyEnable bit is set. a) Transfer data to host is present in a receive FIFO. b) State of the physical response unit is busy processing requests or sending responses. c) The Host Controller sent ack_tardy acknowledgment.
26	phyRegRcvd	R5C551 has received a PHY register data byte that can be read from the PHY control register.
25	cycleTooLong	When LinkControl.cycleMaster is set and the Host Controller is the 1394 root node, this bit indicates that an isochronous cycle lasted longer than the allotted time. R5C551 is expected to trigger this event no less than 115 μsec after sending a cycle start packet unless a sub-action gap or bus reset indication is first observed. LinkControl.cycleMaster is cleared by this event.
24	unrecoverableError	This event occurs when R5C551 encounters any error that forces it to stop operations on any or all of its subunits. For example, when a DMA context sets its contextControl.dead bit. While unrecoverableError is set, all normal interrupts for the context(s) that caused this interrupt will be blocked from being set.
23	cycleInconsistent	A cycle start was received that had an isochronous cycleTimer.seconds and isochronous cycleTimer.count different from the value in the CycleTimer register.
22	cycleLost	A lost cycle is indicated when no cycle_start packet is sent/received between two successive cycleSynch events.
21	cycle64Seconds	This bit indicates that the 7th bit of the cycle second counter has changed.
20	cycleSynch	This bit indicates that a new isochronous cycle has started. Set when the low order bit of the internal isochronousCycleTimer.cycleCount toggles.
19	phy	This bit is generated when the PHY requests an interrupt through a status transfer.
18	Reserved (*v1.0)	This bit is reserved for future use and read-only. The default after reset is zero.
	regAccessFail (*v1.1)	This bit indicates that the OHCI register access failed because of a missing SCLK clock signal from the PHY.
17	busReset	This bit indicates that the PHY chip has entered bus reset mode.
16	selfIDComplete	A selfID packet stream has been received. It will be generated at the end of the bus initialization process if LinkControl.rcvSelfID is set. This bit is turned off simultaneously when IntEvent.busReset is turned on.
15	Reserved (*v1.0)	This bit is reserved for future use and read-only. The default after reset is zero.
	selfIDcomplete2 (*v1.1)	This bit is set to one when the selfIDcomplete is set. This bit is independent of the IntEvent.busReset and reset only by software.
14-10	Reserved	This field is reserved for future use and read-only. The default after reset is zero.
9	lockRespErr	This bit iIndicates that R5C551 attempted to return a lock response for a lock request to a serial bus register, but did not receive an ack_complete after exhausting all permissible retries.
8	postedWriteErr	This bit indicates that a host bus error is occurred while R5C551 was trying to write a 1394 write request into system memory in spite of having already been given an ack_complete. The 1394 destination offset and sourceID are available in the PostedWriteAddress registers.

Bit	Field Name	Description
7	isochRx	Isochronous Receive DMA interrupt. This bit indicates that one or more isochronous receive contexts have generated an interrupt. This is not a latched event, it is the OR'ing all bits in (isoRecvIntEvent & isoRecvIntMask). The isoRecvIntEvent register indicates which contexts have interrupted.
6	isochTx	Isochronous Transmit DMA interrupt. This bit indicates that one or more isochronous transmit contexts have generated an interrupt. This is not a latched event, it is the OR'ing all bits in (isoXmitIntEvent & isoXmitIntMask). The isoXmitIntEvent register indicates which contexts have interrupted.
5	RSPkt	This bit indicates that a packet was sent to an asynchronous receive response context buffer and the descriptor's xferStatus and resCount fields have been updated.
4	RQPkt	This bit indicates that a packet was sent to an asynchronous receive request context buffer and the descriptor's xferStatus and resCount fields have been updated.
3	ARRS	Asynchronous Receive Response DMA interrupt. This bit is conditionally set upon completion of an AR DMA Response context command descriptor.
2	ARRQ	Asynchronous Receive Request DMA interrupt. This bit is conditionally set upon completion of an AR DMA Request context command descriptor.
1	respTxComplete	Asynchronous response transmit DMA interrupt. This bit is conditionally set upon completion of an AT DMA response OUTPUT_LAST* command.
0	reqTxComplete	Asynchronous request transmit DMA interrupt. This bit is conditionally set upon completion of an AT DMA request OUTPUT_LAST* command.

9.4.17 Interrupt Mask Register (set and clear)

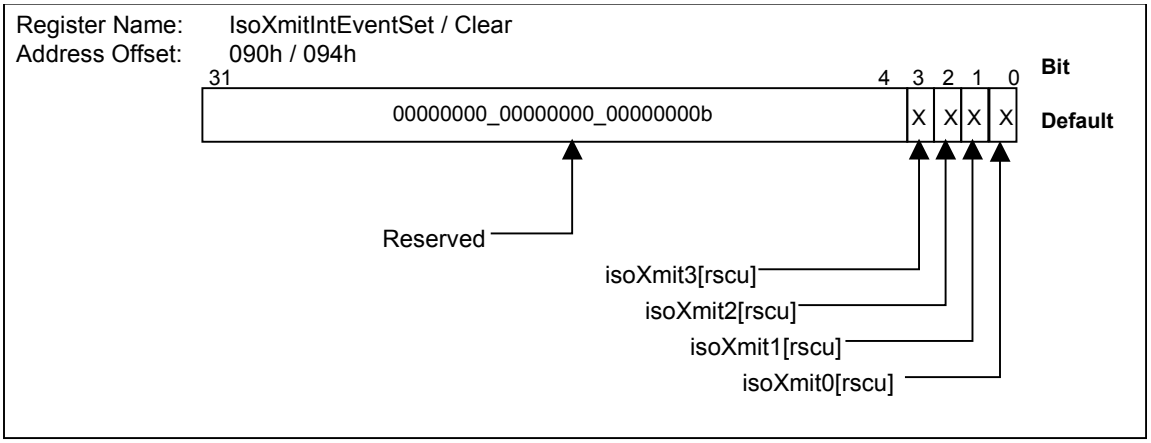
The bits in the IntMask register have the same format as the IntEvent register, with the addition of masterIntEnable (bit 31). A one bit in the IntMask register enables the corresponding IntEvent register bit to generate a processor interrupt. A zero bit in IntMask disables the corresponding IntEvent register bit from generating a processor interrupt. A bit is set in the IntMask register by writing a one to the corresponding bit in the IntMaskSet address and cleared by writing a one to the corresponding bit in the IntMaskClear address. If masterIntEnable is 0, all interrupts are disabled regardless of the values of all other bits in the IntMask register. The value of masterIntEnable has no effect on the value returned by reading the IntEventClear; even if masterIntEnable is 0. On a reset, the IntMask.masterIntEnable bit (31) is set to 0 and the value of all other bits is undefined.

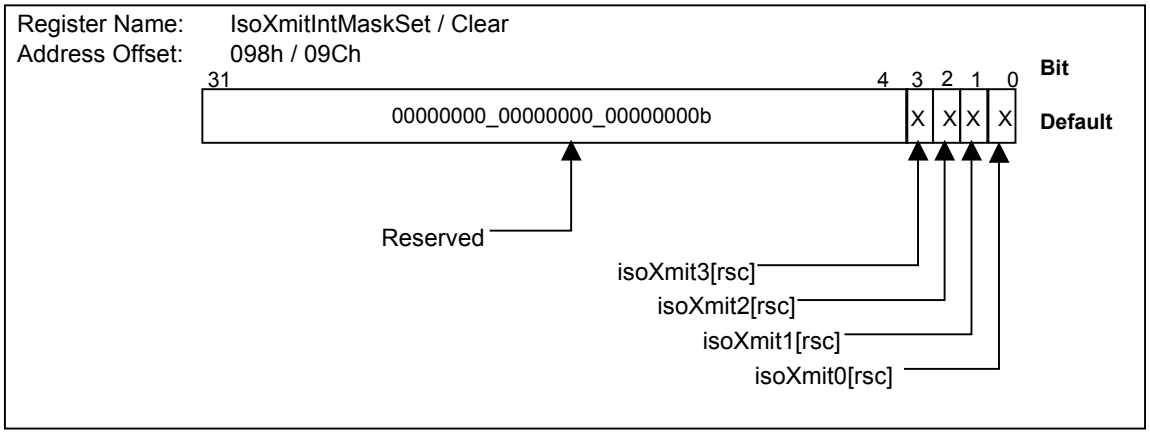


Bit	Field Name	Description
31	masterIntEnable	If set, external interrupts will be generated in accordance with the IntMask register. If clear, no external interrupts will be generated regardless of the IntMask register settings.
30-0		See IntEvent register.

9.4.18 Isochronous Transmit Interrupt Event/Mask Register (set and clear)

This register reflects the interrupt state of the isochronous transmit contexts. An interrupt is generated on behalf of an isochronous transmit context when an OUTPUT_LAST DMA command completes and its i bits are set to 2'b11. (On the OHCI 1.1, an interrupt is also generated when the SKIP transaction is done and i bits of the SKIP transaction command are set to 2'b11.)
Upon determining that the IntEvent.isochTx interrupt has occurred, software can check the isoXmitIntEvent register to determine which context(s) caused the interrupt.
The bits in the isoXmitIntMask register have the same format as the isoXmitIntEvent register. Setting a bit in this register enables the corresponding bit in the isoXmitIntMaskSet address and cleared by writing a one to the corresponding bit in the isoXmitIntMaskClear address.
Reading the isoXmitIntEventSet register returns the current state of the isoXmitIntEvent register. Reading the isoXmitIntEventClear register returns the masked version of the isoXmitIntEvent register (isoXmitIntEvent & isoXmitIntMask).



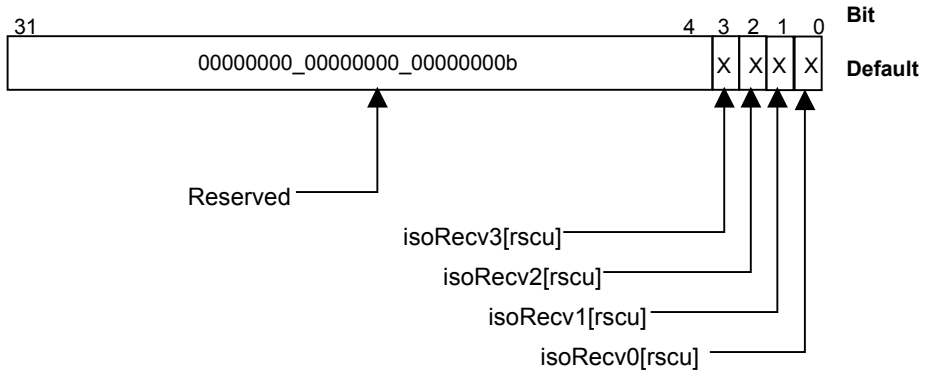


Bit	Field Name	Description
31-4	Reserved	This field is reserved for future use and read-only. The default after reset is zero.
3	isoXmit3	Isochronous transmit context 3 caused the isochTx interrupt.
2	isoXmit2	Isochronous transmit context 2 caused the isochTx interrupt.
1	isoXmit1	Isochronous transmit context 1 caused the isochTx interrupt.
0	isoXmit0	Isochronous transmit context 0 caused the isochTx interrupt.

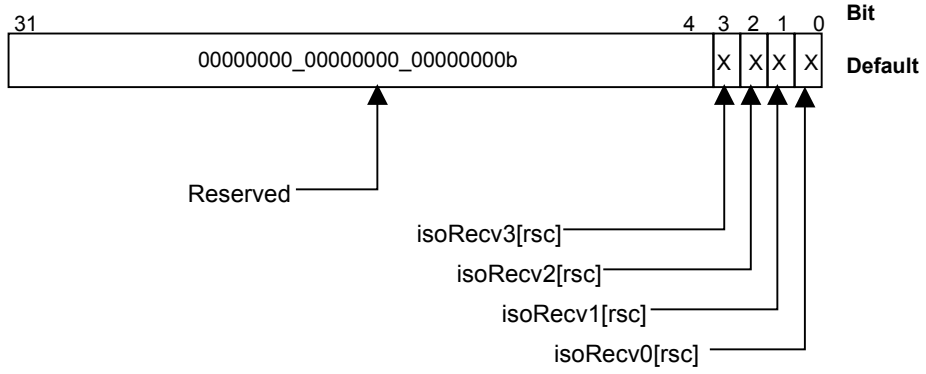
9.4.19 Isochronous Receive Interrupt Event/Mask Register (set and clear)

This register reflects the interrupt state of the isochronous receive contexts. An interrupt is generated on behalf of an isochronous receive context if a final command of a DMA descriptor block completes and its i bits are set to 2'b11. Upon determining that the IntEvent.isochRx interrupt has occurred, software can check the isoRecvIntEvent register to determine which context(s) caused the interrupt.
The bits in the isoRecvIntMask register have the same format as the isoRecvIntEvent register. Setting a bit in this register enables the corresponding bit in the isoRecvIntMaskSet address and cleared by writing a one to the corresponding bit in the isoRecvIntMaskClear address.
Reading the isoRecvIntEventSet register returns the current state of the isoRecvIntEvent register. Reading the isoRecvIntEventClear register returns the masked version of the isoRecvIntEvent register (isoRecvIntEvent & isoRecvInt-Mask).

Register Name: IsoRecvIntEventSet / Clear
Address Offset: 0A0h / 0A4h



Register Name: IsoRecvIntMaskSet / Clear
Address Offset: 0A8h / 0ACh

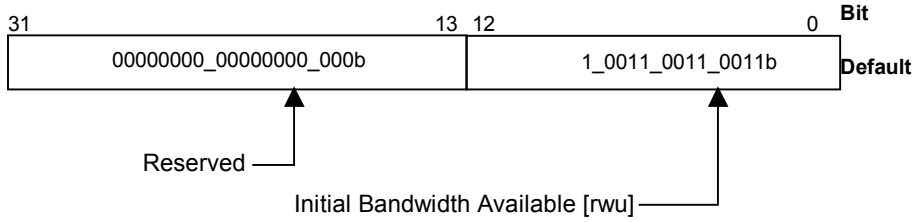


Bit	Field Name	Description
31-4	Reserved	This field is reserved for future use and read-only. The default after reset is zero.
3	isoRecv3	Isochronous receive context 3 caused the isochRx interrupt.
2	isoRecv2	Isochronous receive context 2 caused the isochRx interrupt.
1	isoRecv1	Isochronous receive context 1 caused the isochRx interrupt.
0	isoRecv0	Isochronous receive context 0 caused the isochRx interrupt.

*9.4.20 Bus Management CSR Initialization Register *v1.1*

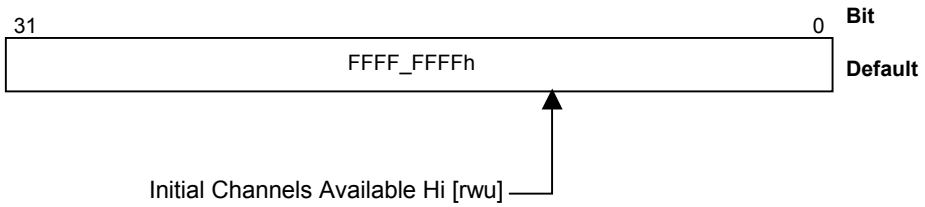
This register stores their values that loaded into each Bus Management CSR registers on hardware reset, software reset and 1394 bus reset. This register is set to their default values on hardware reset and software reset, and isn't affected on 1394 bus reset.

Register Name: Initial Bandwidth Available
Address Offset: 0B0h

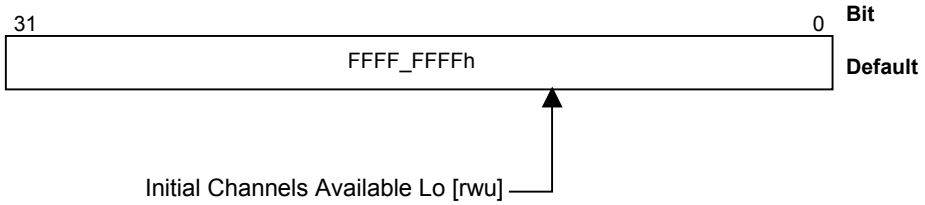


Bit	Field Name	Description
31-13	Reserved	This field is reserved for future use and read-only. The default after reset is zero.
12-0	InitialBandAvailable	This field is set to 13'h1333 (default value) on hardware reset or software reset, and isn't affected on 1394 bus reset. The values of this field are loaded into the BAND WIDTH_AVAILABLE of the CSR register on hardware reset, software reset or 1394 bus reset.

Register Name: Initial Channels Available Hi
Address Offset: 0B4h



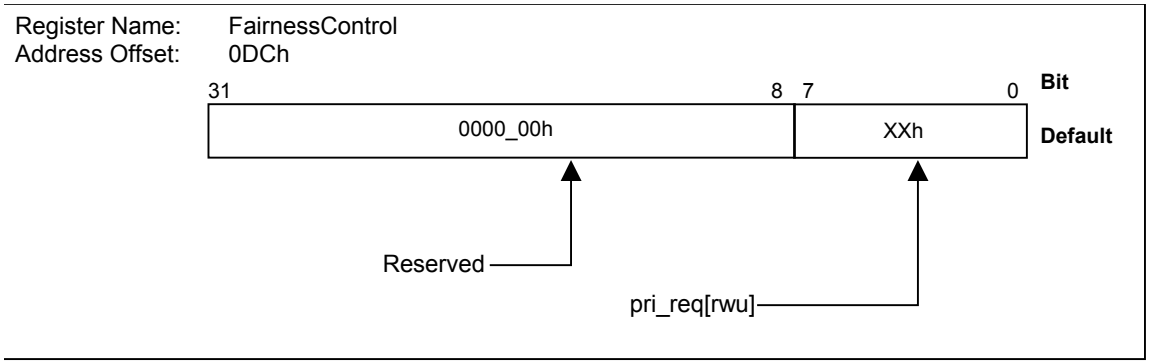
Register Name: Initial Channels Available Lo
Address Offset: 0B8h



Bit	Field Name	Description
Hi 31-0	Initial Channels Available Hi	This field is set to 32'hFFFF_FFFF (default value) on hardware reset or software reset, and isn't affected on 1394 bus reset. The values of this field are loaded into the CHANNELS_AVAILABLE_HI/LO of the CSR register on hardware reset, software reset or 1394 bus reset.
Lo 31-0	Initial Channels Available Lo	

9.4.21 Fairness Control Register

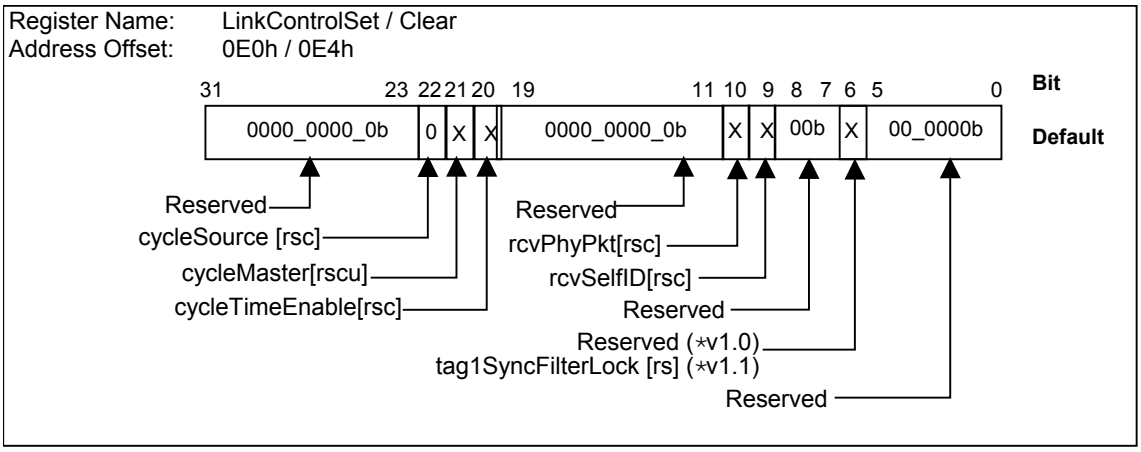
This register provides a mechanism by which software can direct R5C551 to transmit multiple asynchronous request packets during a fairness interval.



Bit	Field Name	Description
31-8	Reserved	This field is reserved for future use and read-only. The default after reset is zero.
7-0	pri_req	This field specifies the maximum number of priority arbitration requests for asynchronous request packets that the link is permitted to make of the PHY during a fairness interval.

9.4.22 Link Control Registers (set and clear)

This register provides the control flags that enable and configure the link core protocol portions of R5C551. It contains controls for the receiver, and cycle timer. There are two addresses for this register: LinkControlSet and LinkControlClear. On read, both addresses return the contents of the control register. For writes, a one bit written to LinkControlSet causes the corresponding bit in the LinkControl register to be set, and a one bit written to LinkControlClear causes the corresponding bit in the LinkControl register to be cleared, while a zero bit leaves the corresponding bit in the LinkControl register unaffected.

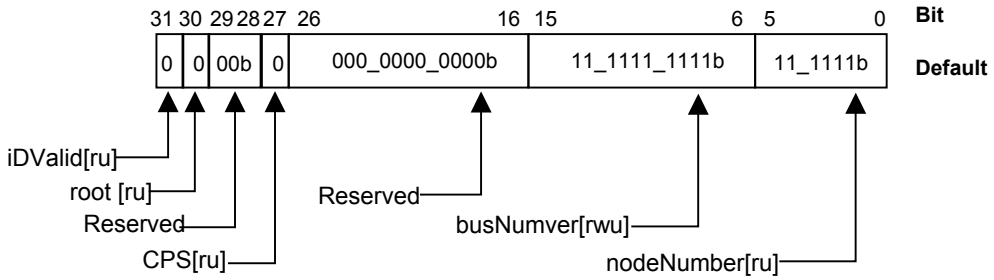


Bit	Field Name	Description
31-23	Reserved	This field is reserved for future use and read-only. The default after reset is zero.
22	cycleSource	When this bit is set to one, the cycle timer will use an external source to determine when to increment cycleCount. When cycleCount is incremented, cycleOffset is reset to zero. If cycleOffset reaches 3071 before an external event occurs, it will remain at 3071 until the external signal is received and is then reset to zero. When zero, the R5C551 will roll the cycle timer over when the timer reaches 3072 cycles of the 24.576 MHz clock. CycleSource has an effect only when cycleMaster is enabled. A software reset has no effect.
21	cycleMaster	When this bit is set to one and the PHY has notified R5C551 that it is root, R5C551 will generate a cycle start packet every time the cycle timer rolls over, based on the setting of the cycleSource bit. When this bit is set to zero, R5C551 will accept received cycle start packets to maintain synchronization with the node that is sending them. This bit is automatically set to zero when the IntEvent.cycleTooLong event occurs and cannot be set until the IntEvent.cycleTooLong bit is cleared.
20	cycleTimeEnable	When this bit is set to one, the cycle timer offset will count cycles of the 24.576 MHz clock and roll over at the appropriate time based on the settings of the above bits. When this bit is set to zero, the cycle timer offset will not count.
19-11	Reserved	This field is reserved for future use and read-only. The default after reset is zero.
10	rcvPhyPkt	When this bit is set to one, the receiver will accept incoming PHY packets into the AR request context if the AR request context is enabled. This does not control either the receipt of self-identification packets during the Self-ID phase of bus initialization or the queuing of synthesized bus reset packets in the AR DMA Request Context buffer.
9	rcvSelfID	When this bit is set to one, the receiver will accept incoming self-identification packets. Before setting this bit to one, software must ensure that the self ID buffer pointer register contains a valid address.
8-7	Reserved	This field is reserved for future use and read-only. The default after reset is zero.
6	Reserved (*v1.0)	This bit is reserved for future use and read-only. The default after reset is zero.
	tag1SyncFilterLock (*v1.1)	When this bit is set to one, ContextMatch.tag1SynchFilter of all IR contexts is set to one. When this bit is set to zero, ContextMatch.tag1SynchFilter has read/write access.
5-0	Reserved	This field is reserved for future use and read-only. The default after reset is zero.

9.4.23 Node Identification Register

This register contains the CSR address for the node on which this chip resides. The 16-bit combination of busNumber and nodeNumber is referred to as the Node ID. This register shall be written by R5C551 with the value in PHY register 0 following the self-identification phase of bus initialization. Although IntEvent.phyRegRcvd shall not be set when the contents of PHY register 0 are written here, software can use the IntEvent.selfIDComplete interrupt to detect that the self-identification phase has completed can then check for a new valid Node ID.

Register Name: NodeID
Address Offset: 0E8h

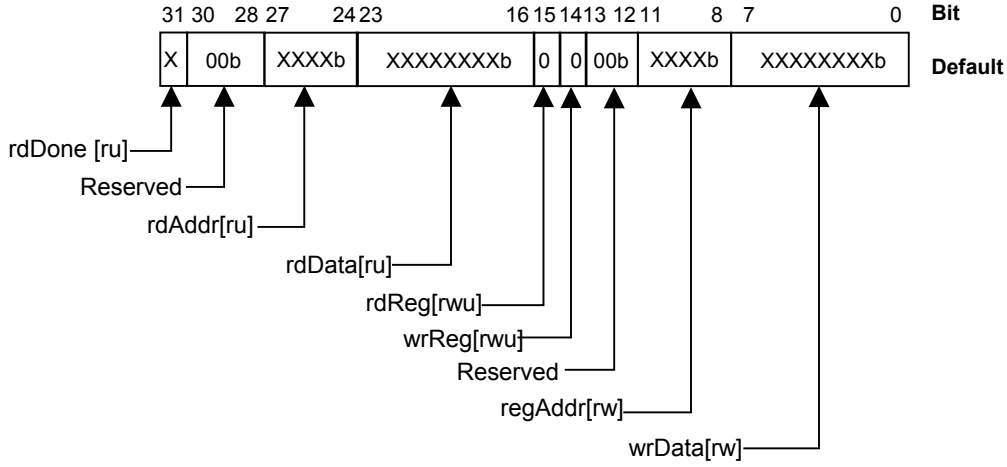


Bit	Field Name	Description
31	iDValid	This bit indicates whether or not R5C551 has a valid node number. It is cleared when the bus reset state is detected and set again when R5C551 receives a new node number from the PHY. If iDValid is clear, software should not set ContextControl.run for either of the AT DMA contexts.
30	root	This bit is set during the bus reset process if the attached PHY is root.
29-28	Reserved	This field is reserved for future use and read-only. The default after reset is zero.
27	CPS	Set if the PHY is reporting that cable power status is OK.
26-16	Reserved	This field is reserved for future use and read-only. The default after reset is zero.
15-6	busNumber	This number is used to identify the specific 1394 bus this node belongs to when multiple 1394-compatible busses are connected via a bridge. This field is set to 10'h3FF on a bus reset.
5-0	nodeNumber	This number is the physical node number established by the PHY during self-identification. It is automatically set to the value received from the PHY after the self-identification phase. If the PHY sets the nodeNumber to 63, software should not set ContextControl.run for either of the AT DMA contexts.

9.4.24 PHY Control Register

The PHY control register is used to read or write a PHY register. To read a register, the address of the register is written to the regAddr field along with a 1 in the rdReg bit. When the read request has been sent to the PHY, the rdReg bit is cleared to 0. When the PHY returns the register, the rdDone bit transitions to one and then the IntEvent.phyRegRcvd interrupt is set. The address of the register received is placed in the rdAddr field and the contents in the rdData field.
To write to a PHY register, the address of the register is written to the regAddr field, the value to write to the wrData field, and a 1 to the wrReg bit. The wrReg bit is cleared when the write request has been transferred to the PHY.
Only after the current PHY register read or write completes may software issue a different PHY register read or write.

Register Name: PhyControl
Address Offset: 0ECh

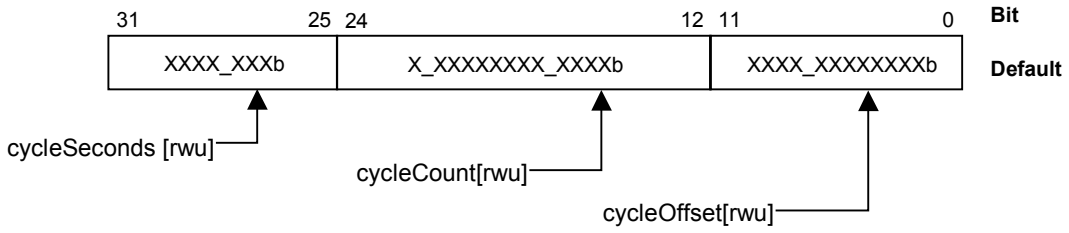


Bit	Field Name	Description
31	rdDone	rdDone is cleared to 0 by R5C551 when either rdReg or wrReg is set to 1. This bit is set to 1 when a register transfer is received from the PHY.
30-28	Reserved	This field is reserved for future use and read-only. The default after reset is zero.
27-24	rdAddr	This is the address of the register most recently received from the PHY.
23-16	rdData	Contains the data read from the PHY register at rdAddr
15	rdReg	Set rdReg to initiate a read request to a PHY register. This bit is cleared when the read request has been sent. The wrReg bit must not be set while the rdReg bit is set.
14	wrReg	Set wrReg to initiate a write request to a PHY register. This bit is cleared when the write request has been sent. The rdReg bit must not be set while the wrReg bit is set.
13-12	Reserved	This field is reserved for future use and read-only. The default after reset is zero.
11-8	regAddr	regAddr is the address of the PHY register to be written or read.
7-0	wrData	This is the contents to be written to a PHY register. Ignored for a read.

9.4.25 Isochronous Cycle Timer Register

The isochronous cycle timer register is a read/write register that shows the current cycle number and offset. The cycle timer register is split up into three fields. The lower order 12 bits are the cycle offset, the middle 13 bits are the cycle count, and the upper order 7 bits count time in seconds. When the R5C551 is cycle master, this register is transmitted with the cycle start message. When R5C551 is not cycle master, this register is loaded with the data field in each incoming cycle start. In the event that the cycle start message is not received, the fields continue incrementing on their own to maintain a local time reference.

Register Name: IsoCycleTimer
Address Offset: 0F0h

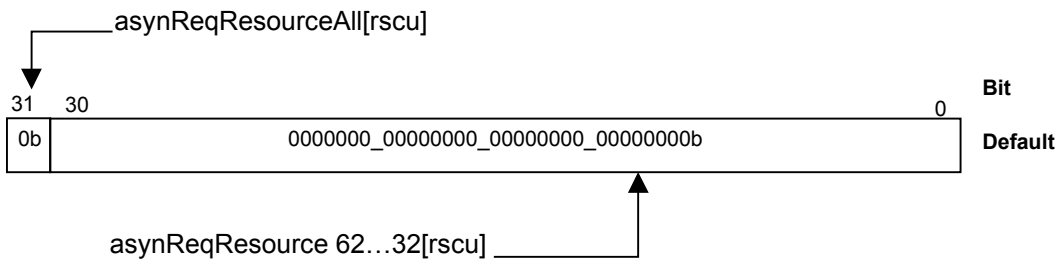


Bit	Field Name	Description
31-25	cycleSeconds	This field counts seconds (cycleCount rollovers) modulo 128
24-12	cycleCount	This field counts cycles (cycleOffset rollovers) modulo 8000.
11-0	cycleOffset	This field counts 24.576MHz clocks modulo 3072, i.e., 125 ms. If an external 8KHz clock configuration is being used, cycleOffset must be set to 0 at each tick of the external clock.

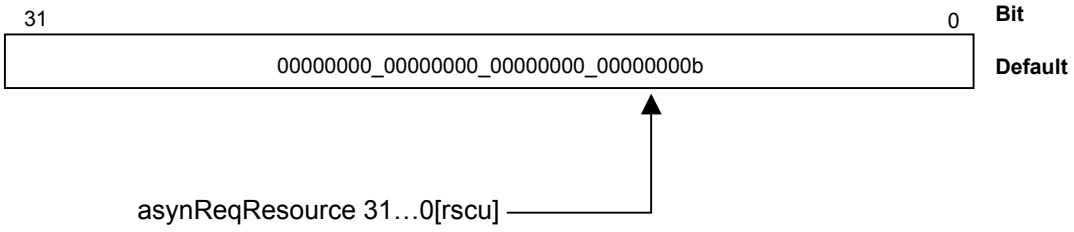
9.4.26 Asynchronous Request Filter Register (set and clear)

When a request is received from the 1394 bus and that request does not access the first 1K of CSR config ROM on R5C551, then the sourceID is used to index into the AsynReqFilter. If the corresponding bit in the AsynReqFilter is set to 0, then requests from that device are not enabled; there will be no ack_sent, and the requests will be ignored by R5C551. If however, the bit is set to 1, the requests are accepted and will be processed according to the address of the request and the setting of the PhyReqFilter register.
Writing a one to the corresponding bit either on the AsynReqFilterHiSet address or on the AsynReqFilterLoSet address sets the AsynReqFilter bits. Writing a one to the corresponding bit either on the AsynReqFilterHiClear address or on the AsynReqFilterLoClear address clears them. If bit asynReqResource"N" is set, then requests with a sourceID of either {10'h3FF, #N} or {busID, #N} will be accepted. If the asynReqResourceAll bit is set in AsynReqFilterHi, requests from all bus nodes including those on the local bus are accepted.
Reading the AsynReqFilter registers returns their current state. All asynReqResource"N" bits in the AsynReqFilter register is cleared to 0 on a 1394 bus reset.
On the OHCI 1.1, the AsynReqFilter register isn't affected by write access when 1394 bus reset is generated and IntEvent.busReset is set to one.

Register Name: AsynReqFilterHiSet / Clear
Address Offset: 100h / 104h



Register Name: AsynReqFilterLoSet / Clear
Address Offset: 108h / 10Ch

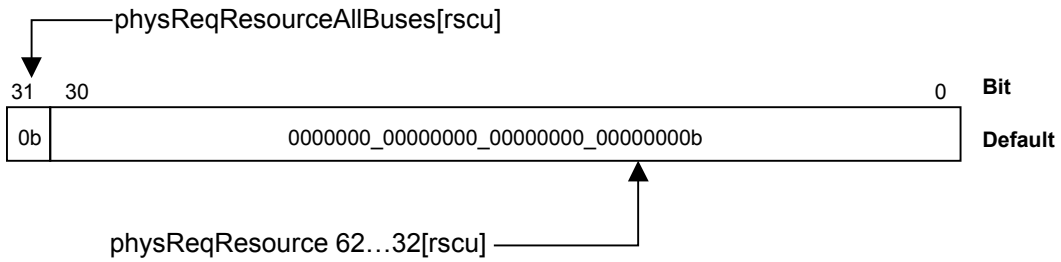


Bit	Field Name	Description
Hi 31	asynReqResouceAll	If set to one, all asynchronous requests received by R5C551 from all bus nodes (including the local bus) will be accepted, and the values of all asynReqResource"N" bits shall be ignored. A bus reset does not affect the value of the asynReqResourceAll bit.
Hi 30-0	asynReqResouce"N"	If set to one for local bus node number "N", asynchronous requests received by R5C551 from that node will be accepted. All asynReqResource"N" bits shall be cleared to zero when a bus reset occurs.
Lo 31-0		

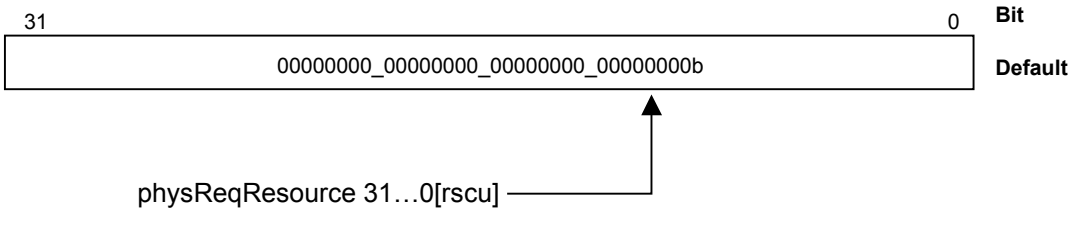
9.4.27 Physical Request Filter Registers (set and clear)

If an asynchronous request is allowed from a node, and the offset is below PhysicalUpperBound the sourceID of the request is used as an index into the PhyReqFilter. If the corresponding bit in the PhyReqFilter is set to 0, then the request is forwarded to the Asynchronous Receive Request DMA context. If however, the bit is set to 1, then the request is sent to the physical response unit. (Note that within the Physical Range, lock transactions and block transactions with a non-zero extended tcode are always forwarded to the Asynchronous Receive Request DMA context.)
Writing a one to the corresponding bit either on the PhyReqFilterHiSet address or on the PhyReqFilterLoSet address sets the PhyReqFilter bits. Writing a one to the corresponding bit either on the PhyReqFilterHiClear address or on the PhyReqFilterLoClear address clears them. If bit physReqResource"N" is set, then requests with a sourceID of either {10'h3FF, #N} or {busID, #N} will be accepted. If the physReqResourceAllBuses bit is set in PhyReqFilterHi, physical requests from any device on any other bus are accepted (bus number other than 10'h3FF and busID).
Reading the PhyReqFilter registers returns their current state. All bits in the PhyReqFilter are set to 0 on a 1394 bus reset.
On the OHCI 1.1, the PhysReqFilter register isn't affected by write access when 1394 bus reset is generated and IntEvent.busReset is set to one.

Register Name: PhyReqFilterHiSet / Clear
Address Offset: 110h / 114h



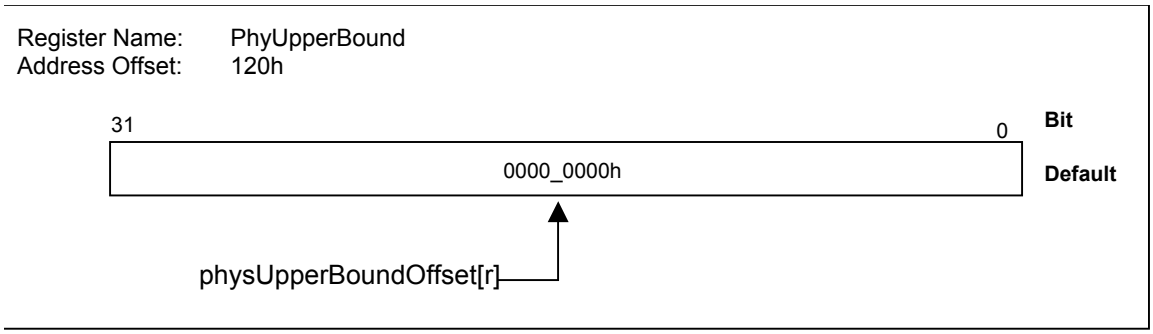
Register Name: PhyReqFilterLoSet / Clear
Address Offset: 118h / 11Ch



Bit	Field Name	Description
Hi 31	physReqResouce AllBuses	If set to one, all asynchronous physical requests received by R5C551 from non-local bus nodes will be accepted.
Hi 30-0	physReqResouce"N"	If set to one for local bus node number "N", then asynchronous physical requests received by R5C551 from that node will be accepted.
Lo 31-0		

9.4.28 Physical Upper Bound Register (optional)

Asynchronous requests that are candidates to be handled by the physical response unit include requests that have a destination offset which falls within the physical range. This range begins at 48'h0 and ends at the offset specified in this register. In general, requests at physUpperBoundOffset or higher will be handled by the Asynchronous Receive Request context.
This register is an optional register and is not implemented. This register is read only and returns all zeros.



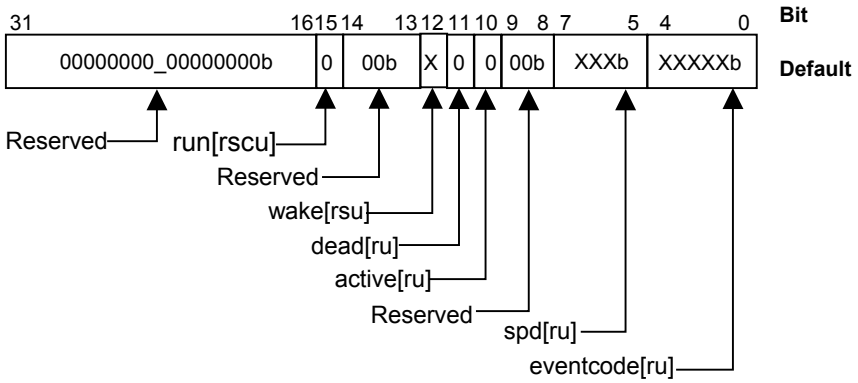
Bit	Field Name	Description
31-0	physUpperBounds Offset	This register is read-only with a value of 32'h0 and the upper bound of the physical range is 48'h0001_0000_0000.

9.4.29 Asynchronous Context Control Register (set and clear)

The ContextControlSet and ContextControlClear registers contain bits that control options, operational state, and status for a DMA context. Software can set selected bits by writing ones to the corresponding bits in the ContextControlSet register. Software can clear selected bits by writing ones to the corresponding bits in the ContextControlClear register. It is not possible for software to set some bits and clear others in an atomic operation. A read from either register will return the same value.

- ContextControlSet/Clear registers for Asynchronous Transmit Request
- ContextControlSet/Clear registers for Asynchronous Transmit Response
- ContextControlSet/Clear registers for Asynchronous Receive Request
- ContextControlSet/Clear registers for Asynchronous Receive Response

Register Name: ATReqContextControlSet/Clear
Address Offset: 180h / 184h
Register Name: ATRespContextControlSet/Clear
Address Offset: 1A0h / 1A4h
Register Name: ARReqContextControlSet/Clear
Address Offset: 1C0h / 1C4h
Register Name: ARRespContextControlSet/Clear
Address Offset: 1E0h / 1E4h



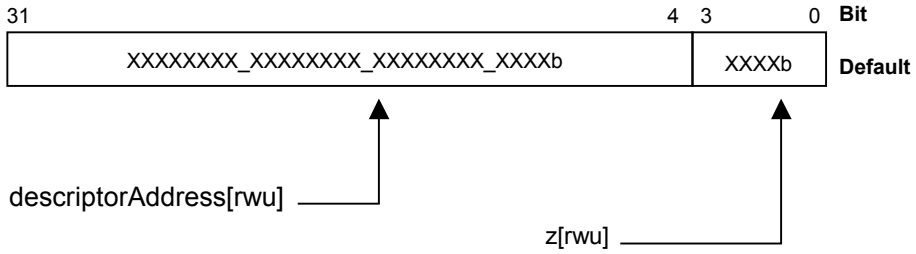
Bit	Field Name	Description
31-16	Reserved	This field is reserved for future use and read-only. The default after reset is zero.
15	run	The run bit is set by software to enable descriptor processing for a context and cleared by software to stop descriptor processing. R5C551 will only change this bit on a hardware or software reset to set it to 0.
14-13	Reserved	This field is reserved for future use and read-only. The default after reset is zero.
12	wake	Software sets this bit to 1 to cause R5C551 to continue or resume descriptor processing. R5C551 will clear this bit on every descriptor fetch.
11	dead	R5C551 sets this bit when it encounters a fatal error, and clears this bit when software clears the run bit.
10	active	R5C551 sets this bit to 1 when it is processing descriptors.
9-8	Reserved	This field is reserved for future use and read-only. The default after reset is zero.
7-5	spd	This field indicates the speed at which the packet was received. 3'b000 = 100 Mbits/sec 3'b001 = 200 Mbits/sec 3'b010 = 400 Mbits/sec All other values are reserved. spd only contains meaningful information for receive contexts. Software should not attempt to interpret the contents of this field while the ContextControl.active or ContextControl.wake bits are set.
4-0	eventcode	This field holds the acknowledge sent by the Link core for this packet, or an internally generated error code. Possible values are: (TX) ack_complete, ack_pending, ack_busy_X, ack_busy_A, ack_busy_B, ack_data_error, ack_type_error, evt_tcode_err, evt_missing_ack, evt_underrun, evt_descriptor_read, evt_data_read, evt_timeout, evt_flushed, evt_unknwn. (RX) ack_complete, ack_pending, ack_type_error, evt_descriptor_read, evt_data_write, evt_bus_reset, evt_unknown, evt_no_status.

9.4.30 Asynchronous Context Command Pointer Register

Software initializes CommandPtr.descriptorAddress to contain the address of the first descriptor block that R5C551 will access when software enables the context by setting ContextControl.run. Software also initializes CommandPtr.Z to indicate the number of descriptors in the first descriptor block. Software shall only write to this register when both ContextControl.run and Context-Control.active are zero. R5C551 is not required to enforce this rule and its behavior when this rule is violated is undefined.

- CommandPtr register for Asynchronous Transmit Request
- CommandPtr register for Asynchronous Transmit Response
- CommandPtr register for Asynchronous Receive Request
- CommandPtr register for Asynchronous Receive Response

Register Name: ATReqCommandPtr
Address Offset: 18Ch
Register Name: ATRespCommandPtr
Address Offset: 1ACh
Register Name: ARReqCommandPtr
Address Offset: 1CCh
Register Name: ARRespCommandPtr
Address Offset: 1ECh



Bit	Field Name	Description
31-4	descriptorAddress	Contains the upper 28 bits of the address of a 16-byte aligned descriptor block.
3-0	z	Indicates the number of contiguous 16-byte aligned blocks at the address pointed to by descriptorAddress. If Z is 0, it indicates that the descriptorAddress is not valid.

Since R5C551 utilizes the CommandPtr register while processing a context, there is a set of guidelines by which software may safely and deterministically read CommandPtr. These guidelines are based on the ContextControl bits as follows (X='don't care'):

CommandPtr read values

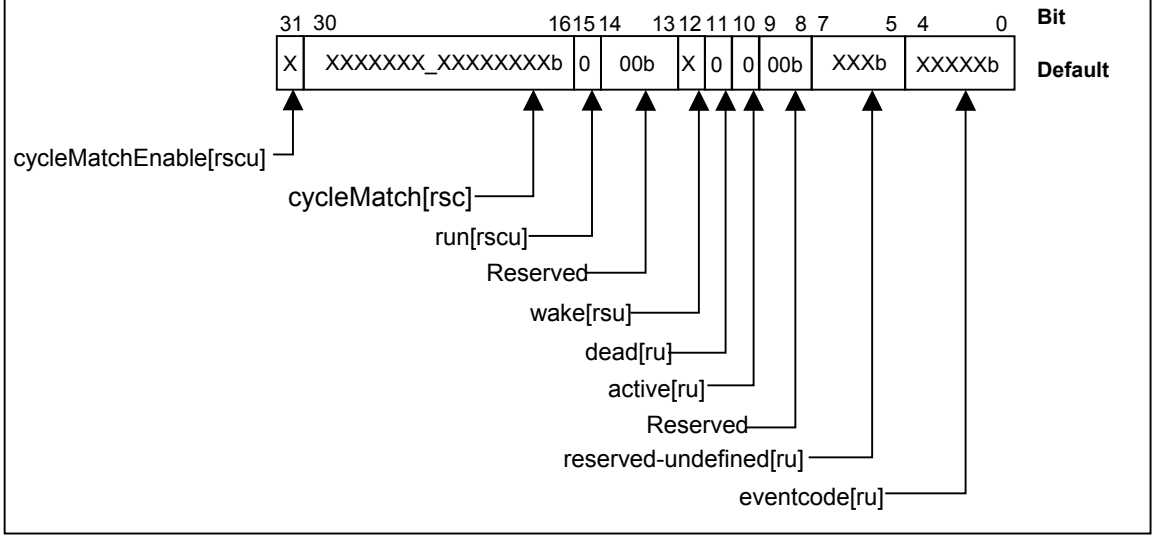
ContextControl fields				CommandPtr.descriptorAddress Value
Run	Dead	Active	Wake	
0	0	0	X	A descriptor block address. Either last written or last executed
0	0	1	X	Contents unspecified.
1	0	0	0	Refers to the descriptor block that contains the Z=0 that caused the Host Controller to set active to 0.
1	0	0	1	Contents unspecified.
1	0	1	X	On processing or Points to the next descriptor block.
1	1	0	X	Points to the descriptor block in which a fatal error occurred.

9.4.31 Isochronous Transmit Context Control Register (set and clear)

IT ContextControl is used by software to control the context's behavior, and is used by hardware to indicate current status. The IT ContextControl set and clear registers contains bits that control options, operational state, and status for the isochronous transmit DMA contexts. Software can set selected bits by writing ones to the corresponding bits in the ContextControlSet register. Software can clear selected bits by writing ones to the corresponding bits in the ContextControlClear register. It is not possible for software to set some bits and clear others in an atomic operation. A read from either register will return the same value.

- ContextControlSet/Clear register for Isochronous Transmit Context 0
- ContextControlSet/Clear register for Isochronous Transmit Context 1
- ContextControlSet/Clear register for Isochronous Transmit Context 2
- ContextControlSet/Clear register for Isochronous Transmit Context 3

Register Name: ITCont0ContextControlSet/Clear
Address Offset: 200h / 204h
Register Name: ITCont1ContextControlSet/Clear
Address Offset: 210h / 214h
Register Name: ITCont2ContextControlSet/Clear
Address Offset: 220h / 224h
Register Name: ITCont3ContextControlSet/Clear
Address Offset: 230h / 234h



Bit	Field Name	Description
31	cycleMatchEnable	When set to one, processing will occur such that the packet described by the context's first descriptor block will be transmitted in the cycle whose number is specified in the cycleMatch field of this register. The 15-bit cycleMatch field must match the low order two bits of cycleSeconds and the 13-bit cycleCount field in the cycle start packet that is sent or received immediately before isochronous transmission begins. Once the context has become active, hardware clears the cycleMatchEnable bit.
30-16	cycleMatch	Contains a 15-bit value, corresponding to the low order two bits of the bus CycleTime.cycleSeconds and the 13-bit CycleTime.cycleCount field. If ContextControl.cycleMatchEnable is set, then this IT DMA context will become enabled for transmits when the low order two bits of the bus CycleTime.cycleSeconds and CycleTime.cycleCount value equals the cycleMatch value.

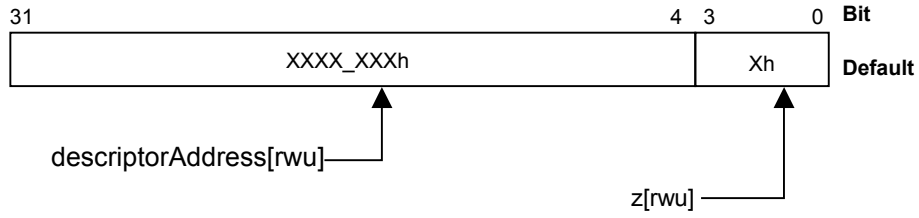
Bit	Field Name	Description
15	run	See Asynchronous ContextControl.run bit
14-13	Reserved	This field is reserved for future use and read-only. The default after reset is zero.
12	wake	See Asynchronous ContextControl.wake bit
11	dead	See Asynchronous ContextControl.dead bit
10	active	See Asynchronous ContextControl.active bit
9-8	Reserved	This field is reserved for future use and read-only. The default after reset is zero.
7-5	reserved-undefined	This field is specified as undefined and may contain any value without impacting the intended processing of this packet.
4-0	eventcode	Following an OUTPUT_LAST* command, the error code is indicated in this field. Possible values are: ack_complete, evt_underrun, evt_descriptor_read, evt_data_read, evt_tcode_err, evt_unknown and evt_timeout (*v1.1).

9.4.32 Isochronous Transmit Context Command Pointer Register

The CommandPtr register specifies the address of the context program that will be executed when a DMA context is started. All descriptors are 16-byte aligned, so the four least-significant bits of any descriptor address must be zero. The four least-significant bits of the CommandPtr register are used to encode a Z value that indicates how many physically contiguous descriptors are pointed to by descriptorAddress.

- CommandPtr register for Isochronous Transmit Context 0
- CommandPtr register for Isochronous Transmit Context 1
- CommandPtr register for Isochronous Transmit Context 2
- CommandPtr register for Isochronous Transmit Context 3

Register Name: ITCont0CommandPtr
Address Offset: 20Ch
Register Name: ITCont1CommandPtr
Address Offset: 21Ch
Register Name: ITCont2CommandPtr
Address Offset: 22Ch
Register Name: ITCont3CommandPtr
Address Offset: 23Ch



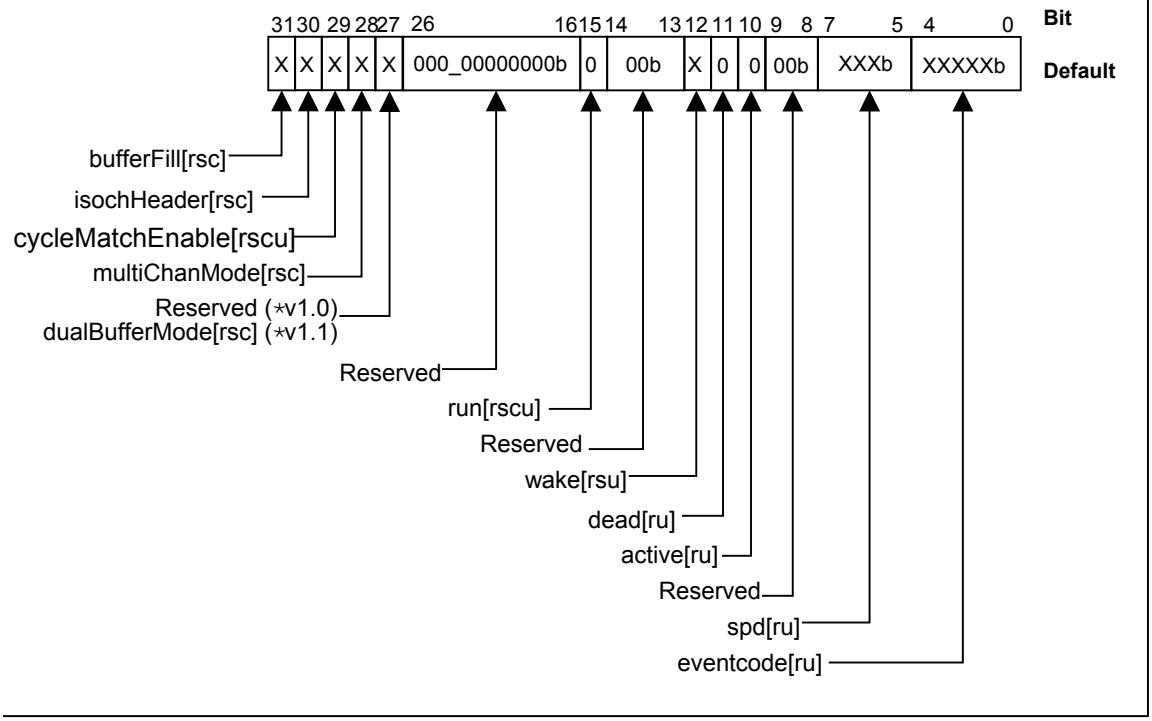
Bit	Field Name	Description
31-4	descriptorAddress	Contains the upper 28 bits of the address of a 16-byte aligned descriptor block.
3-0	z	Indicates the number of contiguous 16-byte aligned blocks at the address pointed to by descriptorAddress. If Z is 0, it indicates that the descriptorAddress is not valid.

9.4.33 Isochronous Receive Context Control Register (set and clear)

The IRContextControl register contains bits that control options, operational state, and status for the isochronous receive DMA contexts. Software can set selected bits by writing ones to the corresponding bits in the ContextControlSet register. Software can clear selected bits by writing ones to the corresponding bits in the ContextControlClear register. It is not possible for software to set some bits and clear others in an atomic operation. A read from either register will return the same value.

- ContextControlSet/Clear register for Isochronous Receive Context 0
- ContextControlSet/Clear register for Isochronous Receive Context 1
- ContextControlSet/Clear register for Isochronous Receive Context 2
- ContextControlSet/Clear register for Isochronous Receive Context 3

Register Name: IRCont0ContextControlSet/Clear
Address Offset: 400h / 404h
Register Name: IRCont1ContextControlSet/Clear
Address Offset: 420h / 424h
Register Name: IRCont2ContextControlSet/Clear
Address Offset: 440h / 444h
Register Name: IRCont3ContextControlSet/Clear
Address Offset: 460h / 464h



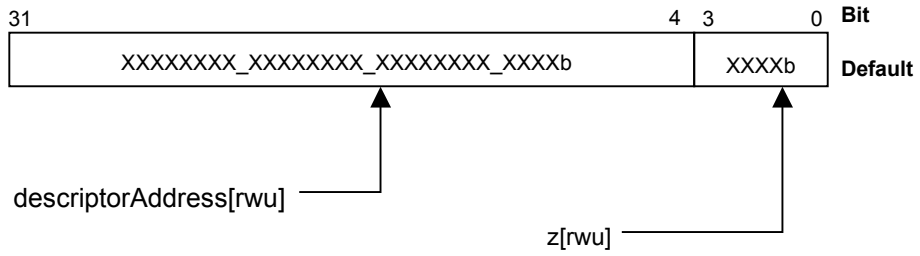
Bit	Field Name	Description
31	bufferFill	When set to one, received packets are placed back-to-back to completely fill each receive buffer. When clear, each received packet is placed in a single buffer. If the multiChanMode bit is set to one, this bit must also be set to one. The value of bufferFill must not be changed while active or run are set to one.
30	isochHeader	When set to one, received isochronous packets will include the complete 4-byte isochronous packet header seen by the link layer. The end of the packet will be marked with a xferStatus in the first doublet, and a 16-bit timeStamp indicating the time of the most recently received (or sent) cycleStart packet. When clear, the packet header is stripped off of received isochronous packets. The packet header, if received, immediately precedes the packet payload. The value of isochHeader must not be changed while active or run are set to one.
29	cycleMatchEnable	In general, when set to one, the context will begin running only when the 15-bit cycleMatch field in the contextMatch register matches the two bits of the bus CycleTime.cycleSeconds and 13-bit CycleTime.cycleCount values. The effects of this bit however are impacted by the values of other bits in this register and are explained below. Once the context has become active, hardware clears the cycleMatchEnable bit. The value of cycleMatchEnable must not be changed while active or run are set to one.
28	multiChanMode	When set to one, the corresponding isochronous receive DMA context will receive packets for all isochronous channels enabled in the IRChannelMaskHi/Lo registers. The isochronous channel number specified in the IRDMA context match register is ignored. When set to zero, the IRDMA context will receive packets for that single channel. Only one IRDMA context may use the IRChannelMask registers. If more than one IRDMA context control register has the multiChanMode bit set, results are undefined. The value of multiChanMode must not be changed while active or run are set to one.
27	Reserved (*v.1.0)	This bit is reserved for future use and read-only. The default after reset is zero.
	dualBufferMode (*v.1.1)	When this bit is set to one, received packets are separated into the first buffer and the second buffer and they are present independently. And also, both of multiChanMode and bufferFill are programmed to zero when this bit is set to one. The value of dualBufferMode cannot be changed while active bit or run bit is set to one.
26-16	Reserved	This field is reserved for future use and read-only. The default after reset is zero.
15	run	See Asynchronous ContextControl.run bit
14-13	Reserved	This bit is reserved for future use and read-only. The default after reset is zero.
12	wake	See Asynchronous ContextControl.wake bit
11	dead	See Asynchronous ContextControl.dead bit
10	active	See Asynchronous ContextControl.active bit
9-8	Reserved	This bit is reserved for future use and read-only. The default after reset is zero.
7-5	spd	This field indicates the speed at which the packet was received. 3'b000 = 100Mbits/sec 3'b001 = 200 Mbits/sec 3'b010 = 400 Mbits/sec All other values are reserved.
4-0	eventcode	For bufferFill mode, possible values are: ack_complete, evt_descriptor_read, evt_data_write and evt_unknown. Packets with data errors (either dataLength mis-matches or dataCRC errors) and packets for which a FIFO overrun occurred are 'backed-out'. For packet-per-buffer mode, possible values are: ack_complete, ack_data_error, evt_long_packet, evt_overrun, evt_descriptor_read, evt_data_write and evt_unknown.

9.4.34 Isochronous Receive Context Command Pointer

The CommandPtr register specifies the address of the context program that will be executed when a DMA context is started. All descriptors are 16-byte aligned, so the four least-significant bits of any descriptor address must be zero. The four least-significant bits of the CommandPtr register are used to encode a Z value that indicates how many physically contiguous descriptors are pointed to by descriptorAddress. In buffer-fill mode, Z will be either one or zero. In packet-per-buffer mode, Z will be from zero to eight.

- CommandPtr register for Isochronous Receive Context 0
- CommandPtr register for Isochronous Receive Context 1
- CommandPtr register for Isochronous Receive Context 2
- CommandPtr register for Isochronous Receive Context 3

Register Name: IRCont0CommandPtr
Address Offset: 40Ch
Register Name: IRCont1CommandPtr
Address Offset: 42Ch
Register Name: IRCont2CommandPtr
Address Offset: 44Ch
Register Name: IRCont3CommandPtr
Address Offset: 46Ch



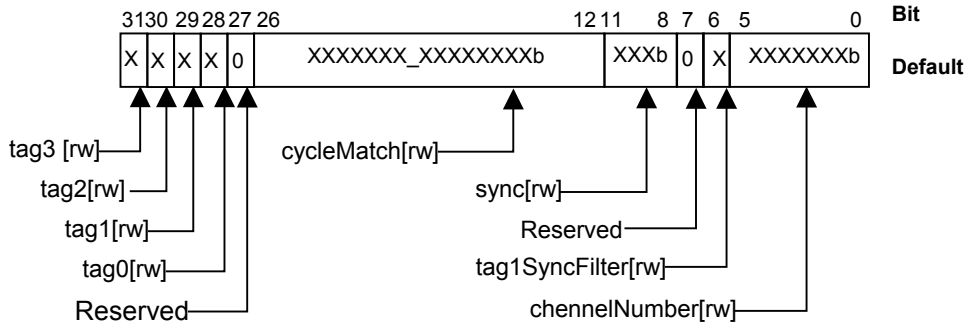
Bit	Field Name	Description
31-4	descriptorAddress	Contains the upper 28 bits of the address of a 16-byte aligned descriptor block.
3-0	z	Indicates the number of contiguous 16-byte aligned blocks at the address pointed to by descriptorAddress. If Z is 0, it indicates that the descriptorAddress is not valid.

9.4.35 Isochronous Receive Context Match Register

The IR ContextMatch register is used to start a context running on a specified cycle number, to filter incoming isochronous packets based on tag values and to wait for packets with a specified sync value. All packets are checked for a matching tag value, and a compare on sync is only performed when the descriptor's w field is set to 2'b11. This register should only be written when ContextControl.active is 0, otherwise unspecified behavior will result. At least one tag bit must be set to 1, otherwise no received packets will match and the context will, in effect, wait forever.

- ContextMatch register for Isochronous Receive Context 0
- ContextMatch register for Isochronous Receive Context 1
- ContextMatch register for Isochronous Receive Context 2
- ContextMatch register for Isochronous Receive Context 3

Register Name: IRCont0ContextMatch
Address Offset: 410h
Register Name: IRCont1ContextMatch
Address Offset: 430h
Register Name: IRCont2ContextMatch
Address Offset: 450h
Register Name: IRCont3ContextMatch
Address Offset: 470h



Bit	Field Name	Description
31	tag3	If set, this context will match on isochronous receive packets with a tag field of 2'b11.
30	tag2	If set, this context will match on isochronous receive packets with a tag field of 2'b10.
29	tag1	If set, this context will match on isochronous receive packets with a tag field of 2'b01.
28	tag0	If set, this context will match on isochronous receive packets with a tag field of 2'b00.
27	Reserved	This bit is reserved for future use and read-only. The default after reset is zero.
26-12	cycleMatch	Contains a 15-bit value, corresponding to the low order two bits of cycleSeconds and the 13-bit cycleCount field in the cycleStart packet. If ContextControl.cycleMatchEnable is set, then this IR DMA context will become enabled for receives when the two low order bits of the bus CycleTime.cycleSeconds and CycleTime.cycleCount values equal the cycleMatch value.
11-8	sync	This field contains the 4-bit field that is compared to the sync field of each isochronous packet for this channel when the command descriptor's w field is set to 2'b11.
7	Reserved	This bit is reserved for future use and read-only. The default after reset is zero.
6	tag1SyncFilter	If set and the contextMatch.tag1 bit is set, then packets with tag 2'b01 shall only be accepted into the context if the two most-significant bits of the packet's sync field are 2'b00. Packets with tag values other than 2'b01 shall be filtered according to the tag0, tag2 and tag3 bits above with no additional restrictions. If clear, this context will match on isochronous receive packets as specified in the tag0-3 bits above with no additional restrictions. On the OHCI 1.1, setting LinkControl.tag1SyncFilterLock to one sets this bit to one, and this bit is changed to read-only.
5-0	channelNumber	This six-bit field indicates the isochronous channel number for which this IR DMA context will accept packets.

10 ELECTRICAL CHARACTERISTICS

10.1 Absolute Maximum Rating

Symbol	Parameter	Range	Unit	Condition	Note
Vcc 1	Supply Voltage Range 1	-0.3 ~ 3.6	V	GND=0V	1
Vcc 2	Supply Voltage Range 2	-0.3 ~ 4.6	V	GND=0V	2
Vte 1	Voltage on Any Pin	-0.3 ~ 5.8	V	GND=0V	4
Vte 2	Voltage on Any Pin	-0.3 ~ 4.6	V	GND=0V	5
Topr	Ambient Temperature under bias	-40 ~ 85	C°		
Tstg	Storage Temperature Range	-55 ~ 125	C°		
ESD1	Human Body Model	±2.0	KV	C=100pF R=1.5KΩ	
ESD2	Charged Device Model	±1.0	KV		
LATUP	Latch-up	±100	mA	5ms	3

Note 1: Applied for VCC_CORE18V.
Note 2: Applied for VCC_3V, VCC_PCI3V, VCC_3V and AVCC_PHY3V.
Note 3: The clamping voltage of the trigger pulse power source should be below a value of Vte.
Note 4: All of Digital pins.
Note 5: IEEE1394 PHY Interface & IEEE1394 Control pins.

Note: Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

10.2 DC Characteristics

10.2.1 Recommended Operating Conditions for Power Supply

Power Pin	Parameter	Min	Typ	Max	Unit	Note
VCC_PCI3V	Supply Voltage for PCI interface (3.3V Operation)	3.0	3.3	3.6	V	
VCC_CORE18V	Supply Voltage for Core Logic (1.8V Operation)	1.65	1.8	1.95	V	
VCC_CORE18V	Supply Voltage for Core Logic (2.5V Operation)	2.3	2.5	2.7	V	
VCC_3V	Supply Voltage for System and Card Interface Signals	3.0	3.3	3.6	V	
AVCC_PHY3V	Supply Voltage for Cable interface block	3.0	3.3	3.6	V	

10.2.2 PCI Interface

For 3.3V signaling
(VCC_CORE18V= 1.65~1.95V or 2.3~2.7V, VCC_PCI3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
VIH	Input High Voltage	0.5VCC_PCI3V	5.75	V		1
VIL	Input Low Voltage	-0.5	0.3VCC_ PCI3V	V		1
VOH	Output High Voltage	0.9VCC_PCI3V		V	Iout=-500μA	1
VOL	Output Low Voltage		0.1VCC_ PCI3V	V	Iout=1500μA	1
IILk	Input Leakage Current		±10	μA	Vin=0~ VCC_PCI3V	1
Cin	Input Pin Capacitance		10	pF		1
Cclk	PCICLK Pin Capacitance		12	pF		1

Note 1: Applied for PCICLK, CLKRUN#, PCIRST#, AD [31:0], C/BE#[3:0], PAR, FRAME#, IRDY#, TRDY#,STOP#, DEVSEL#, IDSEL, PERR#, SERR#, REQ#, GNT#, INTA#, INTB# pins

10.2.3 16-bit PC Card Interface

For 3.3V signaling
(VCC_CORE18V= 1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition	Note
VIH	Input High Voltage	2.0		5.5	V		2
VIL	Input Low Voltage	-0.3		0.6	V		2
VOH1	Output High Voltage	2.4			V	Iout=-4mA	2
VOH2	Output High Voltage	2.4			V	Iout=-2mA	3
VOL1	Output Low Voltage			0.4	V	Iout=4mA	
VOL2	Output Low Voltage			0.4	V	Iout=2mA	3
IILk	Input Leakage Current			±10	μA	Vin=0~ VCC_3V	2
IIL1	Input Leakage Current (Pull-up)		-50		μA	Vin=0	4
Cin	Input Pin Capacitance			10	pF		2

Note 2: Applied for CADR [25:0], CDATA [15:0], CE [2:1]#, IOR#, IOW#, OE#, WE#, REG#, RDY/IREQ#, WAIT#, WP/IOIS16#, RESET, BVD1/STSCHG#/RI#, BVD2/SPKR#, INPACK# pins, if Card interface is configured as a 16-bit Card Socket.
Note 3: Applied for RESET pin
Note 4: Applied for RDY/IREQ#, WAIT#, BVD1/STSCHG#/RI#, BVD2/SPKR#, INPACK# pins

10.2.4 CardBus PC Card Interface

(VCC_CORE18V= 1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition	Note
VIH	Input High Voltage	0.475x VCC_3V		VCC_3V +0.5	V		6
VIL	Input Low Voltage	-0.5		0.325x VCC_3V	V		6
VOH	Output High Voltage	0.9VCC_3V			V	Iout=-150μA	6
VOL	Output Low Voltage			0.1VCC_3V	V	Iout=700μA	6
IILk	Input Leakage Current			±10	μA	Vin=0~VCC_3V	6
IIL1	Input Leakage Current (Pull-up)		-230		μA	Vin=0	7
Cin	Input Pin Capacitance			10	pF		6
IIL2	Input Leakage Current (Pull-down)		16.5		μA	Vin=VCC_3V	8
IIL3	Input Leakage Current (Pull-up)		-70		μA	Vin=0	9

Note 6: Applied for CCLK, CCLKRUN#, CRST#, CAD [31:0], CC/BE#[3:0], CPAR, CFRAME#, CIRDY#,CTRDY#,CSTOP#, CDEVSEL#, CPERR#, CSERR#, CREQ#, CGNT#, CINT#, CAUDIO, CSTSCHG pins, if Card interface is configured as a CardBus Card Socket.
Note 7: Applied for CIRDY#,CTRDY#,CSTOP#, CDEVSEL#, CPERR#, CSERR#, CREQ#, CINT#, CAUDIO pins
Note 8: Applied for CSTSCHG pin
Note 9: Applied for CCLKRUN# pin

10.2.5 PC Card Interface Card detect Pins and System Interface Pins

PC Card Interface Card Detect Pins and System Interface Pins
(VCC_CORE18V= 1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition	Note
VIH1	Input High Voltage	0.8VCC_3V		VCC_3V+0.3	V		10
VIL1	Input Low Voltage	-0.3		0.3VCC_3V	V		10
VIH2	Input High Voltage	2.4		VCC_3V+0.3	V		12
VIL2	Input Low Voltage	-0.3		0.8	V		12
VIH3	Input High Voltage	2.4		5.75	V		13
VIL3	Input Low Voltage	-0.3		0.8	V		13
VOH1	Output High Voltage	2.4			V	Iout=-4mA	11
VOH2	Output High Voltage	2.4			V	Iout=-1mA	12
VOL1	Output Low Voltage			0.4	V	Iout=4mA	11
VOL2	Output Low Voltage			0.4	V	Iout=1mA	12
IILk	Input Leakage Current			±10	μA	Vin=0~VCC_3V	12
IIL1	Input Leakage Current (Pull-up)		-80		μA	Vin=0	10
IOZ	Hi-Z Output Leakage Current			±10	μA	Vout=0~Vcc_3V	11

Note 10: Applied for CD1#(CCD1#), CD2#(CCD2#) pins
Note 11: Applied for RI_OUT#, SPKROUT#,VCC5EN#, VCC3EN#, VPPEN0, VPPEN1 pins
Note 12: Applied for VS1#(CVS1#), VS2#(CVS2#) pins
Note 13: Applied for GBRST#, HWSPND# pins

10.2.6 IRQ3-15 pin

For PCI 3.3V signaling
(VCC_CORE18V= 1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
VOH	Output High Voltage	2.4		V	Iout=-4mA	14
VOL	Output Low Voltage		0.4	V	Iout=4mA	14
IOZ	Hi-Z Output Leakage Current		±10	μA	Vout=0~VCC_3V	14
VIH	Input High Voltage	0.5VCC_3V	5.75	V		15
VIL	Input Low Voltage	-0.5	0.3VCC_3V	V		15
IILK	Input Leakage Current		±10	μA	Vin=0~VCC_3V	15

Note 14: Applied for IRQ3-15 pins
Note 15: Applied for IRQ3-9 and IRQ15 pins.

10.2.7 Cable Interface

(VCC_CORE18V= 1.65~1.95V or 2.3~2.7V, AVCC_PHY3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
VID	Differential Input Voltage	118	260	mV	Cable input, during data reception	16,17
		168	265	mV	Cable input, during arbitration	
VICM	TpB Common Mode Input Voltage	1.165	2.515	V	100Mbps speed signaling off	17
		0.935	2.515	V	200Mbps speed signaling	
		0.523	2.515	V	400Mbps speed signaling	
VOD	Differential Output Voltage	172	265	mV	Cable output, load 56Ω	16,17
ICM	TpA, TpB Common Mode Output Current	-0.81	0.44	mA	Driver enable, speed signal off	16,17
ISPD2	TpB200Mbps Speed Signal	-4.81	-2.53	mA		17
ISPD4	TpB400Mbps Speed Signal	-12.40	-8.10	mA		17
VTCPWD	CPS Threshold Voltage		7.5	V	CPS, R=390KΩ	19
VTPBIAS	TpBias Output Voltage	1.665	2.015	V		18

Note 16: Applied for TPAP0, TPAP1, TPAN0, TPAN1 pins
Note 17: Applied for TPBP0, TPBP1, TPBN0, TPBN1 pins
Note 18: Applied for TPBIAS0, TPBIAS1 pins
Note 19: Applied for CPS pin

10.2.8 Serial ROM Interface

For 3.3V signaling
(VCC_CORE18V= 1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
VIL	Input Low Voltage	-0.5	0.3VCC_3V	V		20
VIH	Input High Voltage	0.7VCC_3V	VCC_3V+0.5	V		20
VOL1	Output Low Voltage	0	0.4	V	Iout=3mA	20
Tof	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance from 10 pF to 400 pF:	-	250	ns	with up to 3 mA sink current at V_{OL1}	20
I_I	Input current each I/O pin		±10	μA	Vin=0.4~0.9VCC_3V	20
Cin	Input Pin Capacitance		10	pF		20

Notes 20: IRQ12, 14 (On use of SROM)

10.2.9 Power Consumption

Power Supply Current

Power Pin	Parameter	Min	Typ	Max	Unit	Condition	Notes
Iccstd	Power Supply Current, Standby			200	μA	fclk(PCICLK)=0 Vin=0 or Vcc PHY Sleep Mode	21
Iccsusp	Power Supply Current, Hardware Suspend Mode			200	μA	Mode = H/W Bridge Suspend PHY Sleep Mode VCC_3V=3.6V VCC_PCI3V=0V VCC_CORE18V=2.7V AVCC_PHY3V=3.6V Vin=0 or Vcc	17
Icc	Power Supply Current, Operating			150	mA	PCICLK=33MHz VCC_3V=3.6V VCC_PCI3V=3.6V VCC_CORE18V=2.7V fclk(XIO)=24.576MHz AVCC_PHY3V=3.6V Vin=0 or Vcc	
				130	mA	PCICLK=33MHz VCC_3V=3.6V VCC_PCI3V=3.6V VCC_CORE18V=1.95V fclk(XIO)=24.576MHz AVCC_PHY3V=3.6V Vin=0 or Vcc	

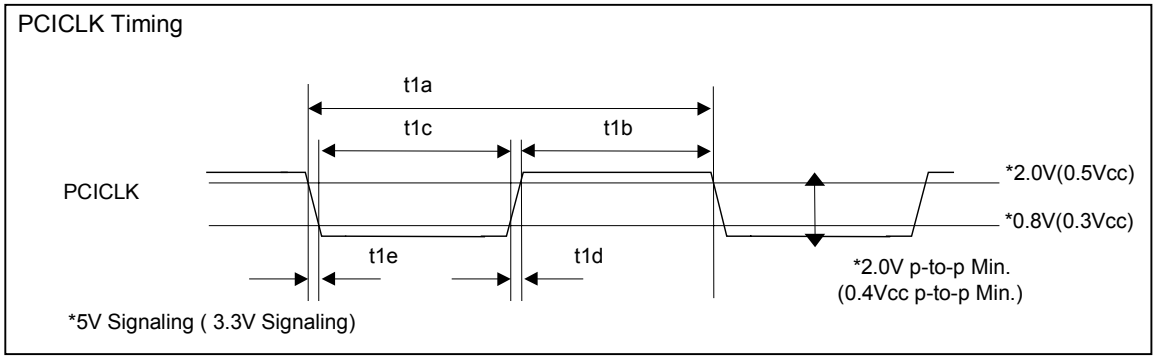
Notes 21: Disable the function of PLL and Oscillator.
(See: 4.11.2 Function on 1394 OHCI-LINK/1394 PHY)

10.3 AC Characteristics

10.3.1 PCI Interface Signals

PCI Clock
(VCC_CORE18V= 1.65~1.95V or 2.3~2.7V, VCC_PCI3V=3.0~3.6V, Ta=0~70ºC)

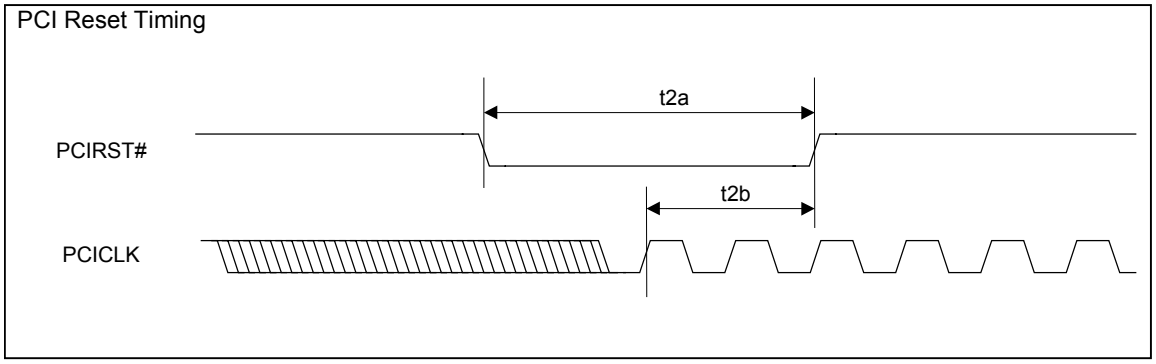
Symbol	Parameter	Min	Max	Unit	Notes
	PCICLK				
t1a	Cycle Time, PCICLK	30		ns	
t1b	Pulse Width Duration, PCICLK High	11		ns	
t1c	Pulse Width Duration, PCICLK Low	11		ns	
t1d	Slew Rate, PCICLK Rising Edge	1	4	V/ns	
t1e	Slew Rate, PCICLK Falling Edge	1	4	V/ns	



PCICLK Timing

PCI Reset
(VCC_CORE18V= 1.65~1.95V or 2.3~2.7V, VCC_PCI3V=3.0~3.6V, Ta=0~70ºC)

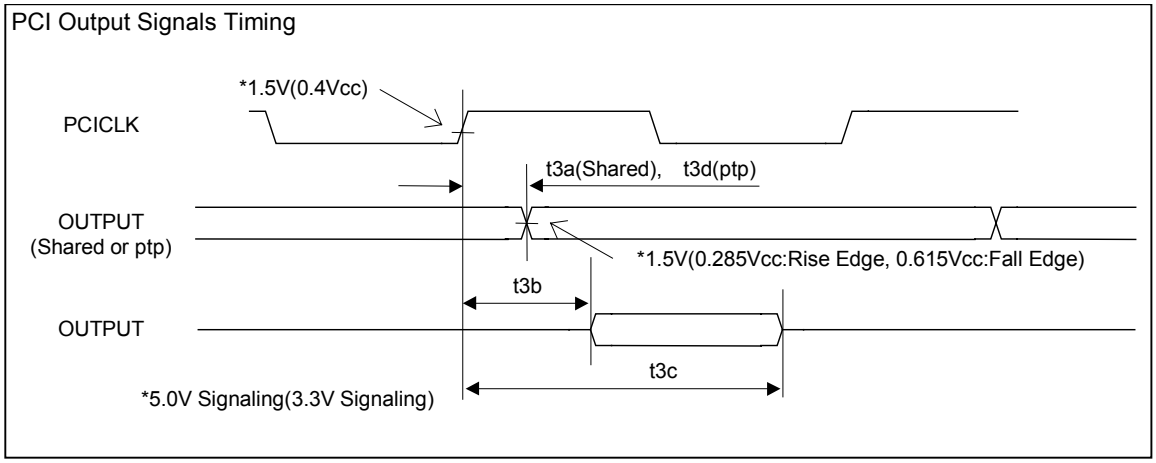
Symbol	Parameter	Min	Max	Unit	Notes
	PCIRST#				
t2a	Pulse Duration, PCIRST#	1		ms	
t2b	Setup Time, PCICLK active at PCIRST# Negation	100		µs	



PCI Reset Timing

PCI Interface Output Signals
(VCC_CORE18V= 1.65~1.95V or 2.3~2.7V, VCC_PCI3V=3.0~3.6V, Ta=0~70ºC)

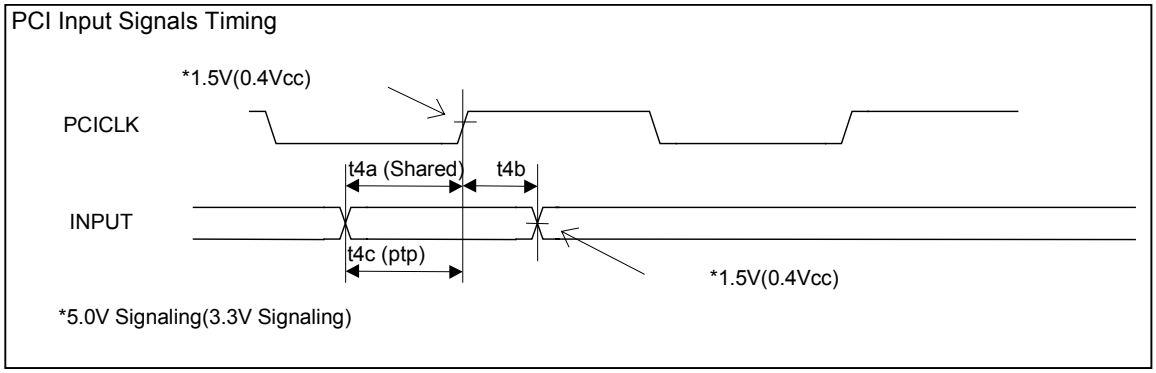
Symbol	Parameter	Min	Max	Unit	Notes
	AD [31:0], C/BE#[3:0], PAR, FRAME#, DEVSEL#, IRDY#, TRDY#, STOP#, PERR#, SERR#, CLKRUN#				
t3a	Shared Signal Valid delay time from PCICLK	2	11	ns	Min: CL=0 pF Max: CL=50 pF (10 pF 3.3v)
t3b	Enable Time, Hi-Z to active delay from PCICLK	2		ns	
t3c	Disable Time, Active to Hi-Z delay from PCICLK		28	ns	
	REQ#				
t3d	Point to Point Signal Valid delay time from PCICLK	2	12	ns	Min: CL=0 pF Max: CL=50 pF (10 pF 3.3v)



PCI Output Signals Timing

PCI Interface Input Signals
(VCC_CORE18V= 1.65~1.95V or 2.3~2.7V, VCC_PCI3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Max	Unit	Notes
	CAD [31:0], C/BE#[3:0], PAR, FRAME#, DEVSEL#, IRDY#, TRDY#, STOP#, IDSEL, PERR#, SERR#, CLKRUN#				
t4a	Setup Time, Shared Signal Valid before PCICLK	7		ns	
t4b	Hold Time, Shared Signal Hold Time after PCICLK High	0		ns	
	GNT#				
t4c	Setup Time, Point to Point Signal Valid before PCICLK	10		ns	



PCI Input Signals Timing

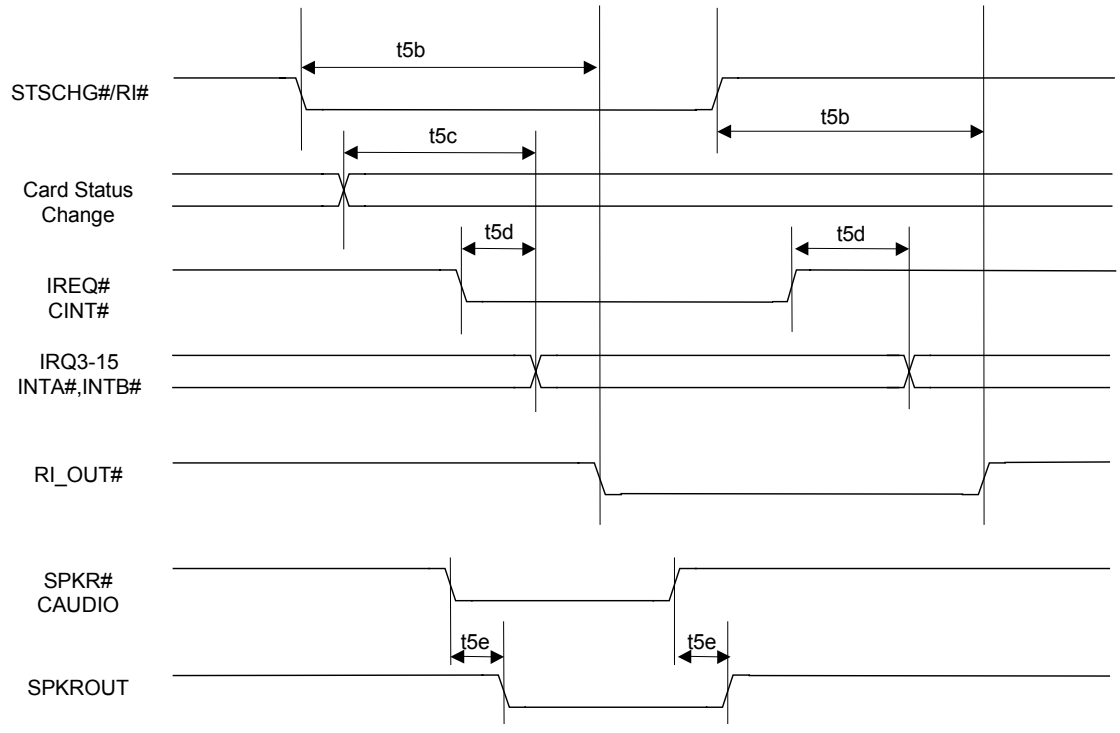
10.3.2 System Interface Signals

System Interface Signals AC Characteristics
(VCC_CORE18V= 1.65~1.95V or 2.3~2.7V, VCC_PCI3V=3.0~3.6V, VCC_3V= 3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Max	Unit	Notes
	RI_OUT#, IRQ3-15, INTA#, INTB#				
t5b	RI# to RI_OUT# Delay		50	ns	
t5c	Card Status Change to IRQ3-15/INTA#, INTB# Delay		2Tcyc+0	ns	1
t5d	Card IREQ#/CINT# to IRQ3-15/INTA#, INTB# Delay		50	ns	
	SPKROUT				
t5e	SPKR#/CAUDIO to SPKROUT Delay		50	ns	

Note1: Tcyc is PCICLK cycle time. (Typically 30ns)

System Signals Timing



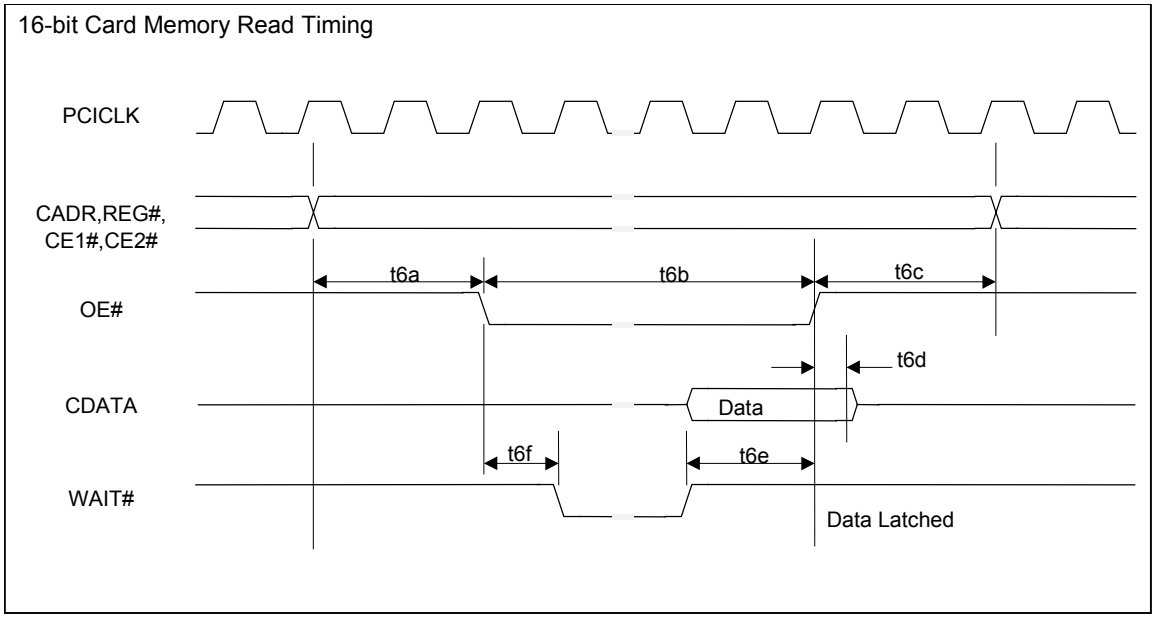
System Signals Timing

10.3.3 16-bit PC Card Interface Signals

Memory Read
(VCC_CORE18V= 1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Max	Unit	Notes
	CADR [25:0], REG#, CE [2:1]#				
t6a	Setup Time, CADR [25:0], REG# and CE [2:1]# before OE# Low	Tsu-20		ns	1,2 Tsu=1~7Tcyc Programmable
t6c	Hold Time, CADR [25:0], REG# and CE [2:1]# after OE# High	Thl-10		ns	1,2 Thl=1~7Tcyc Programmable
	OE#				
t6b	Pulse Duration, OE# Low	Tpw-20		ns	1,2 Tpw=3~31Tcyc Programmable
	CDATA [15:0]				
t6d	Hold Time, CDATA [15:0] after OE# High	0		ns	
	WAIT#				
t6e	Hold Time, OE# Low after WAIT# High	1Tcyc+0		ns	1
t6f	Valid Delay, OE# Low to WAIT# Low		50	ns	

Note1: Tcyc is PCICLK cycle time. (Typically 30ns)
Note2: Tsu, Tpw, Thl can be programmed by setting 16-bit Memory Timing 0 register.

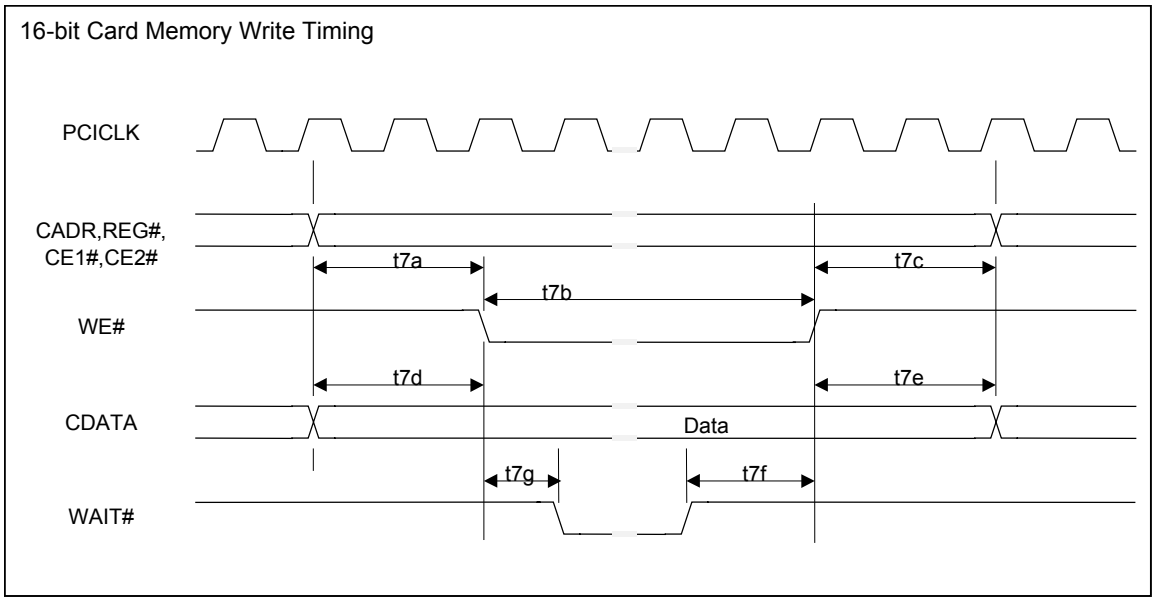


16-bit Card Memory Read Timing

Memory Write
(VCC_CORE18V= 1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Max	Unit	Notes
	CADR [25:0], REG#, CE [2:1]#				
t7a	Setup Time, CADR [25:0], REG# and CE [2:1]# before WE# Low	Tsu-20		ns	1,2 Tsu=1~7Tcyc Programmable
t7c	Hold Time, CADR [25:0], REG# and CE [2:1]# after WE# High	Thl-10		ns	1,2 Thl=1~7Tcyc Programmable
	WE#				
t7b	Pulse Duration, WE# Low	Tpw-20		ns	1,2 Tpw=3~31Tcyc Programmable
	CDATA [15:0]				
t7d	Setup Time, CDATA [15:0] before WE# Low	Tsu-20		ns	1,2 Tsu=1~7Tcyc Programmable
t7e	Hold Time, CDATA [15:0] after WE# High	Thl-10		ns	1,2 Thl=1~7Tcyc Programmable
	WAIT#				
t7f	Hold Time, WE# Low after WAIT# High	Tcyc+0		ns	1
t7g	Valid Delay, WE# Low to WAIT# Low		50	ns	

Note1: Tcyc is PCICLK cycle time. (Typically 30ns)
Note2: Tsu, Tpw, Thl can be programmed by setting 16-bit Memory Timing 0 register.

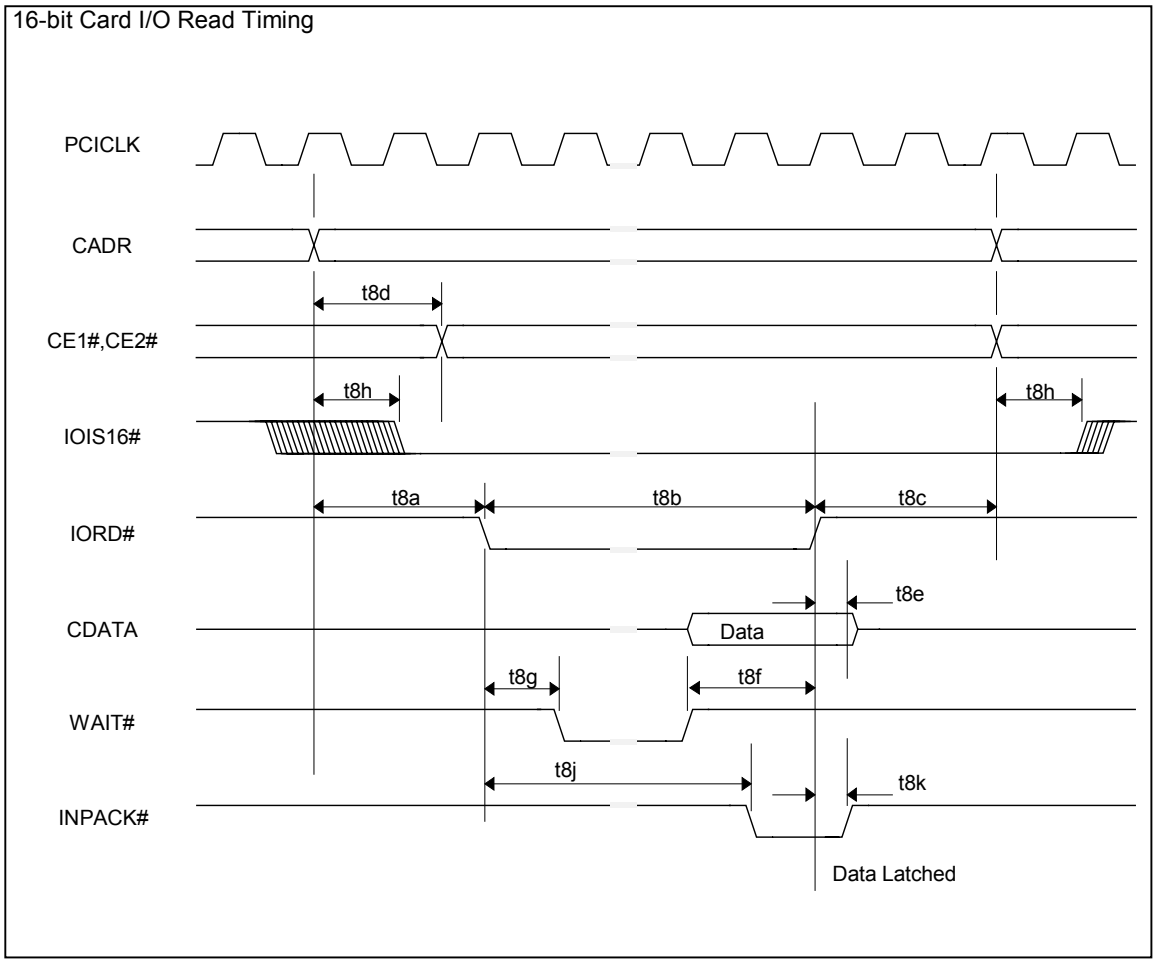


16-bit Card Memory Write Timing

I/O Read
(VCC_CORE18V= 1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Max	Unit	Notes
	CADR [25:0], REG#				
t8a	Setup Time, CADR [25:0] and REG# before IORD# Low	Tsu-20		ns	1,3 Tsu=2~7Tcyc Programmable
t8c	Hold Time, CADR [25:0] and REG# after IORD # High	Thl-10		ns	1,3 Thl=1~7Tcyc Programmable
	IORD#				
t8b	Pulse Duration, IORD # Low	Tpw-20		ns	1,3 Tpw=3~31Tcyc Programmable
	CE [2:1]#				
t8d	Valid Delay, CADR [15:0] and REG# to CE [2:1]#	1Tcyc-10		ns	1
	CDATA [15:0]				
t8e	Hold Time, CDATA [15:0] after IORD # High	0		ns	
	WAIT#				
t8f	Hold Time, IORD # Low after WAIT# High	1Tcyc+0		ns	1
t8g	Valid Delay, IORD # Low to WAIT# Low		50	ns	
	IOIS16#				
t8h	Valid Delay, CADR [25:0] to IOIS16# Low		50	ns	
	INPACK#				
t8k	Hold Time, INPCK# Low after IORD# High	0		ns	
t8j	Valid Delay, IORD # Low to INPACK# Low		50	ns	

Note1: Tcyc is PCICLK cycle time. (Typically 30ns)
Note3: Tsu, Tpw, Thl can be programmed by setting 16-bit I/O Timing 0 register.

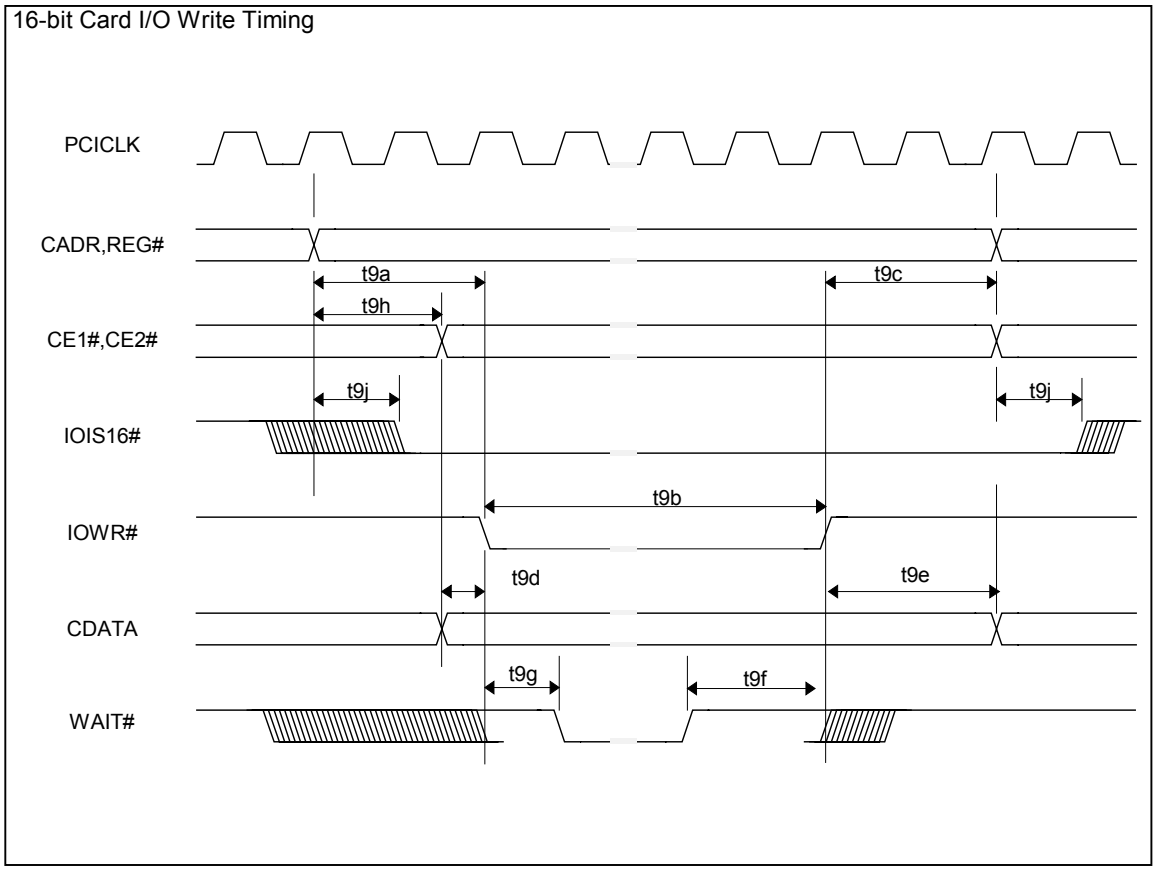


16-bit Card I/O Read Timing

I/O Write
(VCC_CORE18V= 1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Max	Unit	Notes
	CADR [25:0], REG#				
t9a	Setup Time, CADR [25:0] and REG# before IOWR # Low	Tsu-20		Ns	1,3 Tsu=2~7Tcyc Programmable
T9c	Hold Time, CADR[25:0], REG# and CE[2:1]# after IOWR # High	Thl-10		Ns	1,3 Thl=1~7Tcyc Programmable
	IOWR#				
T9b	Pulse Duration, IOWR# Low	Tpw-20		Ns	1,3 Tpw=3~31Tcyc Programmable
	CE[2:1]#				
T9h	Valid Delay, CADR [15:0] and REG# to CE [2:1]#	1Tcyc-10		ns	1
	CDATA [15:0]				
t9d	Setup Time, CDATA [15:0] before IOWR # Low	Tsu-2Tcyc-10		ns	1,3 Tsu=3~7Tcyc Programmable
t9e	Hold Time, CDATA [15:0] after IOWR # High	Thl-10		ns	1,3 Thl=1~7Tcyc Programmable
	WAIT#				
t9f	Hold Time, IOWR # Low after WAIT# High	1Tcyc+0		ns	3
t9g	Valid Delay, IOWR # Low to WAIT# Low		50	ns	
	IOIS16#				
t9j	Valid Delay, CADR [25:0] and REG# to IOIS16# Low		50	ns	

Note1: Tcyc is PCICLK cycle time. (Typically 30ns)
Note3: Tsu, Tpw, Thl can be programmed by setting 16-bit I/O Timing 0 register.



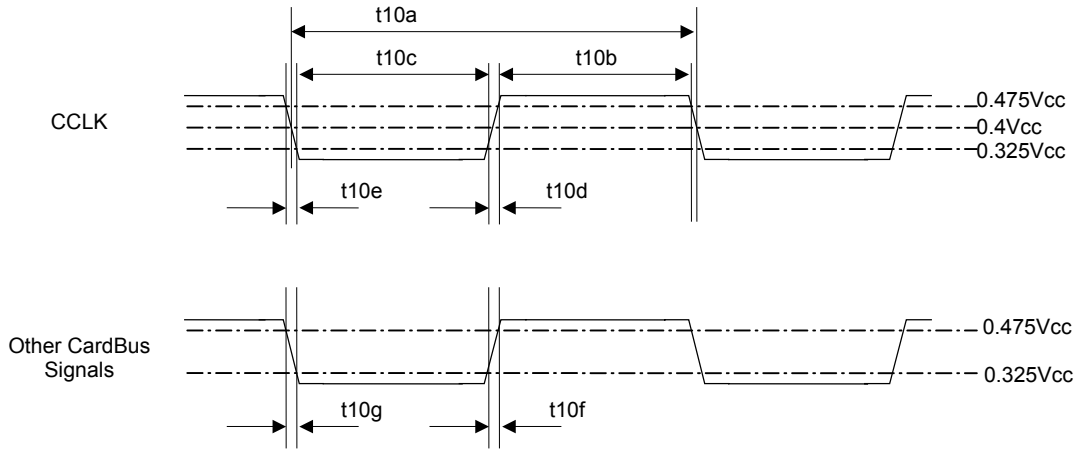
16-bit Card I/O Write Timing

10.3.4 CardBus PC Card Interface Signals

Clock and Signal Slew Rate
(VCC_CORE18V= 1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Max	Unit	Notes
	CCLK				
t10a	Cycle Time, CCLK	30		ns	
t10b	Pulse Width Duration, CCLK High	12		ns	
t10c	Pulse Width Duration, CCLK Low	12		ns	
t10d	Slew Rate, CCLK Rising Edge	1	4	V/ns	
t10e	Slew Rate, CCLK Falling Edge	1	4	V/ns	
	Other CardBus Signals				
t10f	Slew Rate, Rising Edge	0.25	1	V/ns	
t10g	Slew Rate, Falling Edge	0.25	1	V/ns	

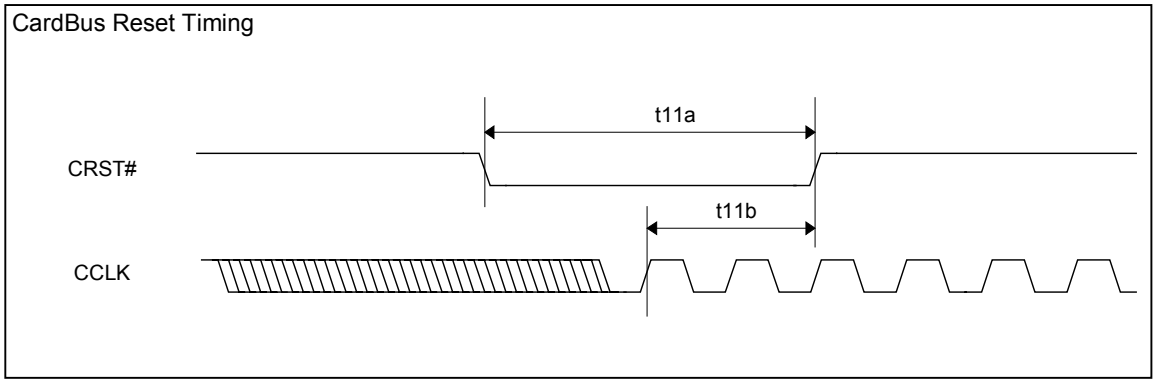
CCLK Timing and CardBus Signals Slew Rate



CCLK Timing and CardBus Slew Rate

Card Reset
(VCC_CORE18V= 1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Max	Unit	Notes
	CRST#				
t11a	Pulse Duration, CRST#	1		ms	
t11b	Setup Time, CCLK active at CRST# Negation	100		µs	

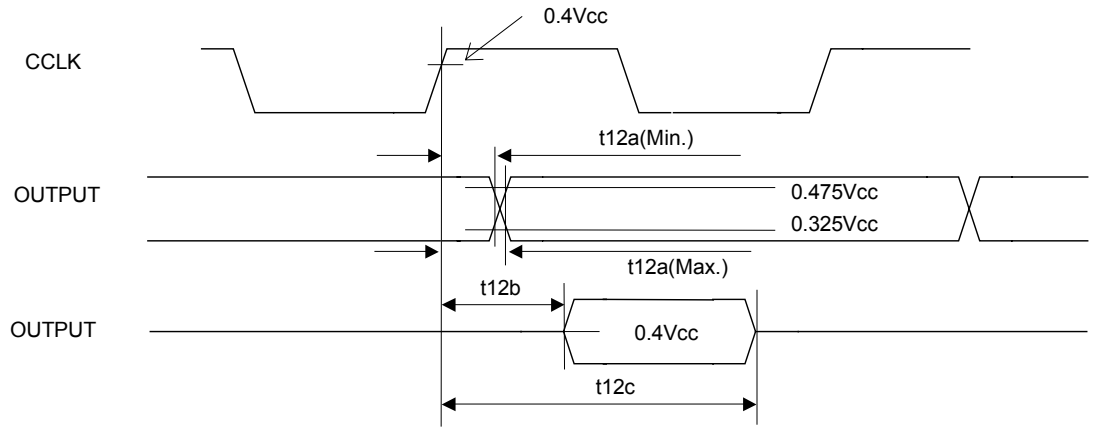


CardBus Reset Timing

Card Output
(VCC_CORE18V= 1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Max	Unit	Notes
	CAD [31:0], CC/BE#[3:0], CPAR, CFRAME#, CDEVSEL#, CIRDY#, CTRDY#, CSTOP#, CPERR#, CSERR#, CCLKRUN#, CGNT#				
t12a	Valid delay time from CCLK	2	18	ns	Min: CL=0 pF Max: CL=30 pF
t12b	Enable Time, Hi-Z to active delay from CCLK	2		ns	
t12c	Disable Time, Active to Hi-Z delay from CCLK		28	ns	

CardBus Interface Output Signals Timing

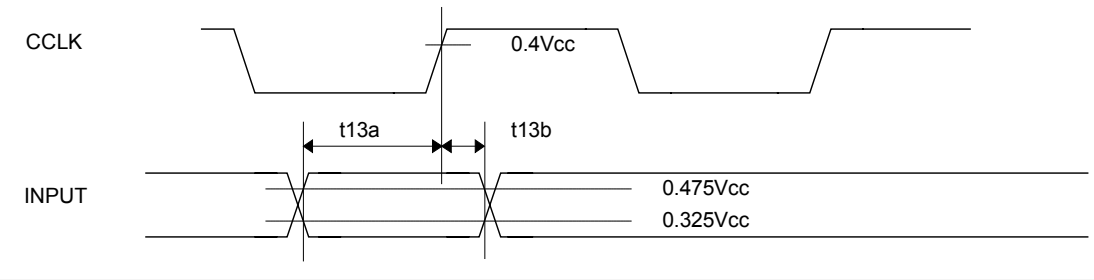


CardBus Interface Output Signals Timing

Card Input
(VCC_CORE18V=1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Max	Unit	Notes
	CAD [31:0], CC/BE#[3:0], CPAR, CFRAME#, CDEVSEL#, CIRDY#, CTRDY#, CSTOP#, CPERR#, CSERR#, CCLKRUN#, CREQ#				
t13a	Setup Time, Signal Valid before CCLK	7		ns	
t13b	Hold Time, Signal Hold Time after CCLK High	0		ns	

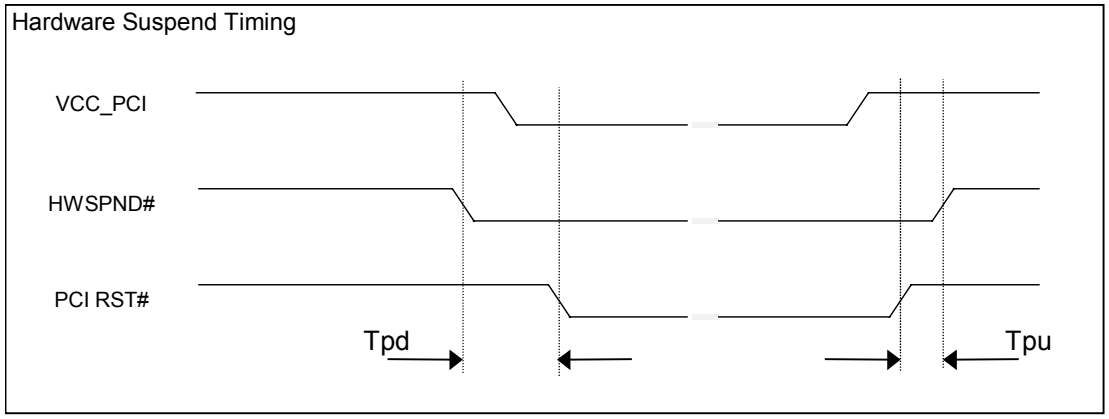
CardBus Interface Input Signals Timing



CardBus Input Signals Timing

10.3.5 Hardware Suspend mode

Timing chart for keeping the value of the internal register on the Suspend mode.

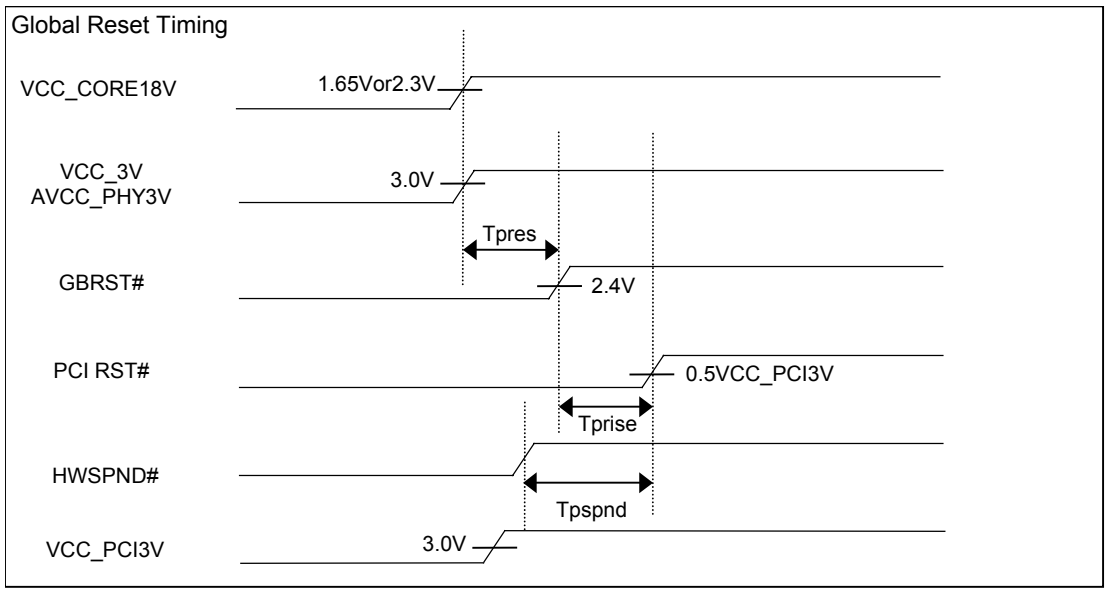


Symbol	Parameter	Min	Typ	Max	Unit
Tpd	HWSPND# to PCIRST# delay	100*1			ns
Tpu	PCIRST# Setup time to HWSPND#	100*1			ns

*1 : PCICLK=33MHz

10.3.6 Global Reset Signals

Timing chart for initializing the internal register on the Power's on.



Symbol	Parameter	Min	Typ	Max	Unit
Tpres	Power_On to GBRST# delay	1		100	ms
Tprise	GBRST# to PCIRST# delay	60*2			ns
Tpspnd	HWSPND# to PCIRST# delay	100*2			ns

*2 : PCICLK=33MHz

10.3.7 Cable Interface Signal

(VCC_CORE18V= 1.65~1.95V or 2.3~2.7V, AVCC_PHY3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Max	Unit	Notes
TTJITTER	TpA, TpB transfer jitter		±0.15	ns	
TTSKEW	TpA, Strobe, TpB Data transfer skew		±0.10	ns	
TTRF	TpA, TpB transfer Rise and Fall	0.5	1.2	ns	10% to 90% At 1394 connector

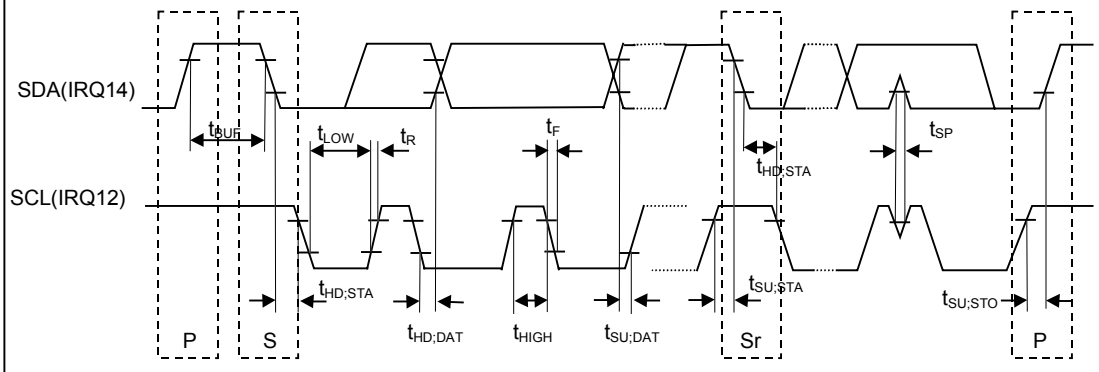
10.3.8 Serial ROM Interface Signals

SDA (IRQ14),SCL(IRQ12)
(VCC_CORE18V= 1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70ºC)

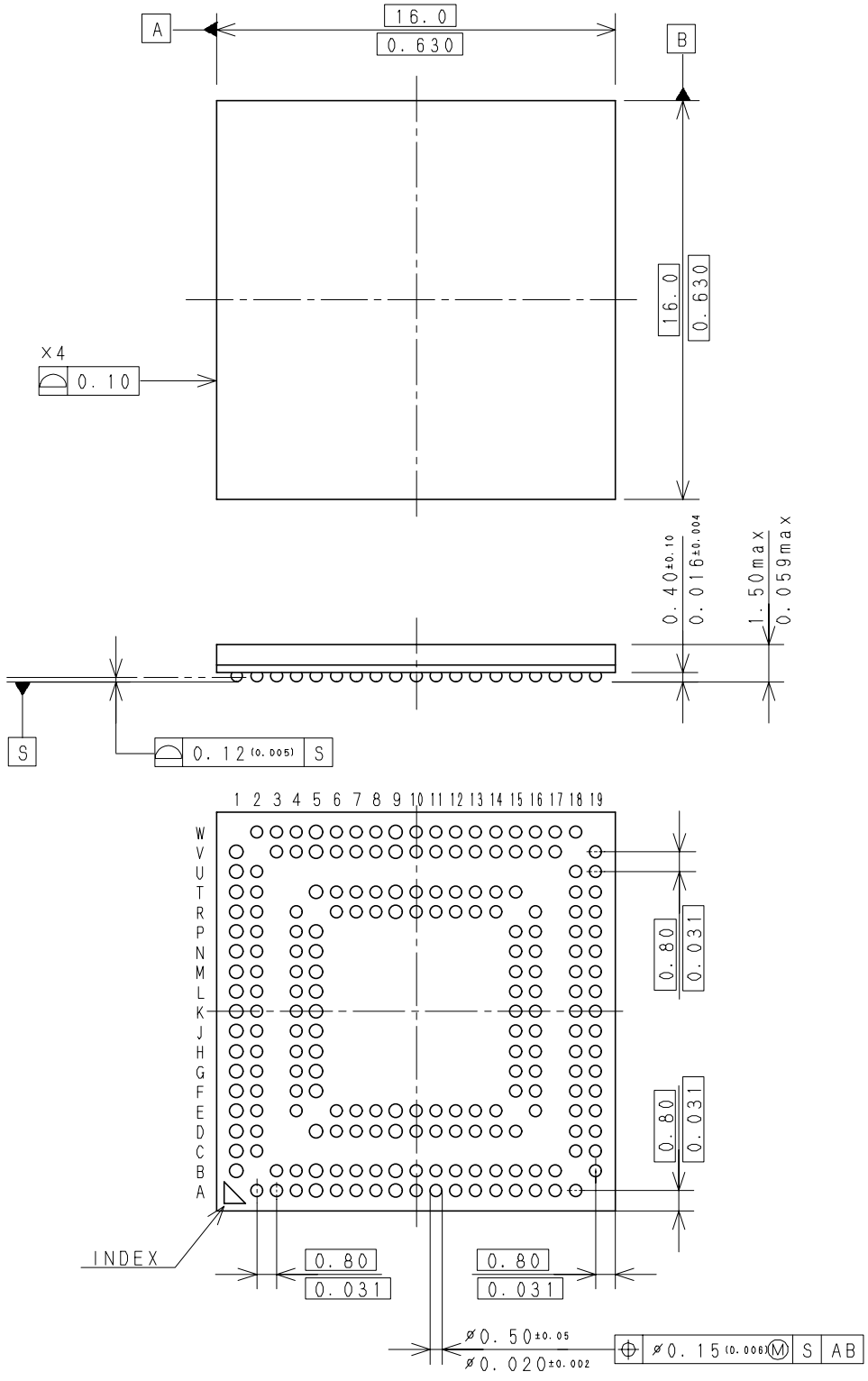
Symbol	Parameter	Min	Max	Unit	Notes
	SDA (IRQ14), SCL (IRQ12)				
f SCL	SCL clock frequency	0	100	kHz	
t BUF	Bus free time between a STOP and START condition	4.7	-	us	
t HD;STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	-	us	
t LOW	LOW period of the SCL clock	4.7	-	us	
t HIGH	HIGH period of the SCL clock	4.0	-	us	
t SU;STA	Set–up time for a repeated START condition	4.7	-	us	
t HD;DAT	Data hold time for I 2 C–bus devices	0		us	
t SU;DAT	Data set–up time	250	-	ns	
t R	Rise time of both SDA and SCL signals	-	1000	ns	
t F	Fall time of both SDA and SCL signals	-	300	ns	
t SU;STO	Set–up time for STOP condition	4.0	-	us	
t sp	Pulse width of spikes which must be suppressed by the input filter	n/a	n/a	ns	
C b	Capacitive load for each bus line	-	400	pF	

All values referred to V IHmin and V ILmax levels (see 10.2.8).

Serial ROM if SDA,SCL timing



PACKAGE CODE	CSP-208-P2 (1616)



UNIT: mm / inch

	· ·		
C	01·03·12	TERMINAL POSITION TOLERANCE (0.15→ø0.15)	R.TOKUYAMA
	· ·	ADDITION OF TOLERANCE	R.TOKUYAMA
B	01·03·06	(TERMINAL POSITION & PACKAGE EDGE)	
	DATE	CHANGE NOTICE	SIGN

DIMENSIONAL TOLERANCE (±)						
DIMENSION X	0	1	2	3	4	5
X ≤ 4	0.05	0.1	0.1	0.1	0.2	0.5
4< X ≤ 16	0.05	0.1	0.1	0.2	0.3	0.8
16< X ≤ 63	0.05	0.1	0.2	0.3	0.5	1.2
63< X ≤ 250	0.1	0.2	0.3	0.5	0.8	1.8
250< X ≤1000		0.3	0.5	0.8	1.2	3.0
1000< X ≤4000			0.8	1.2	1.8	5.0

SPECIFIED GRADE / VISUAL GRADE

ANGLE TOL ±

SCALE NTS

DRAW UP DATE 2000·2·16

PART NAME CSP-208PIN(P2) PACKAGE OUTLINE

APPROVED BY	CHECKED BY	DESIGNED BY	DRAWN BY
T. KAWAKAMI	T. SEIGENJI	M. HIGASHIGUCHI	R. TOKUYAMA

PART NO. DF-208CSP-002 C

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