R5C485

PCI-CARDBUS BRIDGE

DATA SHEET

REV. 1.00

RICOH

REVISION HISTORY

REVISION	DATE	COMMENTS
0.95	3/18/02	First Draft for internal use.
1.00	5/1/02	First public release.

1 OVERVIEW

The R5C485 is the single chip solution offering single PCI bus-PC Card bridge. The R5C485 is compliant with the latest specification in both PC card.
The R5C485 has one PCI function compliant and single PC Card interface.
The PC Card controller of the R5C485 is compliant with PC Card Standard Release 8.0. The R5C485 provides features that make it the best choice for bridging between the PCI bus and PC Cards, and supports any combination of 16-bit (Card-16), and CardBus (Card-32) PC Cards in one socket, powered at 5V or 3.3V, as required.
The R5C485 is compliant with the latest PCI Bus Power Management Specification, and provides several low-power modes that enable the host power system to further reduce power consumption.

- ◆ PC98/99/2001 compliant
  - PC2001 Design Guide compliant (Subsystem ID, Subsystem Vender ID)
  - ACPI and PCI Bus Power Management 1.1 compliant
  - Supports Global Reset

- ◆ Low Power consumption
  - Power decreased by the improvement of Power Management supply on the operation
  - Software Suspend mode compliant with ACPI
  - Hardware Suspend
  - Supports CLKRUN# and CCLKRUN#
  - Powered at 1.8V/2.5V for core logic and 3.3V for others.

- ◆ Single Chip PCI-CardBus Bridge
  - Supports 1 PC Card Socket
  - Supports CardBus(Card-32) Card and 16-bit(PCMCIA2.1/JEIDA4.2) Card
  - Bridge function between PCI bus and CardBus

- ◆ PCI Bus Interface
  - Compliant with PCI Local Bus Specification2.2
  - The maximum frequency 33MHz
  - Supports PCI Master/Target protocol
  - Direct connection to PCI bus
  - 3.3V interface (5V tolerant)

- ◆ CardBus PC card Bridge
  - Compliant with PC Card Standard Release 8.0 Specification
  - The maximum frequency 33MHz
  - Supports CardBus Master/Target protocol
  - Transfer transactions
    - All memory read/write transaction(bi-direction)
    - I/O read/write transaction(bi-direction)
    - Configuration read/write transaction(PCI → Card)
    - 2 programmable memory windows
    - 2 programmable I/O windows

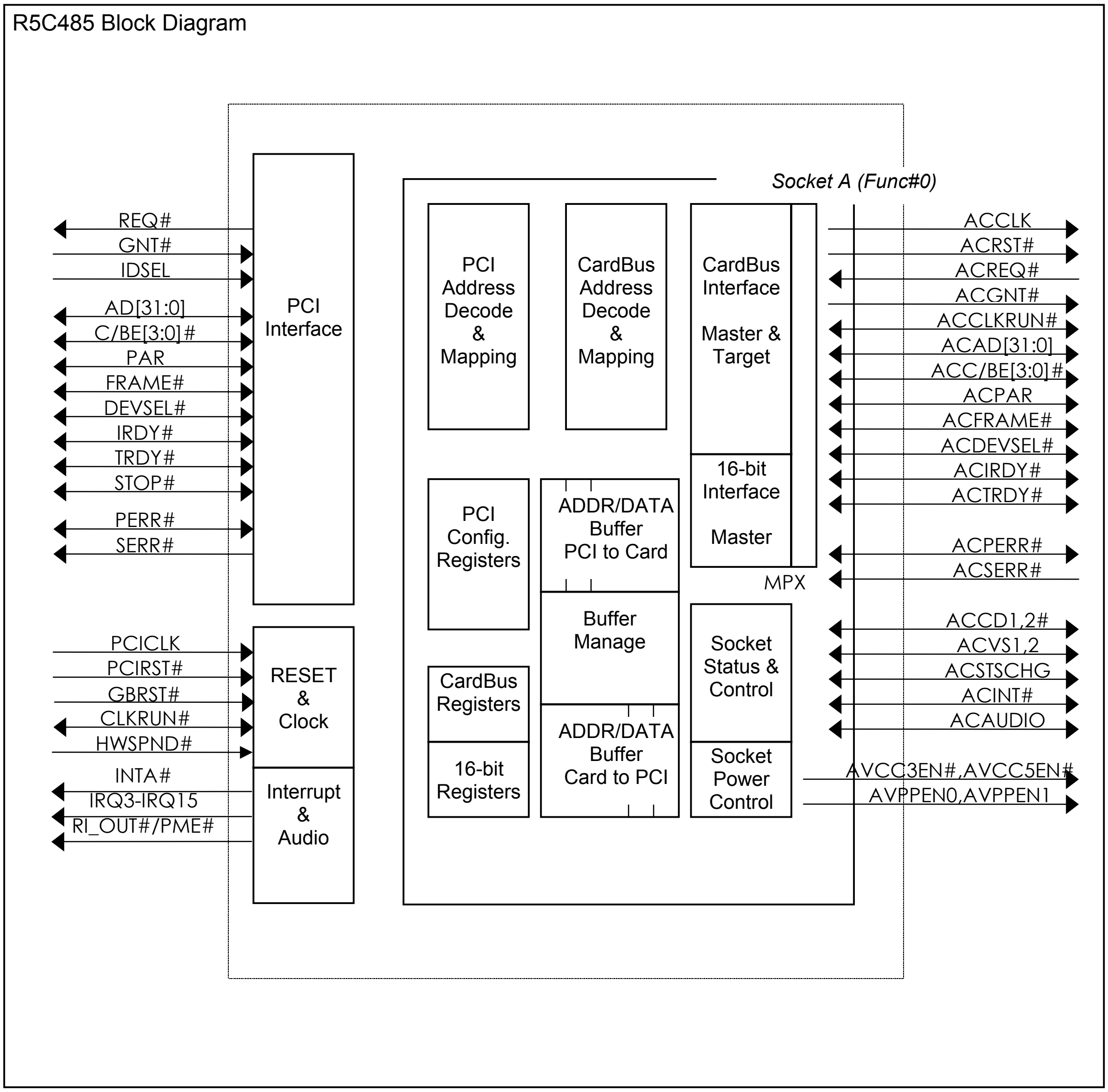
- ◆ PC Card-16 Bridge
  - Compliant with PC Card Standard Release 8.0 Specification
  - 5 programmable memory windows
  - 2 programmable I/O windows
  - Compliant with i82365SL compatible register set / ExCA

- System Interrupt
  - INTA# support for PCI system interrupt
  - IRQx support for ISA system interrupt (Non shared IRQx pins)
  - Supports Serialized IRQ
  - Supports Remote WakeUp by CSTSCHG

- Supports GPIO
- Supports Plug and Play
- Supports Posting Write and Prefetching Read for PC Card bridge
- Supports 16-bit Legacy mode (3E0/3E2 I/O port)
- Supports Zoomed Video Port
  - Bypass type

- Supports PC Card LED
- Pin Compatible with R5C551(CSP1616-208)
- Package
  - 144pin LQFP (size=20x20mm, pitch=0.5mm, t=1.7mm)
  - 208pin CSP (size=16x16mm, pitch=0.8mm, t=1.5mm)

2 BLOCK DIAGRAM

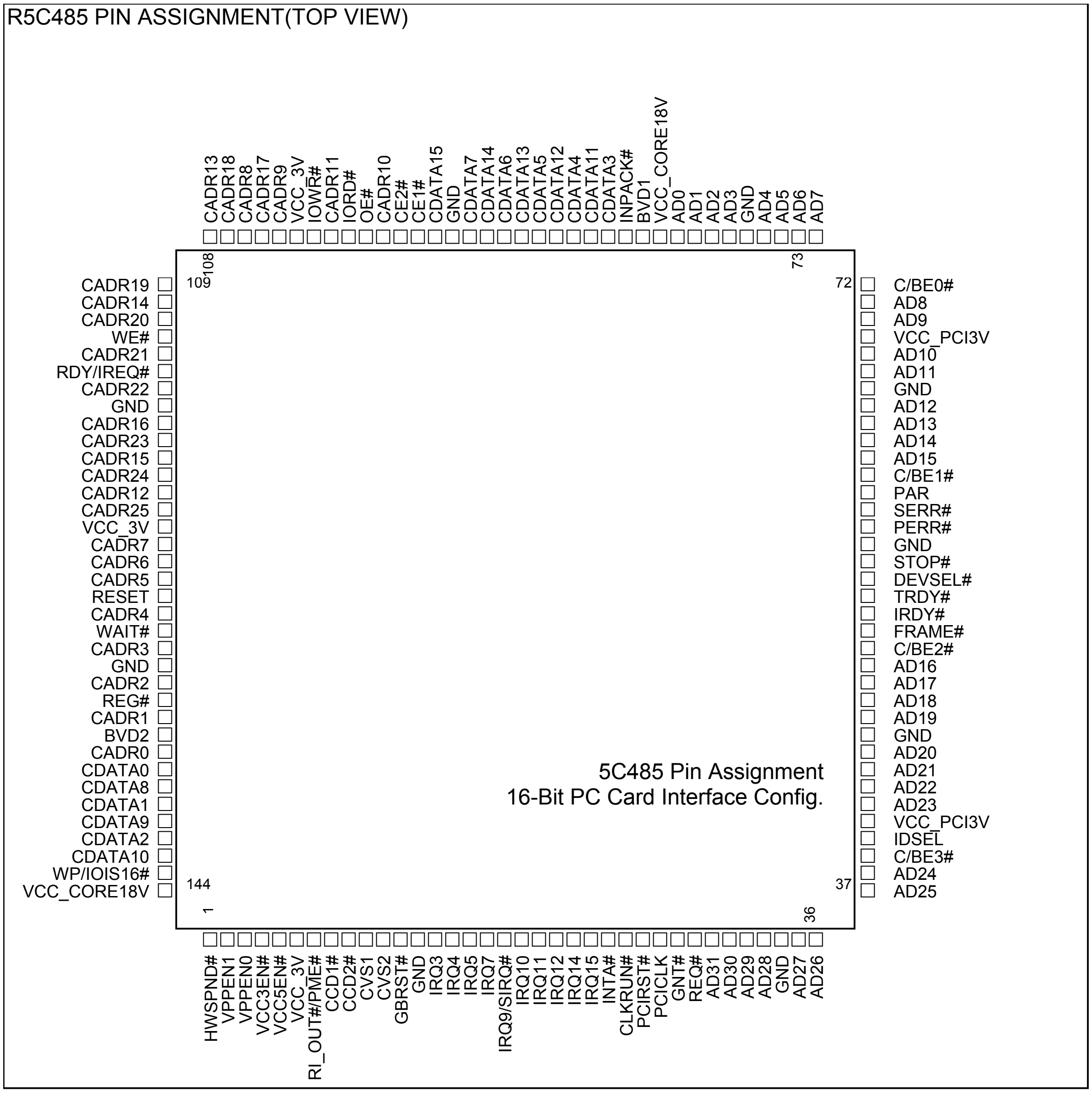

R5C485 Block Diagram
REQ#
GNT#
IDSEL
AD[31:0]
C/BE[3:0]#
PAR
FRAME#
DEVSEL#
IRDY#
TRDY#
STOP#
PERR#
SERR#
PCICLK
PCIRST#
GBRST#
CLKRUN#
HWSPND#
INTA#
IRQ3-IRQ15
RI_OUT#/PME#
PCI Interface
RESET & Clock
Interrupt & Audio
Socket A (Func#0)
PCI Address Decode & Mapping
CardBus Address Decode & Mapping
CardBus Interface Master & Target
16-bit Interface Master
MPX
PCI Config. Registers
ADDR/DATA Buffer PCI to Card
Buffer Manage
ADDR/DATA Buffer Card to PCI
CardBus Registers
16-bit Registers
Socket Status & Control
Socket Power Control
ACCLK
ACRST#
ACREQ#
ACGNT#
ACCLKRUN#
ACAD[31:0]
ACC/BE[3:0]#
ACPAR
ACFRAME#
ACDEVSEL#
ACIRDY#
ACTRDY#
ACPERR#
ACSERR#
ACCD1,2#
ACVS1,2
ACSTSCHG
ACINT#
ACAUDIO
AVCC3EN#,AVCC5EN#
AVPPEN0,AVPPEN1

3 PIN DESCRIPTION

3.1 Pin Assignments

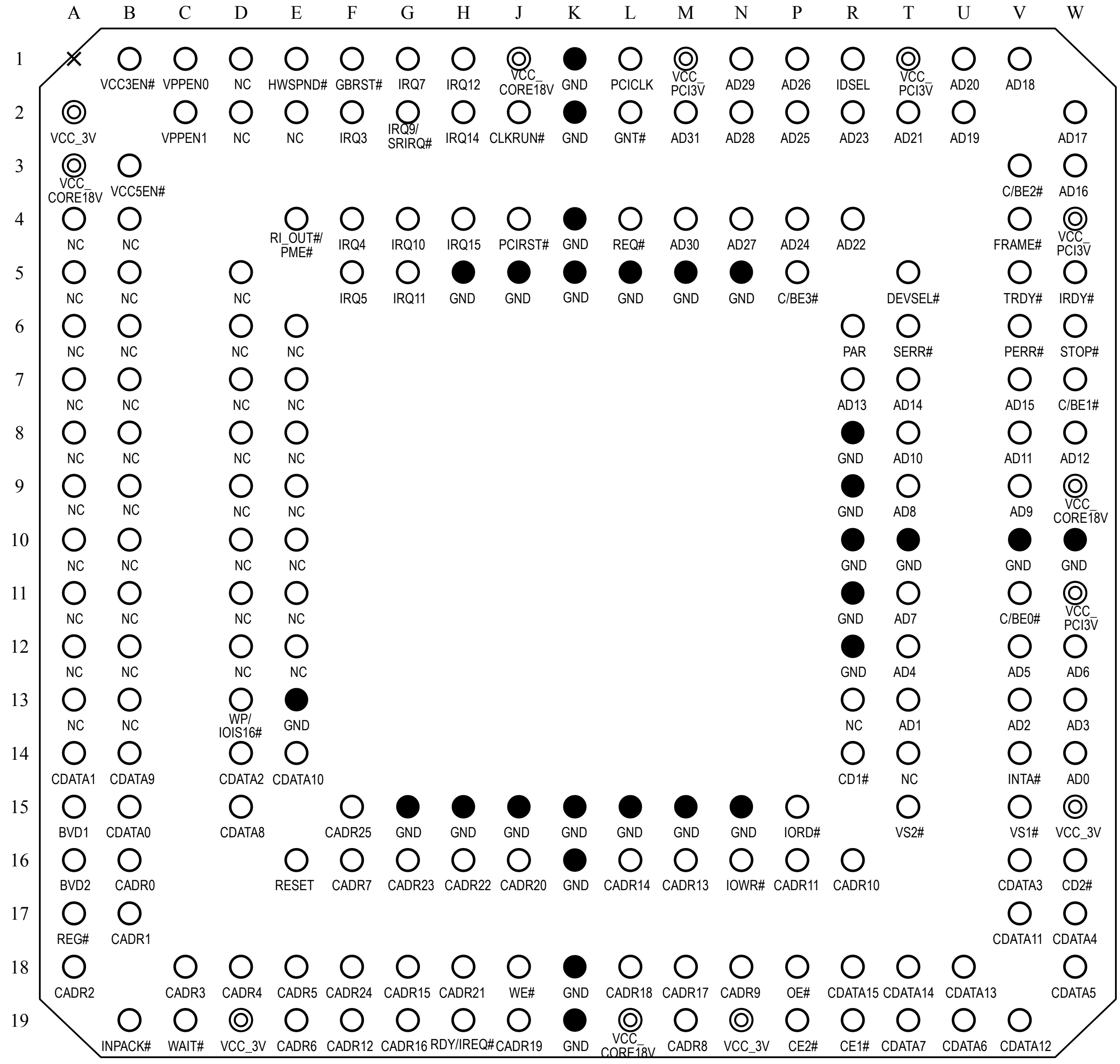
3.1.1 LQFP 144pin Assignments

R5C485 PIN ASSIGNMENT(TOP VIEW)


CADR13
CADR18
CADR8
CADR17
CADR9
VCC_3V
IOWR#
CADR11
IORD#
OE#
CADR10
CE2#
CE1#
CDATA15
GND
CDATA7
CDATA14
CDATA6
CDATA13
CDATA5
CDATA12
CDATA4
CDATA11
CDATA3
INPACK#
BVD1
VCC_CORE18V
AD0
AD1
AD2
AD3
GND
AD4
AD5
AD6
AD7
108
73
109
72
CADR19
CADR14
CADR20
WE#
CADR21
RDY/IREQ#
CADR22
GND
CADR16
CADR23
CADR15
CADR24
CADR12
CADR25
VCC_3V
CADR7
CADR6
CADR5
RESET
CADR4
WAIT#
CADR3
GND
CADR2
REG#
CADR1
BVD2
CADR0
CDATA0
CDATA8
CDATA1
CDATA9
CDATA2
CDATA10
WP/IOIS16#
VCC_CORE18V
C/BE0#
AD8
AD9
VCC_PCI3V
AD10
AD11
GND
AD12
AD13
AD14
AD15
C/BE1#
PAR
SERR#
PERR#
GND
STOP#
DEVSEL#
TRDY#
IRDY#
FRAME#
C/BE2#
AD16
AD17
AD18
AD19
GND
AD20
AD21
AD22
AD23
VCC_PCI3V
IDSEL
C/BE3#
AD24
AD25
5C485 Pin Assignment
16-Bit PC Card Interface Config.
144
37
1
36
HWSPND#
VPPEN1
VPPEN0
VCC3EN#
VCC5EN#
VCC_3V
RI_OUT#/PME#
CCD1#
CCD2#
CVS1
CVS2
GBRST#
GND
IRQ3
IRQ4
IRQ5
IRQ7
IRQ9/SIRQ#
IRQ10
IRQ11
IRQ12
IRQ14
IRQ15
INTA#
CLKRUN#
PCIRST#
PCICLK
GNT#
REQ#
AD31
AD30
AD29
AD28
GND
AD27
AD26

3.1.2 CSP 208pin assignments

Bottom View



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W
1	✕	VCC3EN#	VPPEN0	NC	HWSPND#	GBRST#	IRQ7	IRQ12	VCC_CORE18V	GND	PCICLK	VCC_PCI3V	AD29	AD26	IDSEL	VCC_PCI3V	AD20	AD18	
2	VCC_3V		VPPEN1	NC	NC	IRQ3	IRQ9/SRIRQ#	IRQ14	CLKRUN#	GND	GNT#	AD31	AD28	AD25	AD23	AD21	AD19		AD17
3	VCC_CORE18V	VCC5EN#																C/BE2#	AD16
4	NC	NC			RI_OUT#/PME#	IRQ4	IRQ10	IRQ15	PCIRST#	GND	REQ#	AD30	AD27	AD24	AD22			FRAME#	VCC_PCI3V
5	NC	NC		NC		IRQ5	IRQ11	GND	GND	GND	GND	GND	GND	C/BE3#		DEVSEL#		TRDY#	IRDY#
6	NC	NC		NC	NC										PAR	SERR#		PERR#	STOP#
7	NC	NC		NC	NC										AD13	AD14		AD15	C/BE1#
8	NC	NC		NC	NC										GND	AD10		AD11	AD12
9	NC	NC		NC	NC										GND	AD8		AD9	VCC_CORE18V
10	NC	NC		NC	NC										GND	GND		GND	GND
11	NC	NC		NC	NC										GND	AD7		C/BE0#	VCC_PCI3V
12	NC	NC		NC	NC										GND	AD4		AD5	AD6
13	NC	NC		WP/IOIS16#	GND										NC	AD1		AD2	AD3
14	CDATA1	CDATA9		CDATA2	CDATA10										CD1#	NC		INTA#	AD0
15	BVD1	CDATA0		CDATA8		CADR25	GND	GND	GND	GND	GND	GND	GND	IORD#		VS2#		VS1#	VCC_3V
16	BVD2	CADR0			RESET	CADR7	CADR23	CADR22	CADR20	GND	CADR14	CADR13	IOWR#	CADR11	CADR10			CDATA3	CD2#
17	REG#	CADR1																CDATA11	CDATA4
18	CADR2		CADR3	CADR4	CADR5	CADR24	CADR15	CADR21	WE#	GND	CADR18	CADR17	CADR9	OE#	CDATA15	CDATA14	CDATA13		CDATA5
19		INPACK#	WAIT#	VCC_3V	CADR6	CADR12	CADR16	RDY/IREQ#	CADR19	GND	VCC_CORE18V	CADR8	VCC_3V	CE2#	CE1#	CDATA7	CDATA6	CDATA12	

3.2 Pin Characteristics

3.2.1 LQFP Pin List

Pin No.	16-bit Card Interface		CardBus Card Interface		Pin Characteristics			Note
	Pin Name	Dir	Pin Name	Dir	5V Tolerant	Pwr Rail	Drive	
1	HWSPND#/ SPKROUT	I/O	HWSPND#/ SPKROUT	I/O	✓	3V	4mA	
2	VPPEN1	O	VPPEN1	O	✓	3V	4mA	
3	VPPEN0	O	VPPEN0	O	✓	3V	4mA	
4	VCC3EN#	O	VCC3EN#	O	✓	3V	4mA	
5	VCC5EN#	O	VCC5EN#	O	✓	3V	4mA	
6	VCC_3V	DC in	VCC_3V	DC in		G	—	
7	RI_OUT#/ PME#	O (OD)	RI_OUT#/ PME#	O (OD)	✓	3V	4mA	
8	CD1#	I (PU)	CCD1#	I (PU)	✓	3V	—	
9	CD2#	I (PU)	CCD2#	I (PU)	✓	3V	—	
10	VS1#	I/O	CVS1	I/O	✓	3V	1mA	
11	VS2#	I/O	CVS2	I/O	✓	3V	1mA	
12	GBRST#	I	GBRST#	I	✓	3V	—	
13	GND	DC in	GND	DC in		3V	—	
14	IRQ3/GPIO0	I/O	IRQ3/GPIO0	I/O	✓	3V	4mA	
15	IRQ4/GPIO1	I/O	IRQ4/GPIO1	I/O	✓	3V	4mA	
16	IRQ5/GPIO2	I/O	IRQ5/GPIO2	I/O	✓	3V	4mA	
17	IRQ7/GPIO3	I/O	IRQ7/GPIO3	I/O	✓	3V	4mA	
18	IRQ9/SIRQ#	I/O	IRQ9/SIRQ#	I/O	✓	3V	4mA	
19	IRQ10	I/O	IRQ10	I/O	✓	3V	4mA	
20	IRQ11	I/O	IRQ11	I/O	✓	3V	4mA	
21	IRQ12	I/O	IRQ12	I/O	✓	3V	4mA	
22	IRQ14	I/O	IRQ14	I/O	✓	3V	4mA	
23	IRQ15/ ZVEN#	O (TS)	IRQ15/ ZVEN#	O (TS)	✓	3V	4mA	
24	INTA#	O (OD)	INTA#	O (OD)	✓	P	PCI	
25	CLKRUN#	I/O	CLKRUN#	I/O	✓	P	PCI	
26	PCIRST#	I	PCIRST#	I	✓	P	—	
27	PCICLK	I	PCICLK	I	✓	P	—	
28	GNT#	I	GNT#	I	✓	P	—	
29	REQ#	O (TS)	REQ#	O (TS)	✓	P	PCI	
30	AD31	I/O	AD31	I/O	✓	P	PCI	
31	AD30	I/O	AD30	I/O	✓	P	PCI	
32	AD29	I/O	AD29	I/O	✓	P	PCI	
33	AD28	I/O	AD28	I/O	✓	P	PCI	
34	GND	DC in	GND	DC in		G	—	
35	AD27	I/O	AD27	I/O	✓	P	PCI	
36	AD26	I/O	AD26	I/O	✓	P	PCI	

Pin No.	16-bit Card Interface		CardBus Card Interface		Pin Characteristics			Note
	Pin Name	Dir	Pin Name	Dir	5V Tolerant	Pwr Rail	Drive	
37	AD25	I/O	AD25	I/O	✓	P	PCI	
38	AD24	I/O	AD24	I/O	✓	P	PCI	
39	C/BE3#	I/O	C/BE3#	I/O	✓	P	PCI	
40	IDSEL	I	IDSEL	I	✓	P	—	
41	VCC_PCI3V	DC in	VCC_PCI3V	DC in		P	—	
42	AD23	I/O	AD23	I/O	✓	P	PCI	
43	AD22	I/O	AD22	I/O	✓	P	PCI	
44	AD21	I/O	AD21	I/O	✓	P	PCI	
45	AD20	I/O	AD20	I/O	✓	P	PCI	
46	GND	DC in	GND	DC in		G	—	
47	AD19	I/O	AD19	I/O	✓	P	PCI	
48	AD18	I/O	AD18	I/O	✓	P	PCI	
49	AD17	I/O	AD17	I/O	✓	P	PCI	
50	AD16	I/O	AD16	I/O	✓	P	PCI	
51	C/BE2#	I/O	C/BE2#	I/O	✓	P	PCI	
52	FRAME#	I/O	FRAME#	I/O	✓	P	PCI	
53	IRDY#	I/O	IRDY#	I/O	✓	P	PCI	
54	TRDY#	I/O	TRDY#	I/O	✓	P	PCI	
55	DEVSEL#	I/O	DEVSEL#	I/O	✓	P	PCI	
56	STOP#	I/O	STOP#	I/O	✓	P	PCI	
57	GND	DC in	GND	DC in		G	—	
58	PERR#	I/O	PERR#	I/O	✓	P	PCI	
59	SERR#	O (OD)	SERR#	O (OD)	✓	P	PCI	
60	PAR	I/O	PAR	I/O	✓	P	PCI	
61	C/BE1#	I/O	C/BE1#	I/O	✓	P	PCI	
62	AD15	I/O	AD15	I/O	✓	P	PCI	
63	AD14	I/O	AD14	I/O	✓	P	PCI	
64	AD13	I/O	AD13	I/O	✓	P	PCI	
65	AD12	I/O	AD12	I/O	✓	P	PCI	
66	GND	DC in	GND	DC in		G	—	
67	AD11	I/O	AD11	I/O	✓	P	PCI	
68	AD10	I/O	AD10	I/O	✓	P	PCI	
69	VCC_PCI3V	DC in	VCC_PCI3V	DC in		P	—	
70	AD9	I/O	AD9	I/O	✓	P	PCI	
71	AD8	I/O	AD8	I/O	✓	P	PCI	
72	C/BE0#	I/O	C/BE0#	I/O	✓	P	PCI	
73	AD7	I/O	AD7	I/O	✓	P	PCI	
74	AD6	I/O	AD6	I/O	✓	P	PCI	
75	AD5	I/O	AD5	I/O	✓	P	PCI	
76	AD4	I/O	AD4	I/O	✓	P	PCI	
77	GND	DC in	GND	DC in		G	—	
78	AD3	I/O	AD3	I/O	✓	P	PCI	
79	AD2	I/O	AD2	I/O	✓	P	PCI	

Pin No.	16-bit Card Interface		CardBus Card Interface		Pin Characteristics			Note
	Pin Name	Dir	Pin Name	Dir	5V Tolerant	Pwr Rail	Drive	
80	AD1	I/O	AD1	I/O	✓	P	PCI	
81	AD0	I/O	AD0	I/O	✓	P	PCI	
82	VCC_CORE18V	DC in	VCC_CORE18V	DC in		C	—	
83	BVD1/ STSCHG#/ RI#	I (PU)	CSTSCHG	I (PD)	✓	3V	—	2
84	INPACK#	I (PU)	CREQ#	I (PU)	✓	3V	—	2
85	CDATA3	I/O	CAD0	I/O	✓	3V	4mA	
86	CDATA11	I/O	CAD2	I/O	✓	3V	4mA	
87	CDATA4	I/O	CAD1	I/O	✓	3V	4mA	
88	CDATA12	I/O	CAD4	I/O	✓	3V	4mA	
89	CDATA5	I/O	CAD3	I/O	✓	3V	4mA	
90	CDATA13	I/O	CAD6	I/O	✓	3V	4mA	
91	CDATA6	I/O	CAD5	I/O	✓	3V	4mA	
92	CDATA14	I/O	—	—	✓	3V	4mA	
93	CDATA7	I/O	CAD7	I/O	✓	3V	4mA	
94	GND	DC in	GND	DC in		G	—	
95	CDATA15	I/O	CAD8	I/O	✓	3V	4mA	
96	CE1#	O (TS)	CC/BE0#	I/O	✓	3V	4mA	
97	CE2#	O (TS)	CAD10	I/O	✓	3V	4mA	
98	CADR10	O (TS)	CAD9	I/O	✓	3V	4mA	
99	OE#	O (TS)	CAD11	I/O	✓	3V	4mA	
100	IORD#	O (TS)	CAD13	I/O	✓	3V	4mA	
101	CADR11	O (TS)	CAD12	I/O	✓	3V	4mA	
102	IOWR#	O (TS)	CAD15	I/O	✓	3V	4mA	
103	VCC_3V	DC in	VCC_3V	DC in		3V	—	
104	CADR9	O (TS)	CAD14	I/O	✓	3V	4mA	
105	CADR17	O (TS)	CAD16	I/O	✓	3V	4mA	
106	CADR8	O (TS)	CC/BE1#	I/O	✓	3V	4mA	
107	CADR18	O (TS)	—	—	✓	3V	4mA	
108	CADR13	O (TS)	CPAR	I/O	✓	3V	4mA	
109	CADR19	O (TS)	—	I/O (PU)	✓	3V	4mA	1
110	CADR14	O (TS)	CPERR#	I/O (PU)	✓	3V	4mA	1
111	CADR20	O (TS)	CSTOP#	I/O (PU)	✓	3V	4mA	1
112	WE#	O (TS)	CGNT#	O (TS)	✓	3V	4mA	
113	CADR21	O (TS)	CDEVSEL#	I/O (PU)	✓	3V	4mA	1
114	RDY/ IREQ#	I (PU)	CINT#	I (PU)	✓	3V	—	2
115	CADR22	O (TS)	CTRDY#	I/O (PU)	✓	3V	4mA	1
116	GND	DC in	GND	DC in		G	—	
117	CADR16	O (TS)	CCLK	O (TS)	✓	3V	CB	
118	CADR23	O (TS)	CFRAME#	I/O	✓	3V	4mA	
119	CADR15	O (TS)	CIRDY#	I/O (PU)	✓	3V	4mA	1

Pin No.	16-bit Card Interface		CardBus Card Interface		Pin Characteristics			Note
	Pin Name	Dir	Pin Name	Dir	5V Tolerant	Pwr Rail	Drive	
120	CADR24	O (TS)	CAD17	I/O	✓	3V	4mA	
121	CADR12	O (TS)	CC/BE2#	I/O	✓	3V	4mA	
122	CADR25	O (TS)	CAD19	I/O	✓	3V	4mA	
123	VCC_3V	DC in	VCC_3V	DC in		3V	—	
124	CADR7	O (TS)	CAD18	I/O	✓	3V	4mA	
125	CADR6	O (TS)	CAD20	I/O	✓	3V	4mA	
126	CADR5	O (TS)	CAD21	I/O	✓	3V	4mA	
127	RESET	O (TS)	CRST#	O (TS)	✓	3V	2mA	
128	CADR4	O (TS)	CAD22	I/O	✓	3V	4mA	
129	WAIT#	I (PU)	CSERR#	I (PU)	✓	3V	—	2
130	CADR3	O (TS)	CAD23	I/O	✓	3V	4mA	
131	GND	DC in	GND	DC in		G	—	
132	CADR2	O (TS)	CAD24	I/O	✓	3V	4mA	
133	REG#	O (TS)	CC/BE3#	I/O	✓	3V	4mA	
134	CADR1	O (TS)	CAD25	I/O	✓	3V	4mA	
135	BVD2/ SPKR#	I (PU)	CAUDIO	I (PU)	✓	3V	—	2
136	CADR0	O (TS)	CAD26	I/O	✓	3V	4mA	
137	CDATA0	I/O	CAD27	I/O	✓	3V	4mA	
138	CDATA8	I/O	CAD28	I/O	✓	3V	4mA	
139	CDATA1	I/O	CAD29	I/O	✓	3V	4mA	
140	CDATA9	I/O	CAD30	I/O	✓	3V	4mA	
141	CDATA2	I/O	—	—	✓	3V	4mA	
142	CDATA10	I/O	CAD31	I/O	✓	3V	4mA	
143	WP/ IOIS16#	I(PU)	CCLKRUN#	I/O (PU)	✓	3V	4mA	2
144	VCC_CORE18V	DC in	VCC_CORE18V	DC in		C	—	

Pin Type

I: Input Pin, O: Output Pin, I/O: Input Output Pin,
I (PU): Input Pin with Internal Pullup Resister,
I (PD): Input Pin with Internal Pulldown Resister,
I/O (PU): Input Output Pin with Internal Pullup Resister,
I/O (PD): Input Output Pin with Internal Pulldown Resister,
O (TS): Three State Output Pin, O (OD): Open Drain Output Pin

Power Rail

P: VCC_PCI3V, C: VCC_CORE18V, 3V: VCC_3V

Drive

PCI: PCI Compliant,
CB: PCMCIA CardBus PC Card Compliant

Note

1: Pullup is attached when PC Card Interface is configured as a CardBus Interface Mode.
2: Pullup or Pulldown is configured according to the type of a card inserted.

3.2.2 CSP Pin List

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
E1	HWSPND#	R1	IDSEL	A15	BVD1	F15	CADR25
C2	VPPEN1	R2	AD23	B19	INPACK#	F16	CADR7
C1	VPPEN0	R4	AD22	V16	CDATA3	E19	CADR6
B1	VCC3EN#	T2	AD21	V17	CDATA11	E18	CADR5
B3	VCC5EN#	U1	AD20	W17	CDATA4	E16	RESET
E4	RI_OUT#/PME#	U2	AD19	V19	CDATA12	D18	CADR4
R14	CD1#	V1	AD18	W18	CDATA5	C19	WAIT#
W16	CD2#	W2	AD17	U18	CDATA13	C18	CADR3
V15	VS1#	W3	AD16	U19	CDATA6	A18	CADR2
T15	VS2#	V3	C/BE2#	T18	CDATA14	A17	REG#
F1	GBRST#	V4	FRAME#	T19	CDATA7	B17	CADR1
F2	IRQ3	W5	IRDY#	R18	CDATA15	A16	BVD2
F4	IRQ4	V5	TRDY#	R19	CE1#	B16	CADR0
F5	IRQ5	T5	DEVSEL#	P19	CE2#	B15	CDATA0
G1	IRQ7	W6	STOP#	R16	CADR10	D15	CDATA8
G2	IRQ9/SRIRQ#	V6	PERR#	P18	OE#	A14	CDATA1
G4	IRQ10	T6	SERR#	P15	IORD#	B14	CDATA9
G5	IRQ11	R6	PAR	P16	CADR11	D14	CDATA2
H1	IRQ12	W7	C/BE1#	N16	IOWR#	E14	CDATA10
H2	IRQ14	V7	AD15	N18	CADR9	D13	WP/IOIS16#
H4	IRQ15	T7	AD14	M18	CADR17		
V14	INTA#	R7	AD13	M19	CADR8		
J2	CLKRUN#	W8	AD12	L18	CADR18		
J4	PCIRST#	V8	AD11	M16	CADR13		
L1	PCICLK	T8	AD10	J19	CADR19		
L2	GNT#	V9	AD9	L16	CADR14		
L4	REQ#	T9	AD8	J16	CADR20		
M2	AD31	V11	C/BE0#	J18	WE#		
M4	AD30	T11	AD7	H18	CADR21		
N1	AD29	W12	AD6	H19	RDY/IREQ#		
N2	AD28	V12	AD5	H16	CADR22		
N4	AD27	T12	AD4	G19	CADR16		
P1	AD26	W13	AD3	G16	CADR23		
P2	AD25	V13	AD2	G18	CADR15		
P4	AD24	T13	AD1	F18	CADR24		
P5	C/BE3#	W14	AD0	F19	CADR12		

Pin Name	Ball#	Pin Name	Ball#
VCC_CORE18V	A3, J1, W9, L19	NC	A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, D1, D2, D5, D6, D7, D8, D9, D10, D11, D12, E2, E6, E7, E8, E9, E10, E11, E12, R13, T14
VCC_PCI3V	M1, T1, W4, W11		
VCC_3V	A2, N19, D19, W15		
GND	E13, G15, H5, H15, J5, J15, K1, K2, K4, K5, K15, K16, K18, K19, L5, L15, M5, M15, N5, N15, R8, R9, R10, R11, R12, T10, V10, W10		

3.3 Pin Functions Outline

In this chapter, the detailed signal pins in the R5C485 are explained. Every signal is divided according to their relational interface.

Card Interface signal pin is multi−functional pin. The pin function is configured automatically by the card insertion; CardBus card or 16−bit card. And the pin function is redefined again.

# mark means the signal is on either active or asserted when the signal is low−level. Otherwise, no−mark means the signal is asserted when the signal is high−level.

The following the notations are used to describe the signal type.

IN	Input Pin
OUT	Output Pin
OUT (TS)	Three State Output Pin
OUT (OD)	Open Drain Output Pin
I/O	Input Output Pin
I/O (OD)	Input Output Pin (Output is Open Drain)
s/h/z	Sustained Tri−State is an active low tri−state signal owned and driven by one and only one agent at a time. The agent that drives an s/h/z pin low must drive it high for at least one clock before letting it float. A new agent cannot start driving an s/h/z signal any sooner than one clock after the previous owner tri−state is.

3.3.1 PCI Local Bus interface signals

Pin Name	Type	Description
PCI Bus Interface Pin Descriptions		
PCICLK	IN	***PCI CLOCK:*** PCICLK provides timing for all transactions on PCI. All other PCI signals are sampled on the rising edge of PCICLK.
CLKRUN#	I/O (OD)	***PCI CLOCK RUN:*** This signal indicates the status of PCICLK and an open drain output to request the starting or speeding up of PCICLK. This pin complies with Mobile PCI specification. This signal has no meaning for the PC Card-16 cards. Tie to GND if not used.
PCIRST#	IN	***PCI RESET:*** This input is used to initialize all registers, sequences and signals of the R5C485 to their reset states. All of the outputs of the R5C485 will be tri-stated during PCIRST is asserted.
AD [31:0]	I/O	***ADDRESS AND DATA:*** Address and Data are multiplexed on the same PCI pins.
C/BE [3:0]#	I/O	***BUS COMMAND AND BYTE ENABLES:*** Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of transaction, C/BE [3:0]# define the bus command. During the data phase C/BE [3:0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data.
PAR	I/O	***PARITY:*** Parity is even parity across AD [31:0] and C/BE [3:0]#. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. The master drives PAR for address and write data phases; the target drives PAR for read data phases.
FRAME#	I/O s/h/z	***CYCLE FRAME:*** This signal is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase or has complete.
TRDY#	I/O s/h/z	***TARGET READY:*** This signal indicates the initialing agent‘s ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a read, TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD [31:0]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted both IRDY# and TRDY# are asserted together.
IRDY#	I/O s/h/z	***INITIATOR READY:*** This signal indicates the initiating agent‘s ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD [31:0]. During a read, it indicates the target is prepared to accept data. Wait cycles are inserted both IRDY# and TRDY# are asserted together.
STOP#	I/O s/h/z	***STOP:*** This signal indicates the current target is requesting the master to stop the current transaction.
IDSEL	IN	***INITIALIZATION DEVICE SELECT:*** This signal is used as a chip select during configuration read and writes transactions.
DEVSEL#	I/O s/h/z	***DEVICE SELECT:*** When actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

Pin Name	Type	Description
PCI Bus Interface Pin Descriptions (Continued)		
PERR#	I/O s/h/z	***PARITY ERROR:*** This signal is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The R5C485 drives this output active "low" if it detects a data parity error during a write phase.
SERR#	OUT (OD)	***SYSTEM ERROR:*** This signal is pure open drain. The R5C485 actively drives this output for a single PCI clock when it detects an address parity error on either the primary bus or the secondary bus.
REQ#	OUT (TS)	***REQUEST:*** This signal indicates to the arbiter that the R5C485 desires use of the bus. This is a point-to-point signal.
GNT#	IN	***GRANT:*** This signal indicates the R5C485 that access to the bus has been granted. This is a point-to-point signal.
GBRST#	IN	***GLOBAL RESET:*** This reset brings all of the R5C485 internal registers to their default states, including those registers not initialized by PCIRST#. (See Chapter 4.10.) This should be asserted one time when system power supply is on.

3.3.2 System Interrupt signals

Pin Name	Type	Description
System Interrupt Pin Descriptions		
INTA#	OUT (OD)	***PCI INTERRUPT REQUEST A:*** This signal indicates interrupts from the R5C485 to the host. This signal forwards the interrupt request from the card socket interface on default setting. See Chapter 4.7 about the details of interrupt.
IRQ3/GPIO0 IRQ4/GPIO1 IRQ5/GPIO2 IRQ7/GPIO3 IRQ9/SRIRQ# IRQ12/ LEDOUT IRQ14	I/O *	***SYSTEM INTERRUPT REQUEST IRQ 3-15:*** These signals indicate the interrupt requests from one of the cards and are connected to the ISA bus IRQx signal. IRQ12 is reassigned as an LEDOUT when LED enable bit in ATA control register is set to one. When Serial IRQ Enable bit in Misc Control register is set to one, IRQ9 is reassigned as SRIRQ# signal, at the same time IRQ10 is reassigned as LED# signal. When Serial IRQ signal is enabled, IRQ3, 4,5 and 7 are assigned as GPIO (General Purpose I/O) pins. These are input/output pins determined by user without effect on the controller transaction. When the Serial ROM is used, IRQ12 and 14 work as SCL and SDA and are Open Drain. See the Serial ROM in Chapter 4.15 about the details of SCL/SDA *IRQ[3:9], IRQ12 and IRQ14 are three-state pin on IRQ.
IRQ10/LED# IRQ11 IRQ15/ ZVEN#	OUT (TS)	
RI_OUT#/ PME#	OUT (TS)	***RING INDICATE OUTPUT:*** When 16-bit card is inserted and Ring Indicate Enable bit in the Interrupt and General Control register is set to one, RI# on the IO Card is forwarded to RI_OUT#. ***POWER MANAGEMENT EVENT:*** When PME_En bit in Power Management Control/Status register is set or when Power Status is set to any state mode except D0, this signal is assigned as PME#.

3.3.3 16-bit PC Card Interface signals

Pin Name	Type	Description
16-bit PC Card Interface Pin Descriptions		
CDATA [15:0]	I/O	***16-bit Card DATA BUS SIGNALS [15:0]:*** Input buffer is disabled when the card socket power supply is off or card is not inserted.
CADR [25:0]	OUT (TS)	***16-bit Card ADDRESS BUS SIGNALS [25:0]:*** 16-bit PC Card address lines.
IORD#	OUT (TS)	***16-bit Card I/O READ:*** This signal is driven low to enable 16-bit I/O PC Card data output during host I/O read cycles.
IOWR#	OUT (TS)	***16-bit Card I/O WRITE:*** This signal is driven low to strobe write data into 16-bit I/O PC Card during host I/O write cycles.
OE#	OUT (TS)	***16-bit Card OUTPUT ENABLE:*** This signal is driven low to enable 16-bit memory PC Card data output during host memory read cycles.
WE#	OUT (TS)	***16-bit Card WRITE ENABLE:*** This signal is driven low to strobe memory write data into 16-bit memory PC Cards.
CE1#	OUT (TS)	***16-bit Card CARD ENABLE 1:*** This signal enables even-numbered address bytes.
CE2#	OUT (TS)	***16-bit Card CARD ENABLE 2:*** This signal enables odd-numbered address bytes.
REG#	OUT (TS)	***16-bit Card ATTRIBUTE MEMORY SELECT:*** This signal selects Attribute memory access or common memory access during the 16bit memory cycle. Attribute memory access is selected when this signal is “low”, and common memory access is selected when this signal is “high”.
READY/ IREQ#	IN	***16-bit Card READY/BUSY or INTERRUPT REQUEST:*** This signal has two different functions. READY/BUSY# input on the memory PC card, and IREQ# input on the I/O card.
WP/ IOIS16#	IN	***16-bit Card WRITE PROTECT or CARD IS 16-BIT PORT:*** This signal has two different functions. Write Protect Switch input on the memory PC card, and IOIS16 input on the I/O card.
RESET	OUT (TS)	***16-bit Card CARD RESET:*** This signal forces a hard reset to 16-bit PC Card.
WAIT#	IN	***16-bit Card BUS CYCLE WAIT:*** This signal is driven by a 16-bit PC Card to extend the completion of the memory or I/O cycle in progress.
BVD1/ STSCHG#/ RI#	IN	***16-bit Card BATTERY VOLTAGE DETECT 1 or STATUS CHANGE:*** This signal has three different functions. The battery voltage detect input 1 on the memory PC card, and Card Status Change#/Ring Indicate# input on the I/O card.
BVD2/ SPKR#/ LED	IN	***16-bit Card BATTERY VOLTAGE DETECT 2 or DIGITAL AUDIO or LED INPUT:*** This signal has three different functions. The battery voltage detect input 2 on the memory PC card, and SPKR# input or LED input on the I/O card.
INPACK#	IN	***16-bit Card INPUT ACKNOWLEDGE:*** This signal is asserted by the PC Card when it can respond to an I/O read cycle at the current address. When INPACK# Enable bit of the Misc Control 1 register set to one, this function is enabled.
CD1#	IN	***16-bit Card CARD DETECT 1:*** CD [2:1]# pins are used to detect the card insertion. CD [2:1]# pins are used in conjunction with VS [2:1]# to decode card type information.
CD2#	IN	***16-bit Card CARD DETECT 2:*** CD [2:1]# pins are used to detect the card insertion. CD [2:1]# pins are used in conjunction with VS [2:1]# to decode card type information.
VS1	I/O	***16-bit Card CARD VOLTAGE CAPABILITY SENSE 1:*** VS [2:1]# pins are used in conjunction with CD [2:1]# to decode card type information.
VS2	I/O	***16-bit Card CARD VOLTAGE CAPABILITY SENSE 2:*** VS [2:1]# pins are used in conjunction with CD [2:1]# to decode card type information.

3.3.4 CardBus PC Card Interface signals

Pin Name	Type	Description
		CardBus PC Card Interface Pin Descriptions
CCLK	OUT (TS)	***CardBus Clock:*** This signal provides timing for all transactions on the PC Card Standard interface and it is an input to every PC Card Standard device. All other CardBus PC Card signals, except CRST# (upon assertion), CCLKRUN#, CINT#, CSTSCHG, CAUDIO, CCD [2:1]# and CVS [2:1], are sampled on the rising edge of CCLK, and all timing parameters are defined with respect to this edge.
CCLKRUN#	I/O s/h/z	***CardBus Clock Run:*** This signal is used by cards to request starting (or speeding up) clock; CCLK. CCLKRUN# also indicates the clock status. For PC cards, CCLKRUN# is an open drain output and it is also an input. The R5C485 indicates the clock status of the primary bus to the CardBus card.
CRST#	OUT (TS)	***CardBus Card Reset:*** This signal is used to bring CardBus Card specific registers, sequencers and signals to a consistent state. Anytime CRST# is asserted, all CardBus card output signals will be driven to their initial state.
CAD [31:0]	I/O	***CardBus Address/Data:*** These signals are multiplexed on the same CardBus card pins. A bus transaction consists of an address phase followed by one or more data phases. CardBus card supports both read and write bursts. CAD [31:0] contains a physical address (32 bits). For I/O, this is a byte address; for configuration and memory it is a DWORD address. During data phases, CAD [7:0] contains the least significant byte (LSB) and CAD [31:24] contains the most significant byte (MSB). Write data is stable and valid when CIRDY# is asserted and read data is stable and valid when CTRDY# is asserted. Data is transferred during those clocks where both CIRDY# and CTRDY# are asserted.
CC/BE [3:0]#	I/O	***CardBus Command/Bye Enables:*** These signals are multiplexed on the same CardBus card pins. During the address phase of a transaction, CC/BE [3:0]# define the bus command. During the data phase, CC/BE [3:0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. CC/BE [0]# applies to byte 0 (LSB) and CC/BE [3]# applies to byte 3 (MSB).
CPAR	I/O	***CardBus Parity:*** This signal is even parity across CAD [31:0] and CC/BE [3:0]#. All CardBus card agents require parity generation. CPAR is stable and valid clock after either CIRDY# is asserted on a write transaction or CTRDY# is asserted on a read transaction. Once CPAR is valid, it remains valid until one clock after the completion of the current data phase. (CPAR has the same timing as CAD [31:0] but delayed by one clock.) The master drives CPAR for address and write data phases; the target drives CPAR for read data phases.
CFRAME#	I/O s/h/z	***CardBus Cycle Frame*****:** This signal is driven by the current master to indicate the beginning and the duration for a transaction. CFRAME# is asserted to indicate that a bus transaction is beginning. While CFRAME# is asserted, data transfers continue. When CFRAME# is deasserted, the transaction is in the final data phase.
CIRDY#	I/O s/h/z	***CardBus Initiator Ready:*** This signal indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. CIRDY# is used in conjunction with CTRDY#. A data phase is completed on any clock both CIRDY# and CTRDY# are sampled asserted. During a write, CIRDY# indicates that valid data is present on CAD [31:0]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both CIRDY# and CTRDY# are asserted together.
CTRDY#	I/O s/h/z	***CardBus Target Ready:*** This signal indicates the agent's (selected target's) ability to complete the current data phase of the transaction. CTRDY# is used in conjunction with CIRDY#. A data phase is completed on any clock both CTRDY# and CIRDY# are sampled asserted. During a read, CTRDY# indicates that valid data is present on CAD [31:0]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both CIRDY# and CTRDY# are asserted together.

Pin Name	Type	Description
		CardBus PC Card Interface Pin Descriptions (Continued)
CSTOP#	I/O s/h/z	***CardBus Stop:*** This signal indicates the current target is requesting the master to stop the current transaction.
CDEVSEL#	I/O s/h/z	***CardBus Device Select:*** This signal indicates the driving device has decoded its address as the target of the current access when actively driven. As an input, CDEVSEL# indicates whether any device on the bus has been selected.
CREQ#	IN	***CardBus Request:*** This signal indicates to the arbiter that this agent desires use of the bus. Every master has its own CREQ#.
CGNT#	OUT	***CardBus Grant:*** This signal indicates to the agent that access to the bus has been granted. Every master has its own CGNT#.
CPERR#	I/O s/h/z	***CardBus Parity Error:*** This signal is only for the reporting of data parity errors during all CardBus Card transactions. An agent cannot report a CPERR# until it has claimed the access by asserting CDEVSEL# and completed a data phase.
CSERR#	IN	***CardBus System Error:*** This signal indicates system errors are occurred on the CardBus Card. The R5C485 asserts SERR# to report system errors to PCI.
CINT#	IN	***CardBus Interrupt Request:*** This signal is an input signal from CardBus card. It is level sensitive, and asserted low (negative true), using an open drain output driver. The assertion and deassertion of CINT# is asynchronous to CCLK.
CSTSCHG	IN	***CardBus Card Status Change:*** This signal is an input signal used to alert the system to changes in the READY, WP, or BVD [2:1] conditions of the card. It is also used for the system and/or CardBus card interface Wake up. CSTSCHG is asynchronous to CCLK.
CAUDIO	IN	***CardBus Card Audio:*** This signal is a digital audio input signal from a CardBus Card to the system's speaker. CAUDIO has no relationship to CCLK.
CCD1#	IN	***CardBus Card Detect 1:*** CCD [2:1]# pins are used to detect the card insertion. CCD [2:1]# pins are used in conjunction with CVS [2:1]# to decode card type information.
CCD2#	IN	***CardBus Card Detect 2:*** CCD [2:1]# pins are used to detect the card insertion. CCD [2:1]# pins are used in conjunction with CVS [2:1]# to decode card type information.
CVS1	I/O	***CardBus Card Voltage Sense 1:*** CVS [2:1]# pins are used in conjunction with CCD [2:1]# to decode card type information.
CVS2	I/O	***CardBus Card Voltage Sense 2:*** CVS [2:1]# pins are used in conjunction with CCD [2:1]# to decode card type information.

3.3.5 Socket Power Control signals

Pin Name	Type	Description
		Socket Power Control Signal Descriptions
VCC5EN#	OUT	***VCC 5V ENABLE:*** This signal controls to the PC Card power-switch.
VCC3EN#	OUT	***VCC 3.3V ENABLE:*** This signal controls to the PC Card power-switch.
VPPEN0	OUT	***VPP ENABLE 0:*** This signal controls to the PC Card power-switch. In case of using the Serial ROM I/F, Pullup resistor is required on the AVPPEN0 pin. In case of not using it, Pulldown resistor is required on the AVPPEN0 pin.
VPPEN1	OUT	***VPP ENABLE 1:*** This signal controls to the PC Card power-switch.

3.3.6 Hardware Suspend /Audio signal

Pin Name	Type	Description
		Audio Pin Descriptions
HWSPND#/ SPKROUT	I/O	***Hardware Suspend:*** This signal works as HWSPND# input is 'low'. PCIRST# is not accepted as long as HWSPND# is asserted so that VCC_PCI3V can be powered off. The internal registers of the R5C485 hold the data as long as VCC_CORE18V and VCC_3V are on. When Serial IRQ mode is set, HWSPND# must be asserted after Serial IRQ mode on the chip-set has been disabled. When Hardware Suspend mode is off, HWSPND# must be deasserted before Serial IRQ mode is enabled. When a power is on, follow the reset sequence shown in Chapter 4.10 in order to confirm the input of PCIRST# and PCLK. ***SPEAKER OUTPUT:*** When SPKROUT Enabled bit in the Misc Control register is set to one, this signal is assigned as SPKOUT signal, and outputs a digital audio output from SPKR#.

3.3.7 Power and GND signals

Pin Name	Type	Description
		Power Pin Descriptions
VCC_PCI3V	PWR	***PCI VCC:*** Power Supply pins for PCI interface signals. This pin can be powered at 3.3V.
VCC_CORE18V	PWR	***CORE VCC:*** Power Supply pins for the internal core logic. This pin cant be powered at either 1.8V or 2.5V. Don't turn off this pin during suspension when PME# resume.
VCC_3V	PWR	***3V VCC:*** This supply pin is connected to 3.3V. This pin must not be off on the suspend mode because of the power supply for PME# and GBRST#. This pin supply for Socket of the PC Card Controller also.
GND	PWR	***GND:***

4 FUNCTIONAL DESCRIPTION

4.1 Device Configuration

R5C485 supports PCI-CardBus Bridge Interface functions for PC Card socket with three kinds of register spaces. Logically the R5C485 looks to the primary PCI as a separate secondary bus residing in a single device. The socket has its own register spaces as follows.

4.1.1 PCI Configuration Register Space

PCI Configuration registers are used to control the basic operations, as a setting of PCI device and a status control, in the R5C485. The R5C485 implements 256 bytes configuration space an each function. The first 128 bytes in a socket configuration space adhere to a predefined header format. The remaining 128 bytes of the configuration space are used for a socket control purpose. The R5C485 configuration space is accessible only from the primary PCI bus. No other interfaces respond to configuration cycles.

4.1.2 CardBus (32-bit) Card Control Register Space

CardBus Card Control registers are used to manage status changed events, remote wakeup events and status information about the PC Card in the socket. These registers are used for PC Card-32 as well as PC Card-16. PC Card Control Register Base Address register points to the 4 Kbyte memory mapped I/O space that contains both the PC Card-32 and PC Card-16 Status and Control registers. Socket Status/Control Registers for Card-32 are placed in the lower 2Kbyte of the 4Kbyte and start at offset 000h.

4.1.3 16-bit Card Control Register Space

Socket Status/Control Registers for PC Card-16 are placed in the upper 2Kbyte of the 4Kbyte pointed by the PC Card Control Register Base Address register and start at offset 800h.

4.1.4 16-bit Legacy Port

Legacy mode allows all 16-bit Card Control registers to be accessed through the index/data port at I/O address 3E0/3E2 in order to maintain the backward compatibility with Intel 82365 compatibles like Ricoh RF5C396/366.

4.2 CardBus Card Configuration Mechanism

CardBus Card supports the configuration spaces following the PCI specifications. The host also configures the CardBus Card. The R5C485 supports functions of changing Type 1 PCI configuration command into Type 0 PCI configuration command and transferring them.

4.3 Address Window and Mapping Mechanism

The R5C485 supports one of PCI-Card Bridge Interface function and determines if it is CardBus Card or 16-bit Card automatically on inserting a card.

On CardBus Card interface, the transaction is forwarded by two I/O windows, two memory map I/Os and a prefetchable memory window. CardBus Card address and PCI system address use a flat address in common. So the address range specified by a base register and a limit register is forwarded from PCI to CardBus Card.

And also, the R5C485 supports CardBus Master, so the transfer transaction from CardBus Card interface to PCI interface or to the other card interface is supported. The transaction out of an address range specified by a base register and a limit register is passed to PCI bus.

On 16-bit Card interface, the transaction is transferred by two I/O windows and five memory windows set on 16-bit Card Status Control registers that are compatible with PCIC. The transfer is permitted only from PCI interface to CardBus.

4.3.1 ISA mode

The R5C485 supports the ISA mode for PCI-CardBus Bridge function. Setting ISA enable bit of Bridge Control register enables ISA mode. The ISA mode is applies the I/O transaction of particular addressing area that are enabled by the I/O Base register and the I/O Limit register and are also in the first 64K Byte of PCI I/O space (0000_0000h-0000_FFFFh). When set, the R5C485 forwards from PCI to CardBus I/O transactions addressing the first 256 bytes in 0000X000h, 0000X400h, 0000X800h and 0000XC00h. The R5C485 blocks forwarding from PCI to CardBus I/O transactions addressing the last 768bytes in each 1K-byte block. In the opposite direction (CardBus to PCI) I/O transaction is forwarded if they address the last 768 bytes in each 1K blocks.

4.3.2 VGA mode

The R5C485 supports the VGA mode. When the VGA enable bit of Bridge Control register is set, the R5C485 forwards transactions from PCI to CardBus I/F in the following ranges.

Memory address:	0A0000h to 0BFFFFh
I/O address:	AD [9:0] = 3B0h to 3BBh, and 3C0h to 3DFh (Inclusive of ISA address aliases - AD [15:10] are not decoded.)

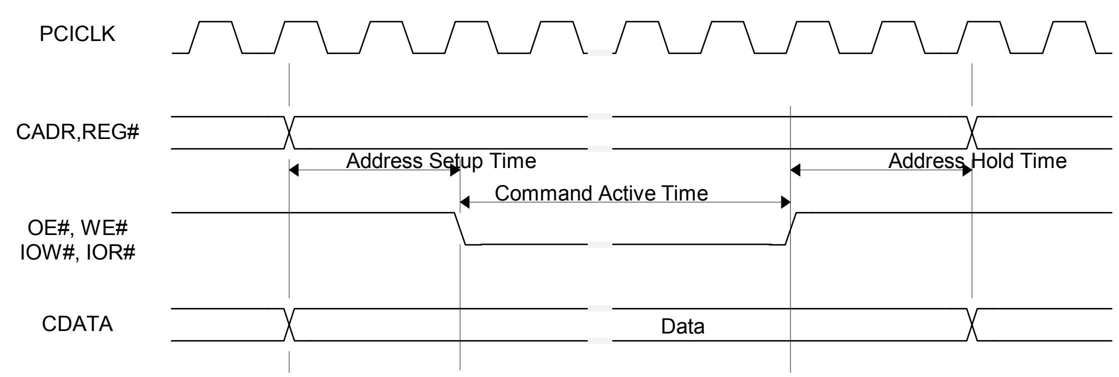
And also, the R5C485 will forward only write transaction to the VGA Palette register in the following ranges.

Palette address:	AD [9:0] = 3C6h, 3C8h, and 3C9h (Inclusive of ISA address aliases - AD [15:10] are not decoded.)

4.4 16-bit Card Interface Timing Control

The R5C485 generates the address, data, and command timing necessary to 16-bit Card interface. Each timing is set in a timer granularity of PCI clock as shown below. When 16-bit I/O enhanced Timing or 16-bit Memory Enhanced Timing bit in each socket control register space is cleared, the default timing is selected regardless of the I/O Win 0-1 Enhanced Timing bit or Memory Enhanced Timing bit. Default timing is selected when the value smaller than the minimum value is set.

16-bit Card Signal Timing Example



Symbol	Parameter	Min	Max	Default	Unit
	I/O Read/ Write				
Tsu	Address Setup Time	2	7	3	PCI Clocks (Typ=30ns)
Tpw	Command Active Time	3	31	6	PCI Clocks (Typ=30ns)
Thl	Address Hold Time	1	7	1	PCI Clocks (Typ=30ns)
	Memory Read/ Write				
Tsu	Address Setup Time	1	7	3 (4) Note 1	PCI Clocks (Typ=30ns)
Tpw	Command Active Time	3	31	6 (8or18) Note 2	PCI Clocks (Typ=30ns)
Thl	Address Hold Time	1	7	1(2) Note3	PCI Clocks (Typ=30ns)

Note1: 4 PCI clocks for 3.3v card attribute memory access.

Note2: 8 PCI clocks for 5v card attribute memory access.
18 PCI clocks for 3.3v card attribute memory access.

Note3: 2PCI clocks for 3.3v card attribute memory access.

4.5 Data Buffers, Posting Write, Prefetching Read

The R5C485 has data buffers, address buffers, and command buffers between the primary PCI bus and the secondary CardBus in order to maintain the high speed data transferring. An 8-DWORD buffer allows Posting Write Data and Prefetching Read Data from PCI bus to CardBus. And a 10-DWORD buffer allows Posting Write Data and Prefetching Read Data from CardBus to PCI bus. Posting of write data is permitted when either Memory Write or Memory Write and Invalidate commands are used for transactions that cross the R5C485 in either direction. In other words, writing buffers are not available during the I/O Write and Configuration Write transactions.

4.6 Error Support

4.6.1 Parity Error

The R5C485 supports parity generation and checks address and data phases on both the primary PCI bus and the secondary CardBus. The R5C485 asserts SERR# when an address parity error occurs during the bus transaction on the PCI bus. When the R5C485 detects a data parity error on either the PCI bus or the CardBus, the bad data and bad parity are passed on to the opposite interface if possible and PERR# is asserted. This enables the parity error recovery mechanisms outlined in the PCI Local Bus Specification.

4.6.2 Master Abort

When the master abort occurs at the destination, the R5C485 behaves in two ways. One is ISA compatible. (Returns all ones during a read. The data will be discarded during a write.) The other way is to assert SERR#.

4.6.3 Target Abort

When the target abort occurs at the opposite side, the R5C485 communicates the error as a target abort to the origination master if possible. But, if cannot, the R5C485 assert SERR# and communicate the error to the system.

4.6.4 CardBus System Error

When CSERR# is asserted on the secondary CardBus interface, the R5C485 always asserts SERR# on the primary PCI interface and communicate the error to the system.

4.7 Interrupts

The R5C485 supports PCI interrupt signals INTA# and ISA interrupt signals IRQx. They inform the Card Status Change Interrupt as a card insert event and the Function Interrupt by the PC card. INTA# is assigned to socket A.

Setting IRQ-ISA enable bit of the Bridge Control register enables the IRQx routing register for PC Card-16/32. On the other hand, setting CINT-ISA Disable bit (Config.A0h bit6) disables the 32bit Function Interrupt to route into the ISA Interrupt and enables to route into the INT interrupt. And also, setting the Card Status Change Interrupt Configuration register on the 16bit Control registers the 16bit Card Status Change Interrupt to route into the ISA Interrupt.

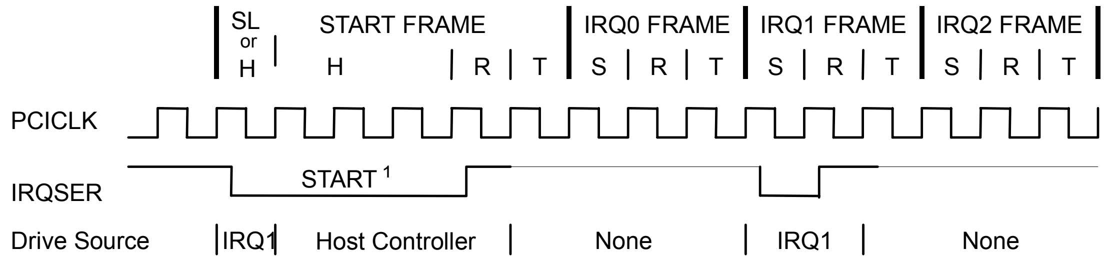
In addition to primary interrupt functions, the R5C485 support Serialized IRQ. IRQ9 is reassigned as SRIRQ# by setting SRIRQ Enable bit (bit7) on the Misc Control register or by connecting IRQ3 with pull-down on a power supply (when the state of GBRST# changes from assertion to deassertion). And LED# and ZVEN# are also enabled. SRIRQ# (Serialized IRQ) output is a Wire-OR structure that simply passes the state of one or more device's IRQ to the host controller. The transfer can be initiated either by a device or by the host controller. A transfer, called an IRQSER Cycle, consists of three frame types: one Start Frame, several IRQ/Data Frames, and one Stop frame. When the SR_PCI_INT_Disable bit (bit5) on the Misc control register is 'Low', the frames of INTA#, INTB#, INTC#, and INTD# (PCI Interrupt signals) following IOCHK# frame are output. When it is 'High', SRIRQ# output only IRQx. IRQ4 has function as same as the SR_PCI_INT_Disable bit (bit5) by connecting IRQ4 with pull-down on a power supply. Setting the SR_PCI_INT_Select bit (bit [4:3]) on the Misc control register enables to assign INTA# into INTB#, INTC# and INTD#. The default is INTA#.

All cycle uses PCICLK as its clock source. There are two modes of operation for the IRQSER Start Frame: Quiet (Active) mode and Continuous (Idle) mode. In Quiet (Active) mode, any device can initiate a Start Frame. The R5C485 output 1PCICLK (Low) and Serialized IRQ is kept on Hi-z during the rest of a Start Frame. After that, IRQ/DATA Frame is repeated.

In Continuous (Idle) mode, only Host Controller can initiate a Start Frame. The R5C485 becomes waiting state to detect 4-8 PCICLK of Start Pulse. These modes change automatically by monitoring the Stop pulse width in a Stop Frame. Quiet (Active) mode is repeated when width of Stop Pulse is 2PCICLK, and Continuous (Idle) mode is repeated when it is 3PCICLK. On the reset, the default is Continuous (Idle) mode.

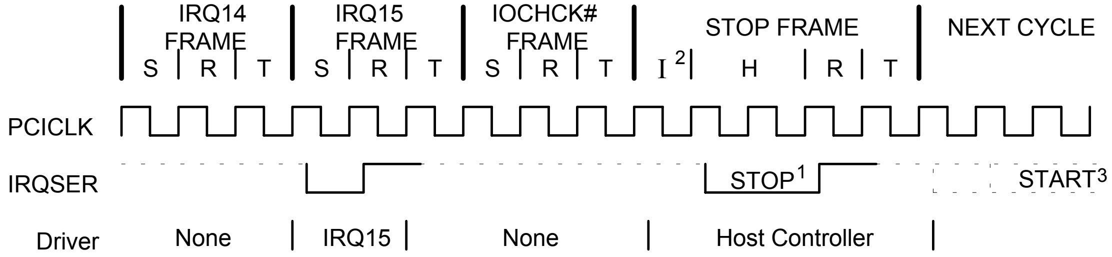
The Start Frame timing and the Stop Frame timing are as follows.

Start Frame timing with source sampled a low pulse on IRQ1


SL
or
H
START FRAME
H
R
T
IRQ0 FRAME
S
R
T
IRQ1 FRAME
S
R
T
IRQ2 FRAME
S
R
T
PCICLK
IRQSER
START 1
Drive Source
IRQ1
Host Controller
None
IRQ1
None

1. Start Frame pulse can be 4-8 clocks wide.

Stop Frame Timing with Host using 17 IRQSER sampling period


IRQ14
FRAME
S
R
T
IRQ15
FRAME
S
R
T
IOCHCK#
FRAME
S
R
T
I 2
STOP FRAME
H
R
T
NEXT CYCLE
PCICLK
IRQSER
STOP1
START3
Driver
None
IRQ15
None
Host Controller

H=Host, SL=Slave Control, R=Recovery, T=Turn-around, S=Sample

1. Stop pulse is 2 clocks wide for Quiet mode, 3 clocks wide for Continuous mode.
2. There may be none, one or more Idle states during the Stop Frame.
3. The nest IRQSER cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stop Frame.

IRQSER Sampling Periods

IRQ/Data Frame	Signal Sampled	# of clocks past Start
1	IRQ0	2
2	IRQ1	5
3	SMI#	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47
17	IOCHCK#	50
18	INTA#	53
19	INTB#	56
20	INTC#	59
21	INTD#	62
32:22	Unassigned	95

4.8 Card Type Detection

If once a valid insertion is detected, the socket state machine of the R5C485 starts to interrogate the PC Card to determine if it is a CardBus PC Card or a 16-bit PC Card. The R5C485 supports VCC values of 5V, 3.3V and combination of them at the socket interface. Card type can be known by reading the Socket Present State register.

CD2#	CD1#	VS2#	VS1#	Card Type		
				Key	Interface	Voltage
ground	ground	open	open	5V	16bit PC Card	5V
ground	ground	open	ground	5V	16bit PC Card	5V and 3.3V
ground	ground	ground	ground	5V	16bit PC Card	5V, 3.3V and X.XV
ground	ground	open	ground	LV	16bit PC Card	3.3V
ground	connect to CVS1	open	connect to CCD1#	LV	CardBus PC Card	3.3V
ground	ground	ground	ground	LV	16bit PC Card	3.3V and X.XV
connect to CVS2	ground	connect to CCD2#	ground	LV	CardBus PC Card	3.3V and X.XV
connect to CVS1	ground	ground	connect to CCD2#	LV	CardBus PC Card	3.3V, X.XV and X.XV
ground	ground	ground	open	LV	16bit PC Card	X.XV
connect to CVS2	ground	connect to CCD2#	open	LV	CardBus PC Card	X.XV
ground	connect to CVS2	connect to CCD1#	open	LV	CardBus PC Card	X.XV and Y.YV
connect to CVS1	ground	open	connect to CCD2#	LV	CardBus PC Card	Y.YV
ground	connect to CVS1	ground	connect to CCD1#	reserved		
ground	connect to CVS2	connect to CDD1#	ground	reserved		

4.9 Mixed Voltage Operation

The R5C485 has 3 independent power nets. The power of Card (VCC_3V) and PCI (VCC_PCI3V) is powered at 3.3V. But the R5C485 can support either 3.3V or 5V of the PCI and the PC Card without external level shifters, because the R5C485's interface has the structure of 5V tolerant.

VCC_CORE18V is powered at 1.8V or 2.5V. VCC_3V are powered at 3.3V.

4.10 Reset Event

Anytime GBRST# is asserted, all R5C485 internal state machines are reset and all registers are set to their default values. (provided that each signal have to follow the reset sequence below.) When PCIRST# is asserted, all registers are set to their default value except the following. The default values of each register are described in each register description.

1. These registers are initialized by only GBRST#, not by PCIRST# (PCI Reset Resistant register).

PCI-CardBus Bridge Config. Space:

Address	Register Name	Bit
·40h	Subsystem Vendor ID	[15:0]
·42h	Subsystem ID	[15:0]
·80h	Bridge Configuration	[15:0]
·82h	Misc Control	[15:0]
·84h	16-bit Interface Control	[15:0]
·88h	16-bit I/O Timing 0	[15:0]
·8Ah	16-bit Memory Timing 0	[15:0]
·A0h	Misc Control 2	[15:0]
·A2h	Misc Control 3	[15:0]
·A4h	Misc Control 4	[31:0]
·C0h	Writable Subsystem Vendor ID	[15:0]
·C2h	Writable Subsystem ID	[15:0]

2. These registers are not initialized by PCIRST# when the power state is D3 and PME Enable bit is set to ”1”. (PME_Context register)

PC Card Socket Status Control Register Space:

Address	Register Name	Bit
·000h	Socket Event	[3:0]
·004h	Socket Mask	[3:0]
·008h	Socket Present State	[11,10,5,4]
·010h	Socket Control	[6:4]
·802h	Power Control	[7:2]
·804h	Card Status Change	[3:0]
·805h	Card Status Change interrupt Configuration	[3:0]
·82Fh	Misc Control 1	[0]

PCI-CardBus Bridge Config. Space:

Address	Register Name	Bit
·DEh	Power Management Capabilities	[15]
·E0h	Power Management Control/ Status	[15,8]

3. Excepting the above registers (PCI Reset Resistant register, PME_Context register), General Purpose I/O 1(AAh) and General Purpose I/O (83Ah), the register is initialized by the reset generated by the power state transition from D3 to D0 as long as the power state is D3.

≡Reset Sequence≡

Follow the sequence for initialization when a power is on.

1. Supply a power to VCC_CORE18V and VCC_3V.
2. Supply a power to VCC_PCI3V.
3. Deassert GBRST#.
4. Deassert HWSPND#.
5. Deassert PCIRST#. (PCLK has to be supplied for 100µsec@33MHz before deasserting PCIRST#.)

Following Step3 by Step2 has no problem.
See the timing a detail of the timing shown in the Chapter 8.3.6.

4.11 Power Management

The R5C485 implements two kinds of power management, software suspend mode and hardware suspend mode, in order to reduce the power consumption on suspend, in addition to the adoption of circuit to reduce the power consumption when power on. The software suspend mode conforms to the ACPI (Advanced Configuration and Power Interface) specification and the PCI Bus Power Management Standard. The R5C485, as a PCI device, implements four power states of D0, D1, D2 and D3. Each power states are the following.
The power management events for the R5C485 and their sources are listed below. When the power state is except D0, the interrupt is disabled and only PME# is enabled to assert.

Event	Source
Card Detect Change	R5C485
Ready/Busy change	card
Battery Warning	card
Ring Indicate (Card Status Change)	card

D0	The maximum powered state. All PCI transactions are acceptable.
D1	Only the PCI Configuration Space access is allowed while the power and clock are provided. CardBus CLK is output.
D2	Only the PCI Configuration Space access is allowed while the power and clock are provided. CardBus CLK is stopped by the protocol of CLKRUN.
D3hot	Only the PCI Configuration Space access is allowed while the power and clock are provided. CardBus CLK is stopped compulsorily. If CardBus card is inserted, CardBus RESET# is asserted at the same time this state is set. When the function is brought back to the D0 state, the reset is automatically performed regardless of the assertion of PCIRST#. PCI interface is disabled when reset. CardBus interface is reset by the assertion of CRST# on CardBus card or RESET on 16bit card.
D3cold	PCI-CardBus Bridge defines D3cold state is to change from VCC_CORE18V and VCC_3V to the auxiliary power source. The R5C485 supports power management events from D3cold with the auxiliary power source. The R5C485 can generate PME# even in D3cold state without PCI clock if the event source is Card Detect Change or Ring Indicate.

In the software suspend mode, when the card is inserted, the interface signals on sockets are kept to the following levels.

CardBus: CCLK=low, CPAR=low, CAD=high or low, CCBE#=high or low, CRST#=low,
CGNT#=high, Pull-up=high, Pull-down=low

16-bit: CDATA=hi-z, CADR=low
Other pins keep the level before the software suspend mode.

In addition to the Operating system-directed power management like ACPI, the R5C485 supports CLKRUN# and CCLKRUN# protocol and it results in a clock stopped and a slow clock. Therefore, it is possible to reduce the power consumption. The state of the card interface signals is the same as the software suspend mode. The hardware suspend mode is enabled when HWSPND# is asserted. Once HWSPND# is asserted, all PCI bus interface signals are disabled and VCC_PCI3V can be powered off. If PCIRST# is asserted, the internal registers of the R5C485 hold the data as long as VCC_CORE18V and VCC_3V are on.

4.12 GPIO

IRQ3, 4, 5 and 7 pins work as GPIO (General Purpose I/O) pin when GPIO Enable bit of the Misc Control 4 register (A4h bit31) is set to 1b on the Serial IRQ mode or on the Multi_IRQ mode of the Misc Control 4 register. When GPIO Enable bit is set to 0b, GPIO outputs are Hi-z and GPIO inputs are disabled. User can change each GPIO pin to either Input or Output by setting either I/O control bits on GPIO register (83Ah) or General Purpose I/O 1 register of the Config register space (AAh). When GPIO Enable bit is set to 1b, setting of GPIO is input mode (default). And it is possible to read the states of their pins from each bit of the GPIO register. On output mode, the written states of each bit are output. If GPIO functions are not used on the Serialized IRQ mode, no pull-up is required.

4.13 ZV port Interface

The R5C485 has Bypass type ZV port interface. On 16-bit interface, when ZV port Enable bit of either Misc Control 1 (82Fh) or Misc Control 2 (A0h) is enabled, CARDR [25:6], IOIS16#, INPACK#, SPKR# are assigned to ZV port input signal.
The R5C485 has no on chip buffer for ZV port interface. So if ZV port is enabled, the signals for ZV port such as CADR [25:4] will be “Hi-z” or “Input disable” and will be reconfigured as ZV port interface. The R5C485 outputs the control signal for the external buffer. Therefore, the buffer controls to switch sockets are enabled.

16 bit interface Signal Name	ZV Port Interface Signal Name	ZV Port card I/O [1]	Comments
A10	**HREF**	O	Horizontal Sync to ZV Port
A11	**VSYNC**	O	Vertical Sync to ZV Port
A9	**Y0**	O	Video Data to ZV Port YUV: 4:2:2 format
A8	**Y2**	O	Video Data to ZV Port YUV: 4:2:2 format
A13	**Y4**	O	Video Data to ZV Port YUV: 4:2:2 format
A14	**Y6**	O	Video Data to ZV Port YUV: 4:2:2 format
A16	**UV2**	O	Video Data to ZV Port YUV: 4:2:2 format
A15	**UV4**	O	Video Data to ZV Port YUV: 4:2:2 format
A12	**UV6**	O	Video Data to ZV Port YUV: 4:2:2 format
A7	**SCLK**	O	Audio SCLK PCM Signal
A6	**MCLK**	O	Audio MCLK PCM Signal
A[5::4]	**RESERVED**	RFU	Put in three state by Host Adapter No connection in PC Card
A[3::0]	**ADDRESS[3::0]**	I	Used for accessing PC Card
IOIS16#	**PCLK**	O	Pixel Clock to ZV Port
A17	**Y1**	O	Video Data to ZV Port YUV: 4:2:2 format
A18	**Y3**	O	Video Data to ZV Port YUV: 4:2:2 format
A19	**Y5**	O	Video Data to ZV Port YUV: 4:2:2 format
A20	**Y7**	O	Video Data to ZV Port YUV: 4:2:2 format
A21	**UV0**	O	Video Data to ZV Port YUV: 4:2:2 format
A22	**UV1**	O	Video Data to ZV Port YUV: 4:2:2 format
A23	**UV3**	O	Video Data to ZV Port YUV: 4:2:2 format
A24	**UV5**	O	Video Data to ZV Port YUV: 4:2:2 format
A25	**UV7**	O	Video Data to ZV Port YUV: 4:2:2 format
INPACK#	**LRCLK**	O	Audio LRCLK PCM signal
SPKR#	**SDATA**	O	Audio PCM Data signal

ZV Port Interface Pin Assignments

1. "I" indicates signal is input to PC Card, "O" indicates signal is output from PC Card.

4.14 Subsystem ID, Subsystem Vendor ID

The R5C485 supports Subsystem ID and Subsystem Vendor ID to meet PC98/99/2001 Design Requirements. There are three ways to write into the Subsystem ID register and the Subsystem Vendor ID register from the system through BIOS.

1. Write Enable bit (Misc Control 82-83h: bit6) control method.
   The BIOS can turn this bit on, change the Subsystem IDs, and turn it off.
2. Copy of the Subsystem ID and the Subsystem Vendor ID in PCI user defined space (C0h) method.
3. Load the Subsystem IDs from the Serial ROM method.
   Connecting VPPEN0 to pull-up enables to use the Serial ROM. The R5C485 has the Serial ROM interface, and load the Subsystem ID and the Subsystem Vendor ID after the PCI reset disabled.

This register is initialized only by GBRST#.

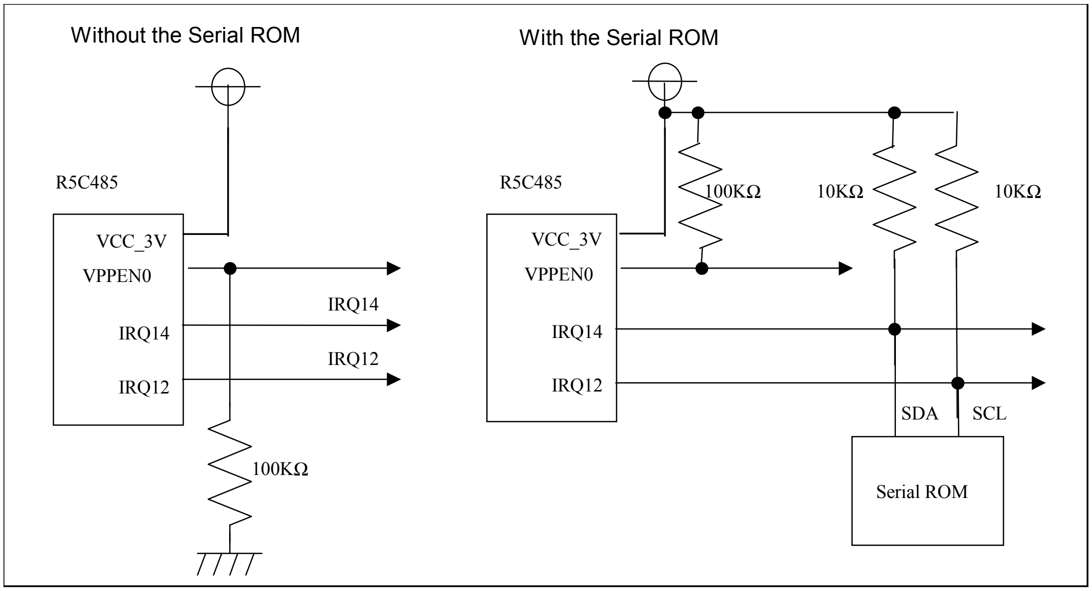
4.15 Serial ROM interface

The R5C485 supports the only read function of the external Serial ROM.
The R5C485 can load data for Subsystem ID/Subsystem Vendor ID (PCI Interface) from Serial ROM (I^{2}C BUS).

- 「I^{2}C BUS」is registered trademark of PHILIPS ELECTRONICS N.V.
  Purchase of Ricoh's I^{2}C components conveys a license under the Philips I^{2}C patent to use the components of the I^{2}C system, provided the system conforms to the I^{2}C specifications defined by Philips.

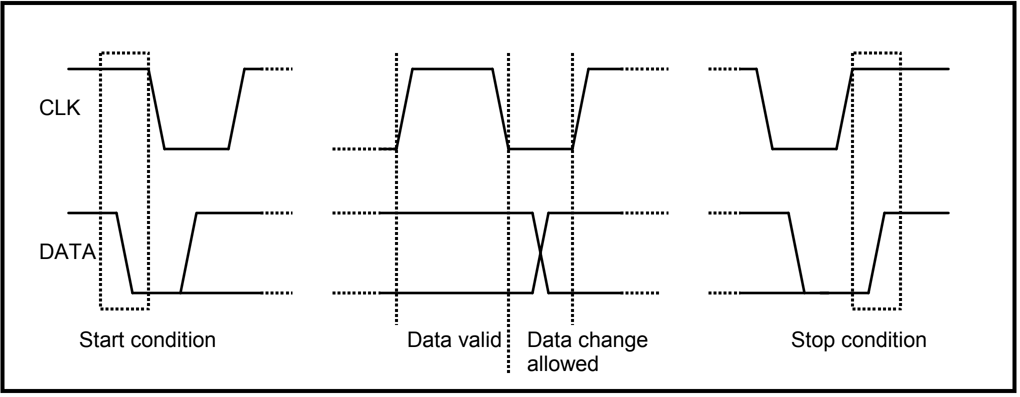
4.15.1 Serial ROM interface implementation

Connecting the VPPEN0 pin to pull-up resistor of 100KΩ enables to use the Serial ROM. When the first PCI Reset is deasserted, the R5C485 starts to sample VPPEN0 pin. When the VPPEN0 pin is connected to pull-up resistor of 100KΩ, the R5C485 attempts to load data through the Serial ROM. In this case, IRQ12 is reassigned to SCL (Clock signal) and IRQ14 is reassigned to SDA (Data signal). SDA (Data signal) and SCL (Clock signal) must be connected to VCC_3V through pull-up resistor of 10KΩ.
When the VPPEN0 pin is connected to pull-down resistor of 100 KΩ, the R5C485 does not load data through the Serial ROM. In this case, the function of IRQ12 and IRQ14 depends on setting of the Misc Control 4 register (See Ch.5.4.34).

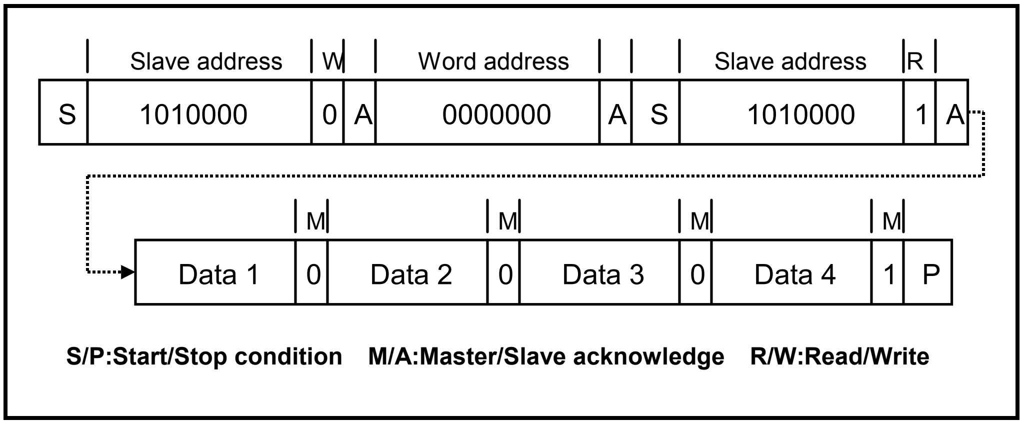

Without the Serial ROM
R5C485
VCC_3V
VPPEN0
IRQ14
IRQ12
IRQ14
IRQ12
100KΩ
With the Serial ROM
R5C485
VCC_3V
VPPEN0
IRQ14
IRQ12
100KΩ
10KΩ
10KΩ
SDA
SCL
Serial ROM

4.15.2 Serial ROM interface protocol

The CLK and DATA serial buses are bidirecrtional, and connected to pull-up. Both are in the high state while the R5C485 does not drive the Serial ROM.
The peculiar characteristic situation of "Start" condition and "Stop" condition occurs in communication procedure of Serial Bus. When the CLK line is in the high state, The “Start” condition is signaled by a high-to-low transition of the DATA line and the “Stop” condition is signaled by a low-to-high transition of the DATA line. The DATA line is enabled to change when the CLK line is in the low state. The data on the stable DATA line remains as the proper data during the high period of the CLK line. One clock pulse is formed every each data bit transmitted by the serial bus master.


CLK
DATA
Start condition
Data valid
Data change allowed
Stop condition

The serial bus master always generates “Start” condition and “Stop” condition. The serial bus becomes busy after “start” condition. And the serial bus becomes free again after “Stop” condition. Each byte on the DATA line is 8 bits long. The Acknowledge bit is required after each byte. The Acknowledge clock pulse is generated by the serial bus master.
The transmitter releases the DATA line to the high state, and the receiver pulls down the DATA line to the low state when the Acknowledge clock pulse is in the high state. The R5C485 works only as the serial bus master. As connecting with the Serial ROM, the R5C485 performs reading Double word when a PCI reset is deassert, and automatically loads the Subsystem vendor ID and the Subsystem ID. The Serial ROM interface protocol is as follows.


Slave address
W
Word address
Slave address
R
S
1010000
0
A
0000000
A
S
1010000
1
A
M
M
M
M
Data 1
0
Data 2
0
Data 3
0
Data 4
1
P
S/P:Start/Stop condition M/A:Master/Slave acknowledge R/W:Read/Write

4.15.3 Serial ROM Application

When the PCI bus is reset, and the Serial ROM interface is detected, the R5C485 starts to load the default from the Serial ROM. The Serial ROM data format is as follows.

ROM Address	Write Register Address	Register Name
00h	40h	Subsystem Vendor ID 7-0
01h	41h	Subsystem Vendor ID 15-8
02h	42h	Subsystem ID 7-0
03h	43h	Subsystem ID 15-8

The slave address of the Serial ROM is 1010000b. The R5C485 starts to load from the Serial ROM addressed at 1010000b. The read start address is set to 00000000b.

4.16 Power Up/Down Sequence

Follow the sequence when the power sequence is ON/OFF.

- On the power sequence is ON.

  1) Supply to VCC_CORE18V.
  2) Supply to VCC_3V.
  3) Supply to VCC_PCI3V.

- On the power sequence is OFF.

  1) Stop supplying to VCC_PCI3V.
  2) Stop supplying to VCC_3V.
  3) Stop supplying to VCC_CORE18V.

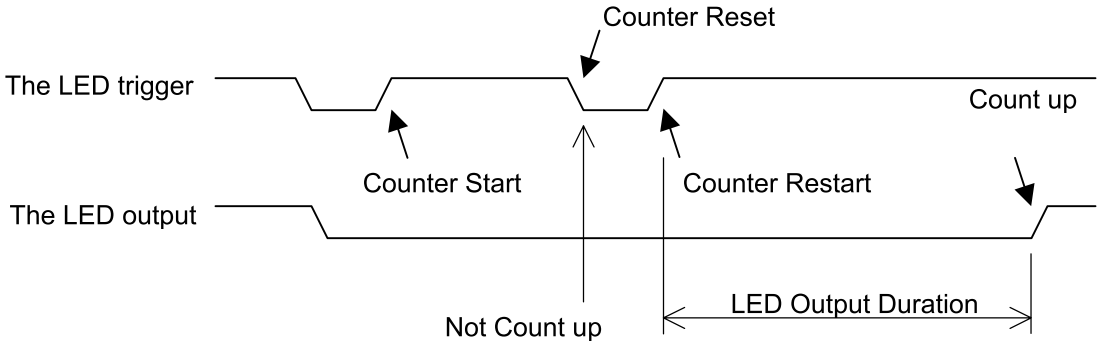
On the power sequence is on, sustain to timing of Global Reset (Chapter 8.3.6) in regards to the control of HWSPND# and GBRST#.

On the power sequence is off, a special limit for Delay Time is none.

4.17 LED# Output

The R5C485 enables to output the activity signals of the PC card as LED#. The R5C485 uses IRQx pins as LED#. Refer to the Misc Control 4 (Config.A4h) register as for how to use these pins. The default of the LED signal is 'Low' active. But it is possible to set the LED signal to 'high' active by setting the LED Polarity bit (Config, 82h bit11) to 1b.

The LED signal is asserted at the same time the trigger of its signal is asserted. And the internal counter works after the trigger is deasserted. In default, the LED signal is sustained for 64msec after the deassertion of the trigger, and is deasserted. When the trigger is reasserted on work of the counter, the counter is cleared and restarted to count up at the same time the deassertion of the LED signal. See as follows.



The LED Output Duration is selected from among 64msec(default), 1msec and No Duration time (through the trigger).

PCLK has operated a counter used for the LED Output Duration and therefore a stop request of PCLK by Clock_Run protocol is refused while the counter is worked. When PCLK must be stopped during 64msec on system, change the LED Output Duration.

4.17.1 PC Card LED (CardBus/R2)

The trigger signals of the PC Card LED are as follows. The R5C485 outputs as the PC Card LED.

CardBus:	CFRAM#, CINT#
R2:	Card command by IORD#, IOWR#, OE#, WE#, IREQ#

Bit 13 and bit 12 of the Config (func.0) A2h register enable to set the counter's hold time.
(These bits are set as the Ricoh Purpose register.)

bit 13	12	the LED Output Duration
0	0	64 msec (default)
1	1	1 msec
1	0	No Duration Time (through)
0	1	test mode(3.8µsec)

4.18 Notation

The following table shown the notation used in the register description.

NS	**not supported:** is used to indicate that registers and bits are not supported in R5C485. Writing to these registers and bits has no effect. Returns zero when read.
RO	**read only:** is used to indicate that registers and bits are read only type. Writing to these registers and bits has no effect.
R/W	**read/write:** is used to indicate that registers and bits are readable and writable.
WO	**write only:** is used to indicate that registers and bits are write only type. Writing to these registers and bits has no effect. Returns zero when read.
RC	**read clear:** is used to indicate that registers and bits are read only type. Reading these registers and all bits clear. Writing to these registers and bits has no effect.
R/WC	**read/write clear:** is used to indicate that registers and bits are readable and writable. Writing a 1 to these registers and bits clears the corresponding field. Writing a 0 to them has no effect.

5 PCI CONFIGURATION REGISTERS

5.1 Overview

The R5C485 supports PCI CardBus Bridge Interface functions for one PC Card socket. The configuration space can be configured in compliance with the PCI Local Bus Specification.

5.2 Configuration

The R5C485 supports only Type0 PCI configuration cycles (AD [1:0]=00). The bridge configuration registers for the socket A are addressed as a function #0 with AD [10:8] as shown in the following table. The R5C485 makes no response to attempted access of a register in the 1-7 function range and a PCI- master aborts.

AD [10:8]	**R5C485 PCI Function Addressed**	
000	#0	PCI-CardBus bridge for socket A
001-111	none	(Reserved)

5.3 Register Configuration

The R5C485 implements a 256 bytes configuration space. This space is divided into a predefined header space and a device dependent space. The first 128 bytes in a socket is defined the same predefined header format for all types of devices. The remaining 128 bytes are used as a unique configuration space.

The R5C485 configuration space is accessible only from the primary PCI bus. No other interfaces respond to configuration cycles. Based on the configuration command (Read/Write) and the C/BE [3:0]# lines, the R5C485 will provide data from selected register or write the data proffered. Read data will be all 32-bit DWORD register, regardless of byte enables, with the requested data driven in its natural byte location. Write data will be deposited into the selected register using the C/BE [3:0]# lines to enable the write.

The PCI configuration register is consisted of the 8-bit BYTE register, the 16-bit WORD register and the 32-bit DWORD register. During a configuration access cycle, the PCI configuration register is accessed using a 32-bit DWORD. The C/BE [3:0]# byte enable to access to specified BYTE/WORD registers.

Register Space Name: PCI-CARDBUS Bridge Configuration Space

<table>
<tr><th>31 24</th><th>23 16</th><th>15 8</th><th>7 0</th><th>Bit</th></tr>
<tr><td colspan="2">Device ID</td><td colspan="2">Vendor ID</td><td>00h</td></tr>
<tr><td colspan="2">PCI Status</td><td colspan="2">PCI Command</td><td>04h</td></tr>
<tr><td colspan="3">Class Code</td><td>Revision ID</td><td>08h</td></tr>
<tr><td>BIST</td><td>Header Type</td><td>PCI Latency Timer</td><td>Cache Line Size</td><td>0Ch</td></tr>
<tr><td colspan="4">Card Control Registers Base Address</td><td>10h</td></tr>
<tr><td colspan="2">CardBus Status</td><td>Reserved</td><td>Cap_Ptr</td><td>14h</td></tr>
<tr><td>CardBus Latency Timer</td><td>Subordinate Bus Number</td><td>CardBus Bus Number</td><td>PCI Bus Number</td><td>18h</td></tr>
<tr><td colspan="4">Memory Base 0</td><td>1Ch</td></tr>
<tr><td colspan="4">Memory Limit 0</td><td>20h</td></tr>
<tr><td colspan="4">Memory Base 1</td><td>24h</td></tr>
<tr><td colspan="4">Memory Limit 1</td><td>28h</td></tr>
<tr><td colspan="4">I/O Base 0</td><td>2Ch</td></tr>
<tr><td colspan="4">I/O Limit 0</td><td>30h</td></tr>
<tr><td colspan="4">I/O Base 1</td><td>34h</td></tr>
<tr><td colspan="4">I/O Limit 1</td><td>38h</td></tr>
<tr><td colspan="2">Bridge Control</td><td>Interrupt Pin</td><td>Interrupt Line</td><td>3Ch</td></tr>
<tr><td colspan="2">Subsystem ID</td><td colspan="2">Subsystem Vender ID</td><td>40h</td></tr>
<tr><td colspan="4">16-bit Legacy Mode Base Address</td><td>44h</td></tr>
<tr><td colspan="4">Reserved</td><td>48h ~ 7Ch</td></tr>
<tr><td colspan="2">Misc Control</td><td colspan="2">Bridge Configuration</td><td>80h</td></tr>
<tr><td colspan="2">Reserved</td><td colspan="2">16-bit Interface Control</td><td>84h</td></tr>
<tr><td colspan="2">16-bit Memory Timing 0</td><td colspan="2">16-bit I/O Timing 0</td><td>88h</td></tr>
<tr><td colspan="2">Reserved</td><td colspan="2">Reserved</td><td>8Ch</td></tr>
<tr><td colspan="4">DMA Slave Configuration</td><td>90h</td></tr>
<tr><td colspan="4">Reserved</td><td>94h ~ 9Ch</td></tr>
<tr><td colspan="2">Misc Control 3</td><td colspan="2">Misc Control 2</td><td>A0h</td></tr>
<tr><td colspan="4">Misc Control 4</td><td>A4h</td></tr>
<tr><td>Reserved</td><td>General Purpose I/O 1</td><td colspan="2">Reserved</td><td>A8h</td></tr>
<tr><td colspan="4">Reserved</td><td>ACh ~ BCh</td></tr>
<tr><td colspan="2">Writable Subsystem ID</td><td colspan="2">Writable Subsystem Vender ID</td><td>C0h</td></tr>
<tr><td colspan="4">Reserved</td><td>C4h ~ D8h</td></tr>
<tr><td colspan="2">Power Management Capabilities</td><td>Next Item Ptr</td><td>Capability ID</td><td>DCh</td></tr>
<tr><td>Data</td><td colspan="3">Power Management CSR</td><td>E0h</td></tr>
<tr><td colspan="4">Reserved</td><td></td></tr>
</table>

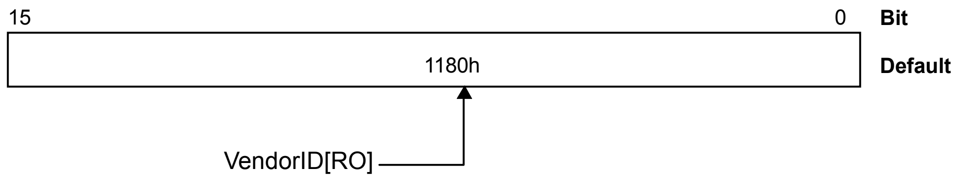
5.4 Register Description

5.4.1 Vendor ID register

Register Name:	Vendor ID
Address Offset:	00h-01h(16bit)
Default:	1180h
Access:	RO

This is a unique 16-bit value that is assigned to a vendor identification, and it is used with the Device ID in order to identify each PCI device. Writing to this register has no effect.

Register Name: Vendor ID
Address Offset: 00-01h (16bit)



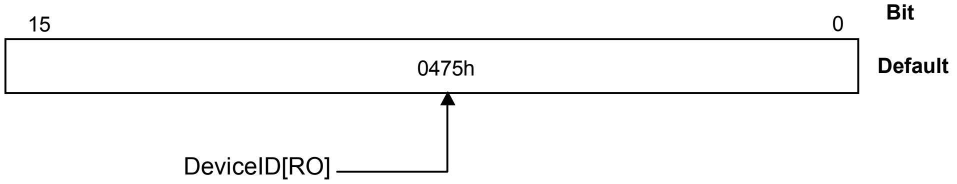
Bit	Field Name	Description
15-0	Vendor ID	This read-only field is the vendor identification assigned to RICOH by the PCI Special Interest Group. This field always returns 1180h when read.

5.4.2 Device ID register

Register Name:	Device ID
Address Offset:	02h-03h(16bit)
Default:	0475h
Access:	RO

This is a unique 16-bit value that is assigned to the PCI CardBus Bridge function, and it is used with the Vendor ID in order to identify each PCI device. Writing to this register has no effect.

Register Name: Device ID
Address Offset: 02-03h (16bit)

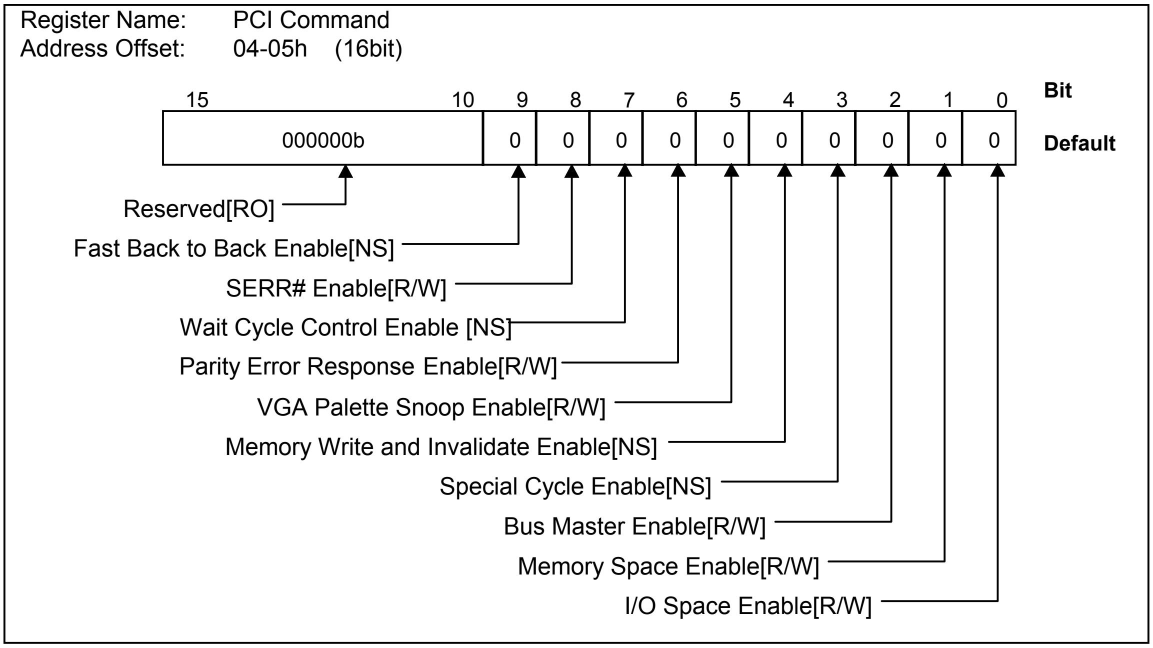


Bit	Field Name	Description
15-0	Device ID	This read-only field is the device identification assigned to the R5C485 by RICOH. This field always returns 0475h when read.

5.4.3 PCI Command register

Register Name:	PCI Command
Address Offset:	04h-05h(16bit)
Default:	0000h
Access:	NS, RO, R/W

The PCI Command Register controls the R5C485's responses to PCI Bus transactions on the primary interface. When this register has a value of '0', the function accepts only configuration accesses. The bits, with the exception of VGA Palette Snoop bit, in this register adhere to the definitions in the PCI Local Bus Specification.

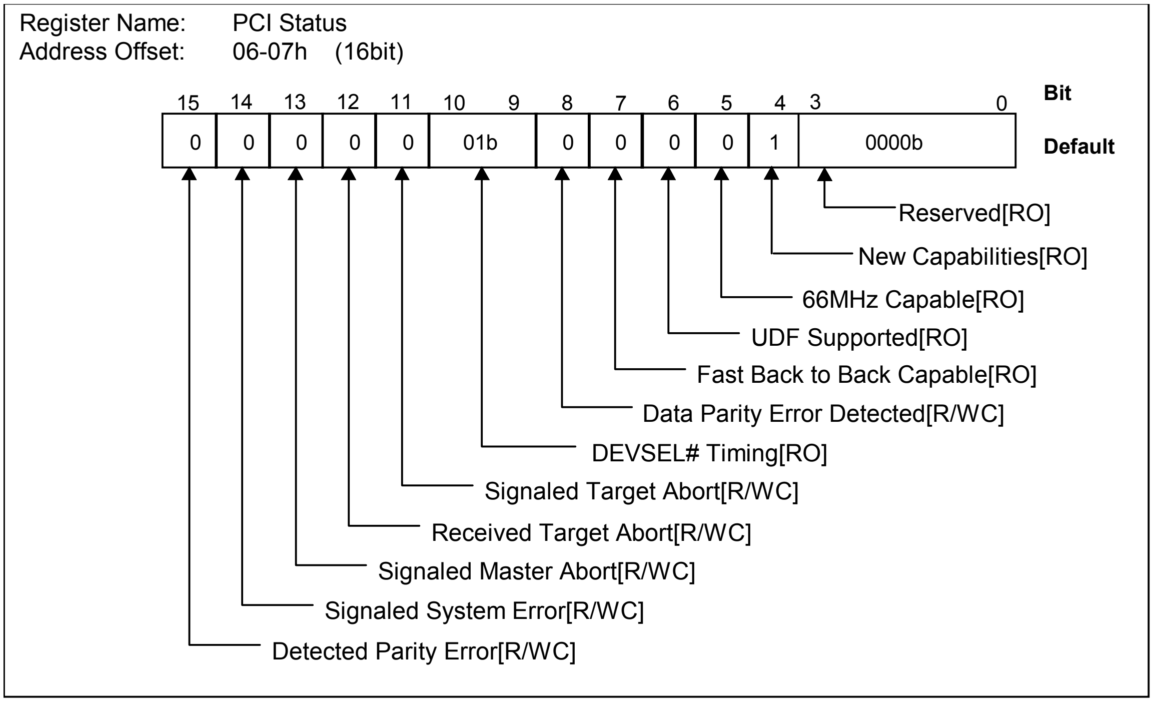

Register Name: PCI Command
Address Offset: 04-05h (16bit)
15
10
9
8
7
6
5
4
3
2
1
0
Bit
000000b
0
0
0
0
0
0
0
0
0
0
Default
Reserved[RO]
Fast Back to Back Enable[NS]
SERR# Enable[R/W]
Wait Cycle Control Enable [NS]
Parity Error Response Enable[R/W]
VGA Palette Snoop Enable[R/W]
Memory Write and Invalidate Enable[NS]
Special Cycle Enable[NS]
Bus Master Enable[R/W]
Memory Space Enable[R/W]
I/O Space Enable[R/W]

Bit	Field Name	Description
15-10	Reserved	This field reserved for future use by PCI Local Bus Specification. This field always returns zero when read.
9	Fast Back to Back Enable	This bit controls whether the PCI master dose fast back-to-back transactions or not. But, this function is not implemented in the R5C485. This bit always returns zero when read. Writing to this field has no effect.
8	SERR# Enable	This bit controls whether or not the SERR# output buffer is enabled on the PCI interface. The default after reset is zero. 0b disable the SERR# driver. 1b enable the SERR# driver. This bit must be set to report address parity errors.
7	Wait Cycle Control Enable	This bit controls whether or not a card does address/data stepping. But, this function is not implemented in the R5C485. This bit always returns zero when read. Writing to this field has no effect.
6	Parity Error Response Enable	This bit controls the device's response to parity errors. When this bit is set to 1, the R5C485 takes its normal action - enable an error bit and assert PERR#, when a parity error is detected. When this bit is set to 0, the R5C485 ignores any parity errors and continue normal operation. The default after reset is zero.
5	VGA Palette Snoop Enable	This bit controls the R5C485's response to VGA palette registers. When this bit is set to 1, palette snooping is enabled (AD [9:0] = 3C6h, 3C8h and 3C9h are decoded, AD [15:10] are not). The R5C485 forwards these addresses to the CardBus interface. Conversely, the R5C485 ignores to read from these addresses on the CardBus interface. When this bit is set to 0, the R5C485 ignores palette accesses. The default after reset is zero.
4	Memory Write and Invalidate Enable	This bit controls whether or not the PCI master uses the Memory Write and Invalidate command. But, this function is not implemented in the R5C485. This bit always returns zero when read. Writing to this field has no effect.
3	Special Cycle Enable	This bit controls an action on Special Cycle operations. But, this function is not implemented in the R5C485. This bit always returns zero when read. Writing to this field has no effect.
2	Bus Master Enable	This bit controls the R5C485's ability to operate as a master on the PCI interface. Setting this bit has no effect upon the configuration command operations. When this bit is set to 0, the R5C485 ignores all memory or I/O transactions on the CardBus interface. The default after reset is zero. 0b inhibit the R5C485 to operate as a master on the PCI interface. 1b allow the R5C485 to operate as a master on the PCI interface
1	Memory Space Enable	This bit controls the R5C485's response to memory accesses for both the memory mapped I/O ranges and the prefetchable memory ranges. The default after reset is zero. 0b ignore all memory transactions on the PCI interface, and the R5C485 DEVSEL# logic is inhibited during the memory cycle. 1b enable response to memory transactions on the PCI interface. And also, this bit controls accesses to the memory mapped I/O ranges that are defined in the Card Control Base Address register.
0	I/O Space Enable	This bit controls the R5C485's response to I/O accesses for transactions on the PCI interface. The default after reset is zero. 0b ignore all I/O transactions on the PCI interface, and the R5C485. DEVSEL# logic is inhibited during the I/O cycle. 1b enable response to I/O transactions on the PCI interface.

5.4.4 PCI Status register

Register Name:	PCI Status
Address Offset:	06h-07h(16bit)
Default:	0210h
Access:	RO, R/WC

This 16-bit register is used to record status information for PCI bus related events. These bits can be reset, but not set. A bit is reset whenever the register is written and the data in the corresponding bit location is a one. Writing a zero to this register has no effect. The bits in this register adhere to the definitions in the PCI Local Bus Specification, but only apply to the primary PCI interface.

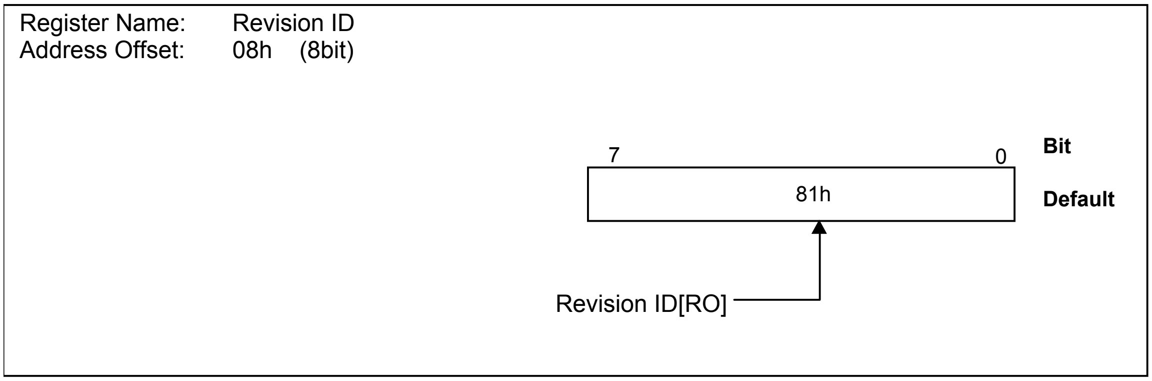

Register Name: PCI Status
Address Offset: 06-07h (16bit)
15
14
13
12
11
10
9
8
7
6
5
4
3
0
Bit
0
0
0
0
0
01b
0
0
0
0
1
0000b
Default
Reserved[RO]
New Capabilities[RO]
66MHz Capable[RO]
UDF Supported[RO]
Fast Back to Back Capable[RO]
Data Parity Error Detected[R/WC]
DEVSEL# Timing[RO]
Signaled Target Abort[R/WC]
Received Target Abort[R/WC]
Signaled Master Abort[R/WC]
Signaled System Error[R/WC]
Detected Parity Error[R/WC]

Bit	Field Name	Description
15	Detected Parity Error	This bit is set by the R5C485 whenever it detects a parity error, even if parity error handing is disabled (as controlled by bit 6 in the Command register). Writing a one to this bit clears the state.
14	Signaled System Error	This bit is set whenever the R5C485 asserts SERR#. Writing a one to this bit clears the state.
13	Signaled Master Abort	This bit is set by the R5C485 as a master device whenever its transaction is terminated with Master-abort. Writing a one to this bit clears the state.
12	Received Target Abort	This bit is set by the R5C485 as a master device whenever its transaction is terminated with Target-abort. Writing a one to this bit clears the state.
11	Signaled Target Abort	This bit is set by the R5C485 as a target device whenever its transaction is terminated with Target-abort. Writing a one to this bit clears the state.
10-9	DEVSEL# Timing	These bits encode the timing of DEVSEL#. These are encoded as 01b for medium speed. These bits are read-only. Writing to these bits has no effect.
8	Data Parity Error Detected	This bit is set when three conditions are met: 1) the bus agent asserted PERR# itself or observed PERR# asserted. 2) the agent setting the bit acted as the bus master for the operation in which the error occurred. 3) the Parity Error Response bit (Command register) is set. Writing a one to this bit has no effect.
7	Fast Back to Back Capable	This read-only bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. The R5C485 returns zero when read, because it is not capable of accepting fast back-to-back transactions. Writing to this bit had no effect.
6	UDF Supported	This read-only bit indicates whether or not the PCI device supports the UDF function. The R5C485 doesn't support the UDF function, and therefore returns a zero when read. Writing to this bit has no effect.
5	66MHz Capable	This read-only bit indicates whether or not the PCI device is capable of running at 66MHz. The R5C485 is capable of running only at 33MHz, and therefore returns a zero when read. Writing to this bit has no effect.
4	New Capabilities	This bit indicates whether PCI device implements a list of new capabilities such as PCI Power Management. The R5C485 implements it, and therefore returns a one when read. The register at 14h provides an offset into the configuration space pointing to the location of Power Management Register Block.
3-0	Reserved	These read-only bits are reserved for future use by PCI Local Bus specification. Return a zero when read. Writing to these bits has no effect.

5.4.5 Revision ID register

Register Name:	Revision ID
Address Offset:	08h(8bit)
Default:	81h
Access:	RO

This is a unique 8-bit value that is asserted to the device revision information. It is used with the Vendor ID and the Device ID in order to identify each PCI device. Writing to this register has no effect.

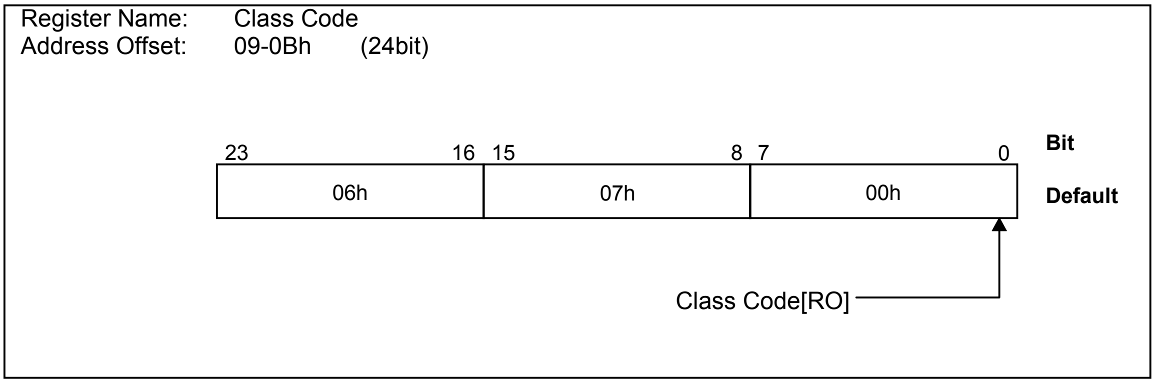

Register Name: Revision ID
Address Offset: 08h (8bit)
7
0
Bit
81h
Default
Revision ID[RO]

Bit	Field Name	Description
7-0	Revision ID	This read-only field is the revision identification number assigned to the R5C485 by RICOH. This field always returns 81h when read.

5.4.6 Class Code register

Register Name:	Class Code
Address Offset:	09h-0Bh(24bit)
Default:	060700h
Access:	RO

The Class Code register is read-only and is used to identify the generic function of the device. The bits in this register adhere to the definitions in the PCI Local Bus Specification. This register is formed into three byte-size fields; a base class code, a sub-class code and a programming interface. Writing to this register has no effect.

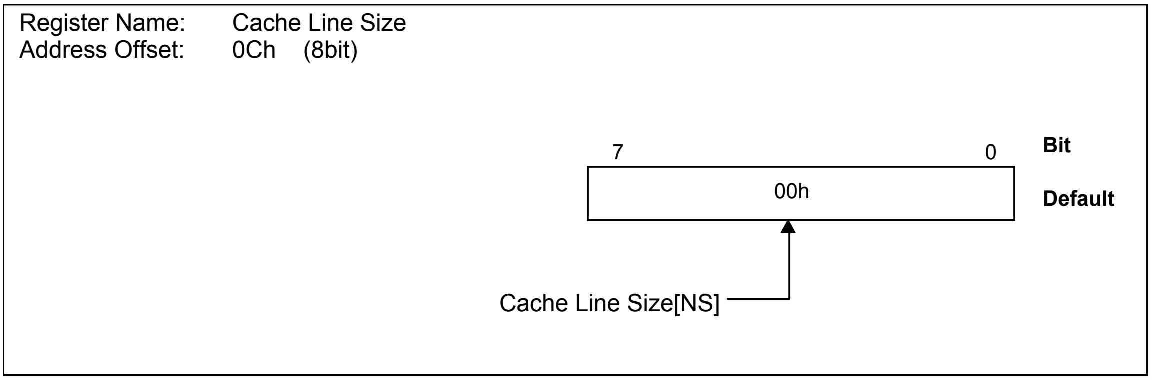


Bit	Field Name	Description
23-0	Class Code	This register is a read-only register and is used to identify the device. This register is formed into three byte-size fields. The upper byte (at offset 0Bh) is a base class code. The middle byte (at offset 0Ah) is a sub-class coded. The lower byte (at offset 09h) identifies a specific register-level programming interface. The R5C485 returns 060700h when this register is indicated as a PCI-CardBus bridge device; a base class of 06h (bridge device), a sub-class code of 07h (PCI to CardBus) and a programming interface of 00h. Writing to this register has no effect.

5.4.7 Cache Line Size register

Register Name:	Cache Line Size
Address Offset:	0Ch(8bit)
Default:	00h
Access:	NS

The Cache Line register specifies the system cache line size in units of 32-bit words. The R5C485 doesn't participate in the caching protocol, and therefore returns zero when read. Writing to this register has no effect.


Register Name: Cache Line Size
Address Offset: 0Ch (8bit)

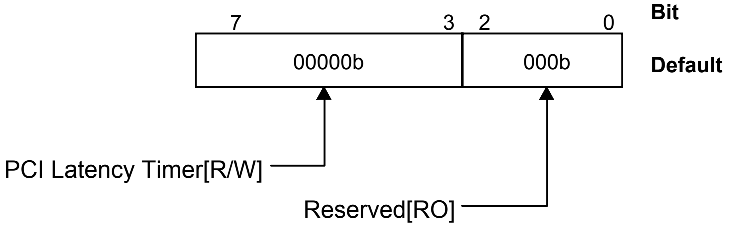
Bit	Field Name	Description
7-0	Cache Line Size	The R5C485 doesn't participate in the caching protocol. This register is read-only. Returns zero when read. Writing to this register has no effect.

5.4.8 PCI Latency Timer register

Register Name:	PCI Latency Timer
Address Offset:	0Dh(8bit)
Default:	00h
Access:	RO, R/W

The PCI Latency Timer specifies, in units of PCI bus clocks, the value of the Latency Timer for the PCI bus master. This register adheres to the PCI Local Bus Specification but applies only to the primary interface. The bottom three bits in this register are read-only and hardwired to 000b, resulting in a timer granularity of eight clocks.

Register Name: PCI Latency Timer
Address Offset: 0Dh (8bit)

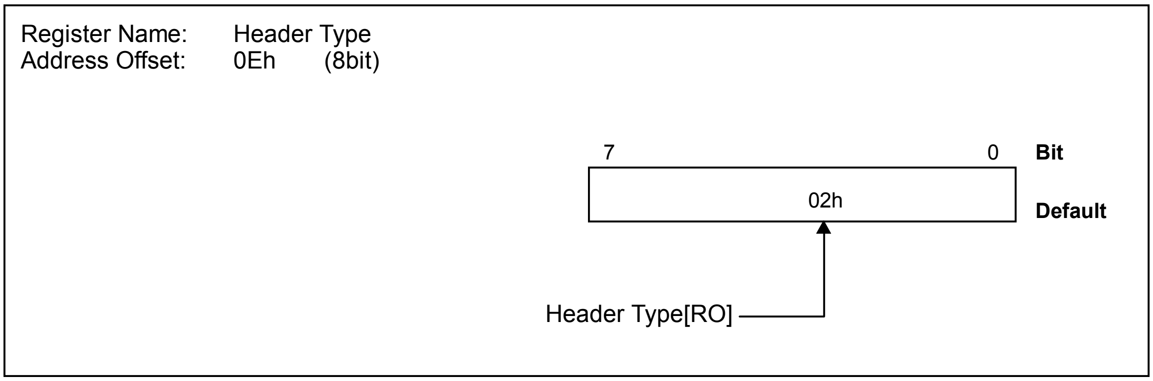


Bit	Field Name	Description
7-3	PCI Latency Timer	This register specifies, in units of PCI bus clocks, the value of the Latency Timer for the PCI bus master.
2-0	Reserved	The bottom three bits in this register are read-only and hardwired to 000b, resulting in a timer granularity of eight clocks. Writing to this field has no effect.

5.4.9 Header Type register

Register Name:	Header Type
Address Offset:	0Eh(8bit)
Default:	02h
Access:	RO

The Header Type register identifies the layout of bytes 10h through 3Fh in configuration space and also whether or not the device contains multiple functions. The R5C485 is a single-function device and the PCI-CardBus bridge and therefore returns 02h when read. Writing to this register has no effect.


Register Name: Header Type
Address Offset: 0Eh (8bit)
7
0
Bit
02h
Default
Header Type[RO]

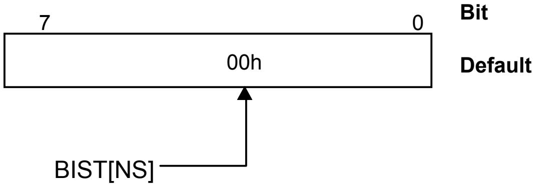
Bit	Field Name	Description
7-0	Header Type	This register identifies the layout of bytes 10h through 3Fh in configuration space and also whether or not the device contains multiple functions. Return 02h when read. Writing to this register has no effect.

5.4.10 BIST register

Register Name:	BIST
Address Offset:	0Fh(8bit)
Default:	00h
Access:	NS

The BIST register is used for control and status of BIST (Built In Self Test). The R5C485 does not implement BIST, and therefore returns zero when read.

Register Name: BIST
Address Offset: 0Fh (8bit)

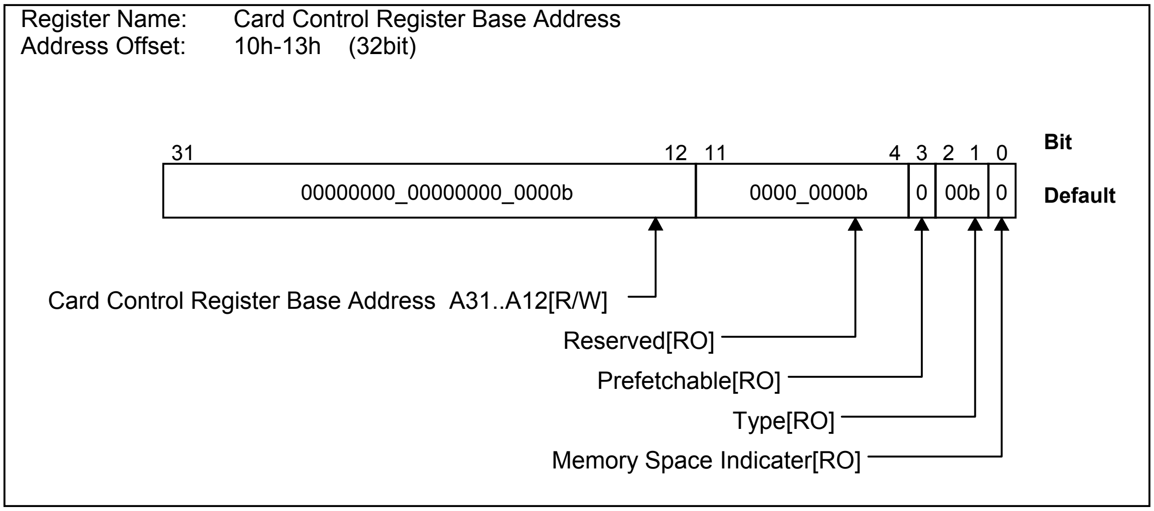


Bit	Field Name	Description
7-0	BIST	The R5C485 doesn't support this register. This read-only register always returns zero when read. Writing to this register has no effect.

5.4.11 Card Control Register Base Address register

Register Name:	Card Control Register Base Address
Address Offset:	10h(32bit)
Default:	0000_0000h
Access:	RO, R/W

The Card Control Register Base Address register points to the memory mapped I/O space that contains Status and Control registers for both the PC Card-32 and the PC Card-16. The upper bits [31:12] are read/write and the lower bits [11:0] are hardwired to zero. This indicates to Configuration software that the R5C485 must take 4K bytes of non-prefetchable memory space. The PC Card-32 (CardBus Card) Status and Control registers start at offset 000h (in the bottom 2K bytes) and the PC Card-16 registers start at offset 800h (in the top 2K bytes). The R5C485 dose not respond to PCI cycles unless specifically loaded with a non-zero address after PCIRST# is deasserted.

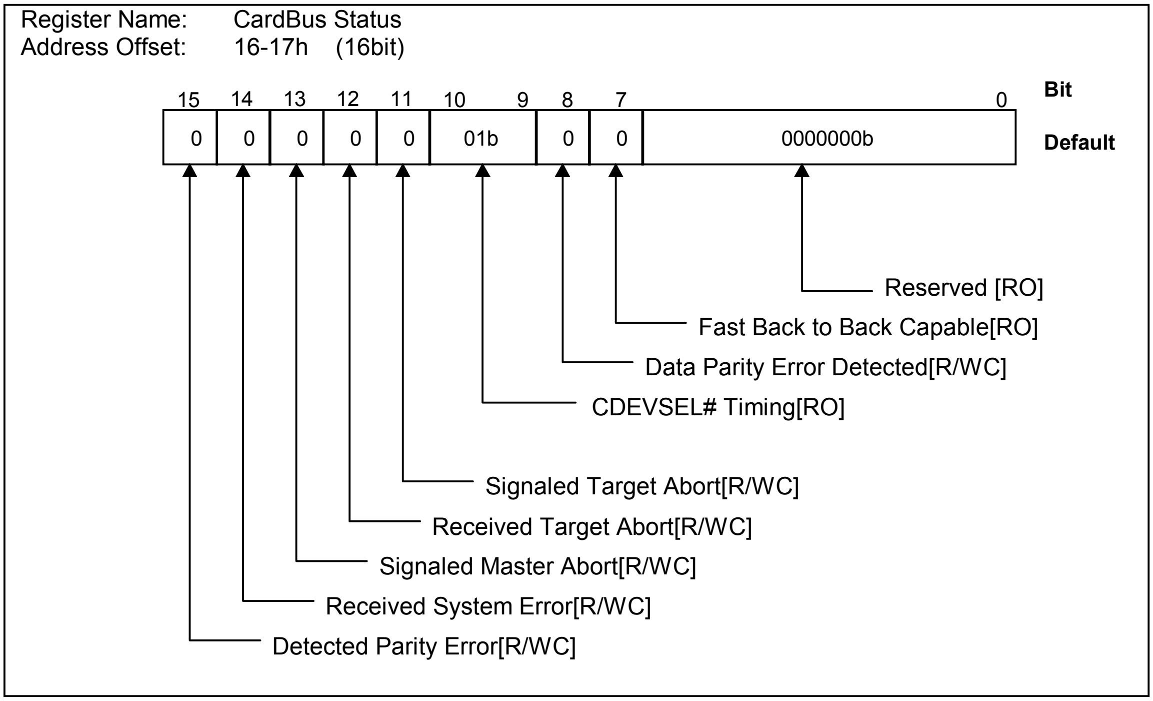

Register Name: Card Control Register Base Address
Address Offset: 10h-13h (32bit)
31
12
11
4
3
2
1
0
Bit
00000000_00000000_0000b
0000_0000b
0
00b
0
Default
Card Control Register Base Address A31..A12[R/W]
Reserved[RO]
Prefetchable[RO]
Type[RO]
Memory Space Indicater[RO]

Bit	Field Name	Description
31-12	Card Control Register Base Address A31..A12	These bits indicate the memory mapped I/O space that contains status and control registers for both the PC Card-32 and the PC Card-16. Bits [31:12] are read/write.
11-4	Reserved	These bits are read-only and hardwired to zero. Writing to this field has no effect.
3	Prefetchable	This bit is set to one when the data is prefetchable and reset to a zero otherwise. This filed is hardwired to zero in the R5C485. Writing to this field has no effect.
2-1	Type	These bits have encoded meanings as shown below for Memory Base Address registers. 00b locate anywhere in 32-bit address space 01b locate below 1M 10b locate anywhere in 64-bit address space 11b reserved This field is read-only and hardwired to zero in the R5C485. Writing to this field has no effect.
0	Memory Space Indicator	This bit indicates the Base Address register maps into either a memory space or an I/O space. This bit returns zero when the register maps into a memory space and one when the register maps into an I/O space. This bit is read-only and hardwired to zero in the R5C485. Writing to this field has no effect.

5.4.12 CardBus Status register

Register Name:	CardBus Status
Address Offset:	16h-17h(16bit)
Default:	0200h
Access:	RO, R/WC

The CardBus Status register is used to record status information for CardBus related events. These bits can be reset, but not be set. A bit is reset whenever the register is written and the data in the corresponding bit location is a one. Writing a zero to this register has no effect. The bits in this register adhere to the definitions in the PCI Local Bus Specification, but only apply to the secondary CardBus interface.

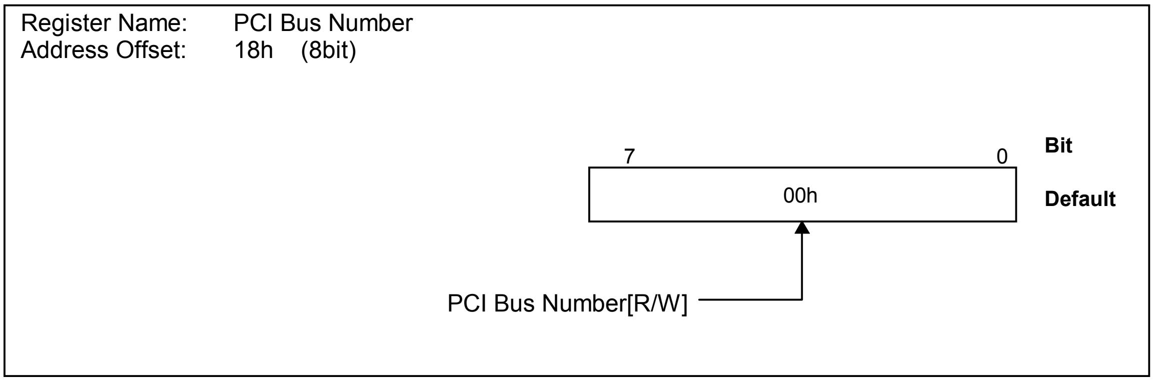

Register Name: CardBus Status
Address Offset: 16-17h (16bit)
15
14
13
12
11
10
9
8
7
0
Bit
0
0
0
0
0
01b
0
0
0000000b
Default
Reserved [RO]
Fast Back to Back Capable[RO]
Data Parity Error Detected[R/WC]
CDEVSEL# Timing[RO]
Signaled Target Abort[R/WC]
Received Target Abort[R/WC]
Signaled Master Abort[R/WC]
Received System Error[R/WC]
Detected Parity Error[R/WC]

Bit	Field Name	Description
15	Detected Parity Error	This bit is set by the R5C485 whenever it detects a parity error on the secondary bus, even if parity error handing is disabled (as controlled by bit 6 in the Command register). Writing a one to this bit clears the state.
14	Received System Error	This bit is set whenever the R5C485 receives CSERR#. Writing a one to this bit clears the state. When both CSERR# enable bit in the Bridge Control register and SERR# enable bit in the PCI Command register are set, the R5C485 asserts SERR# on the primary PCI bus whenever it receives CSEER#.
13	Signaled Master Abort	This bit is set by the R5C485 as a master device on the CardBus interface whenever its transaction is terminated with master-abort. Writing a one to this bit clears the state.
12	Received Target Abort	This bit is set by the R5C485 as a master device on the CardBus interface whenever its transaction is terminated with target-abort. Writing a one to this bit clears the state.
11	Signaled Target Abort	This bit is set by the R5C485 as a target device on the CardBus interface whenever its transaction is terminated with target-abort. Writing a one to this bit clears the state.
10-9	CDEVSEL# Timing	This field encodes the timing of CDEVSEL#. These read-only bits are encoded as 01b for medium speed in the R5C485. Writing to this field has no effect.
8	Data Parity Error Detected	This bit is set by a CardBus master when three conditions are met: 1) the bus agent asserted CPERR# itself or observed CPERR# asserted. 2) the agent setting the bit acted as the bus master for the operation in which the error occurred. 3) the Parity Error Response bit (Control register) is set. Writing a one to this bit clears the state.
7	Fast Back to Back Capable	This read-only bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not the same agent. The R5C485 returns a zero when read, because it is not capable of fast back-to-back transactions on the CardBus interface. Writing to this bit has no effect.
6-0	Reserved	This bit is reserved for future use by the PCI Local Bus specification. This field is read-only. Returns zero when read. Writing to this field has no effect.

5.4.13 PCI Bus Number register

Register Name:	PCI Bus Number
Address Offset:	18h(8bit)
Default:	00h
Access:	R/W

The PCI Bus Number register indicates the number of the PCI bus on the primary side of the R5C485. The appropriate configuration software sets this register. The R5C485 doesn't decode Type 1 configuration transactions on the CardBus interface that should be converted to Special Cycle transactions on PCI bus interface.



Register Name: PCI Bus Number
Address Offset: 18h (8bit)

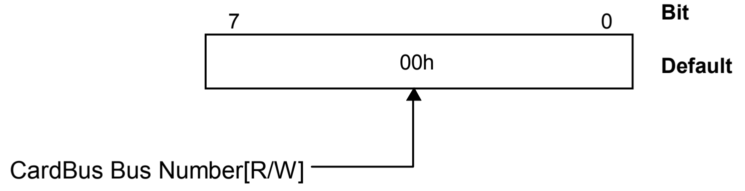
Bit	Field Name	Description
7-0	PCI Bus Number	This field indicates the number of the PCI bus on the primary side of the R5C485. This field is read/write, but this register has no effect upon the R5C485's operation. The default after reset is zero.

5.4.14 CardBus Bus Number register

Register Name:	CardBus Bus Number
Address Offset:	19h(8bit)
Default:	00h
Access:	R/W

The CardBus Bus Number register indicates the number of the CardBus attached to the socket. This read/write register is set by the appropriate configuration software, or the socket services software. The R5C485 uses this register to convert Type 1 configuration transactions on the primary (PCI) interface to Type 0 transactions on the secondary (CardBus) interface.

Register Name: CardBus Bus Number
Address Offset: 19h (8bit)

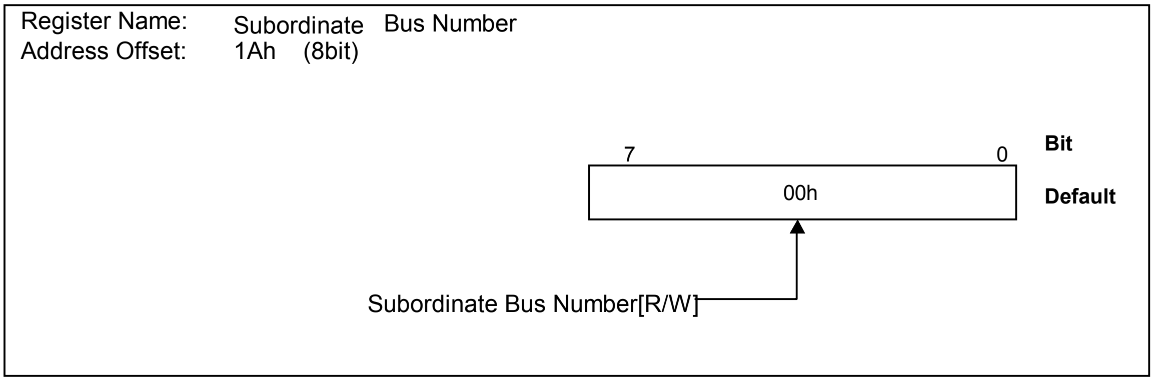


Bit	Field Name	Description
7-0	CardBus Bus Number	This register indicates the number of the CardBus attached to the socket. This is set by the appropriate configuration software or the socket services software. If the values of a Bus Number field agree with the values of this register on a Type 1 configuration transactions on the primary (PCI) interface, the R5C485 converts them to a Type 0 configuration transactions on the secondary (CardBus) interface. The default after reset is zero.

5.4.15 Subordinate Bus Number register

Register Name:	Subordinate Bus Number
Address Offset:	1Ah(8bit)
Default:	00h
Access:	R/W

The Subordinate Bus Number register is used to record the number of the bus at the lowest part of the hierarchy behind the bridge. This read/write register is set by the appropriate configuration software or the socket services software. Normally, a CardBus bridge will be at the bottom of the bus hierarchy and this register will hold the same value as the CardBus Bus Number register. The R5C485 uses this register in conjunction with the Card Bus Number register to convert Type 1 configuration transactions on the primary (PCI) interface to Type 0 or 1 configuration transactions on the secondary interface.


Register Name: Subordinate Bus Number
Address Offset: 1Ah (8bit)
7
0
Bit
00h
Default
Subordinate Bus Number[R/W]

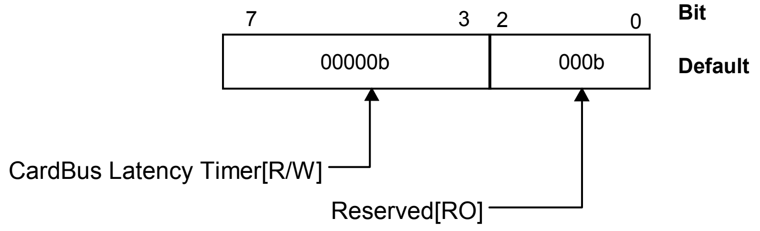
Bit	Field Name	Description
7-0	Subordinate Bus Number	This register is used to record the number of the bus at the lowest part of the hierarchy behind the R5C485. This read/write register is set by the appropriate configuration software, or the socket services software. Normally, a CardBus bridge will be at the bottom of the bus hierarchy and this register will hold the same value as the CardBus Bus Number register. When the value of Bus Number field is more over the CardBus Bus Number register's and less than this register's in Type 1 configuration cycles on the primary (PCI) interface, the R5C485 converts the value to Type1 configuration cycles on the secondary (CardBus) interface. The default after reset is zero.

5.4.16 CardBus Latency Timer register

Register Name:	CardBus Latency Timer
Address Offset:	1Bh(8bit)
Default:	00h
Access:	RO, R/W

The CardBus Latency Timer register has the same functionality of the primary PCI bus Latency Timer but applies to the CardBus attached to this specific socket. This is set by the PCI BIOS configuration software or the socket services software. This register adheres to the PCI Local Bus Specification but applies only to the primary interface. The bottom three bits in this register are read-only and hardwired to zeros, resulting in a timer granularity of eight clocks.

Register Name: CardBus Latency Timer
Address Offset: 1Bh (8bit)



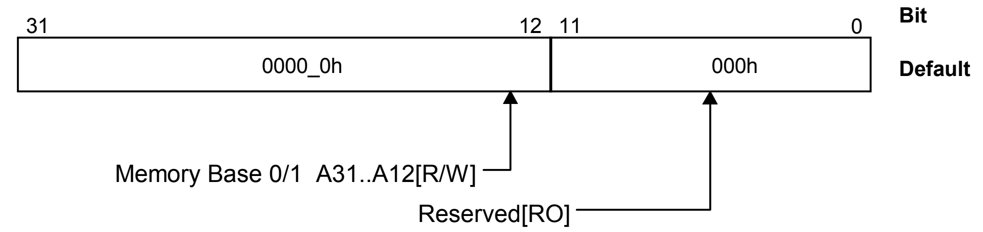
Bit	Field Name	Description
7-3	CardBus Latency Timer	This field specifies, in units of CardBus clocks, the value of the Latency Timer for the CardBus master.
2-0	Reserved	These bits are read-only and hardwired to 000b, resulting in a timer granularity of eight clocks. Writing to this field has no effect.

5.4.17 Memory Base 0/1 register

Register Name:	Memory Base 0/1
Address Offset:	#0: 1Ch-1Fh (32bit)
	#1: 24h-27h (32bit)
Default:	0000_0000h
Access:	RO, R/W

The Memory Base 0/1 register indicates the bottom address of a memory mapped I/O space 0/1. The upper 20-bits corresponds to address bits AD [31:12] that is read/write. The bottom 12-bits of this register is read-only and hardwired to zeros. The Memory Space Enable bit (bit1) in the Command register enables this window. The Memory 0/1 Prefetch Enable bit (bit8,9) in the Bridge Control register specifies whether the memory window is prefetchable or non-prefetchable. The default of this bit is prefetchable, but this bit must be non-prefetchable only when side effects are caused by memory read command on the installed CardBus card. This register has no meaning for PC Card-16.

Register Name: Memory Base 0/1
Address Offset: 1Ch-1Fh/24h-27h (32bit)



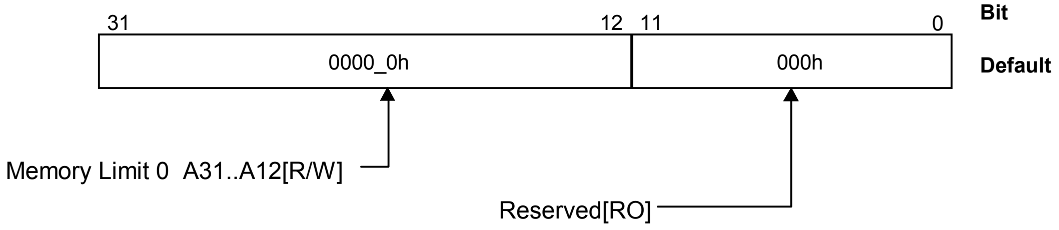
Bit	Field Name	Description
31-12	Memory Base 0/1 A31..A12	This register indicates the base address of a memory mapped I/O range that is used by the R5C475 to determine when to forward memory transactions from PCI interface to CardBus interface. This field is read/write.
11-0	Reserved	This field is read-only and hardwired to zeros. Writing to this field has no effect.

5.4.18 Memory Limit 0/1 register

Register Name:	Memory Limit 0/1
Address Offset:	#0: 20h-23h (32bit) #1: 28h-2Bh (32bit)
Default:	0000_0000h
Access:	RO, R/W

The Memory Limit 0/1 register indicates the top address of the memory mapped I/O space 0/1. The upper 20-bits corresponds to address bits AD [31:12] that are read/write. The bottom 12-bits of this register is read-only and hardwired to zeros. The bridge assumes the bottom address bits [11:0] are ones when the address range is decoded. So if the Memory Base and Limit registers are set to the same value, a window of 4Kbyte is defined. Both Memory windows #0 and #1 are enabled by the Memory Space Enable bit in the PCI Command register. To disable either window individually, the Limit register of that range should be set below the Base register. This will cause the bridge to never detect a hit on that window. This register has no meaning for PC Card-16.

Register Name: Memory Limit 0/1
Address Offset: 20h-23h/28h-2Bh (32bit)



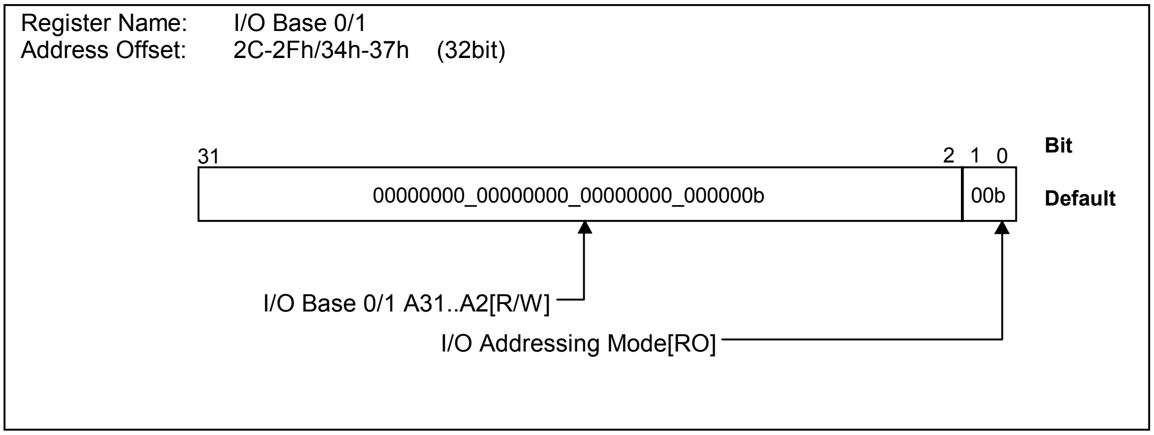
Bit	Field Name	Description
31-12	Memory Limit 0/1 A31..A12	This field indicates the top address of a PCI memory address range that is used by the R5C485 to determine when to forward memory transactions from the PCI interface to the CardBus interface.
11-0	Reserved	This field is read-only and hardwired to zeros. Writing to this field has no effect.

5.4.19 I/O Base 0/1 register

Register Name:	I/O Base 0/1
Address Offset:	#0: 2Ch-2Fh(32bit)
	#1: 34h-37h (32bit)
Default:	0000_0000h
Access:	RO, R/W

The I/O Base 0/1 register indicates the bottom address of a PCI I/O address range that used by the R5C485 to determine when to forward an I/O transaction to the CardBus. The upper bits of this register corresponding to AD [31:2] are read/write, and the lower bits corresponding to AD [1:0] are read-only. AD [1:0] are fixed to 00b on the R5C5485's 16bit I/O addressing mode, and 01b on the R5C485's 32bit I/O addressing mode. Therefore, each 4byte of I/O space 0/1 is enabled.

If these bits have the value 0, then the bridge implements only 16-bit I/O addressing and assumes that the upper 16 address bits AD [31:16] of the I/O base address register are zero. And if they have the value 1, then the bridge implements 32-bit I/O addressing and the 16 bits of the base register hold the upper 16 bits corresponding to AD [31:16] of the 32-bit I/O address space. The I/O Space Enable bit in the PCI Command register enables these I/O window 0/1. This register has no meaning for PC Card-16.

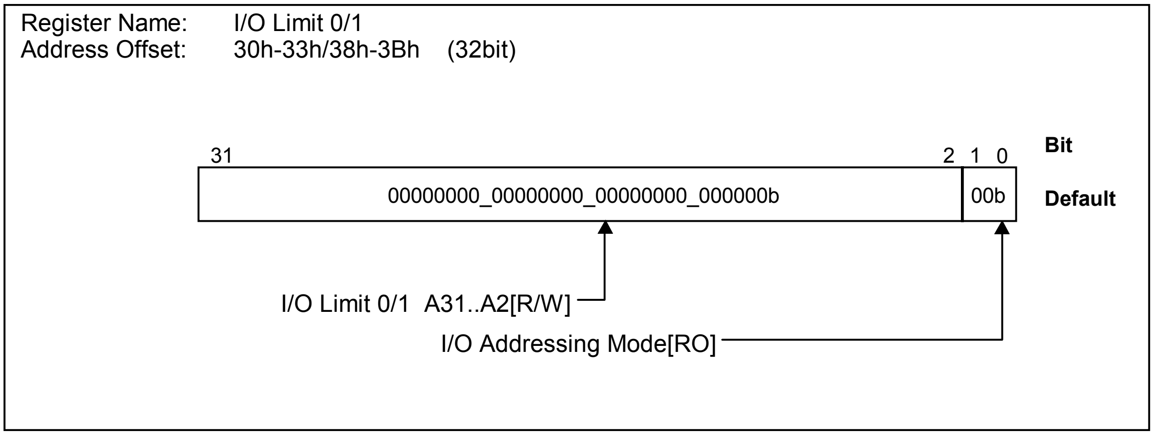

Register Name: I/O Base 0/1
Address Offset: 2C-2Fh/34h-37h (32bit)
31
2 1 0
Bit
00000000_00000000_00000000_000000b
00b
Default
I/O Base 0/1 A31..A2[R/W]
I/O Addressing Mode[RO]

Bit	Field Name	Description
31-2	I/O Base 0/1 A31..A2	This field indicates the base address of an address range that is used by the R5C485 to determine when to forward an I/O transaction from PCI interface to the CardBus interface.
1-0	I/O Addressing Mode	This field is read-only and returns 00b on the 16-bit I/O addressing mode, and returns on 01b on the 32-bit addressing mode. Writing to this field has no effect.

5.4.20 I/O Limit 0/1 register

Register Name:	I/O Limit 0/1
Address Offset:	#0: 30-33h (32bit) #1: 38h-3Bh (32bit)
Default:	0000_0000h
Access:	RO, R/W

The I/O Limit 0/1 register indicates the top address of an address range that is used by the R5C485 to determine when to forward an I/O transaction to the CardBus. The upper bits of this register correspond to AD [31:2] are read/write, and the lower bits AD [1:0] are read-only. AD [1:0] are fixed to 00b the R5C485's 16bit I/O addressing mode, and 01b on the R5C485's 32bit I/O addressing mode. Therefore, each 4byte of I/O space 0/1 is enabled.
The I/O Space Enable bit in the PCI Command register enables I/O windows #0 and #1. This register has no meaning for PC Card-16.


Register Name: I/O Limit 0/1
Address Offset: 30h-33h/38h-3Bh (32bit)
31
2 1 0
Bit
00000000_00000000_00000000_000000b
00b
Default
I/O Limit 0/1 A31..A2[R/W]
I/O Addressing Mode[RO]

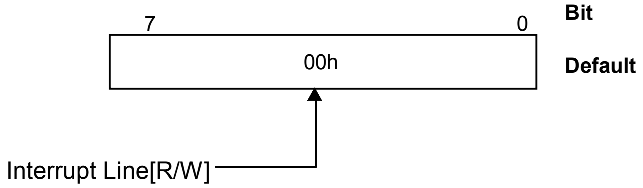
Bit	Field Name	Description
31-2	I/O Limit 0/1 Lower A31..A2	This field indicates the limit address of an address range that is used by the R5C485 to determine when to forward an I/O transaction from the PCI interface to the CardBus interface.
1-0	I/O Addressing Mode	This field is read-only and returns 00b on the 16-bit I/O addressing mode, and returns 01b on the 32-bit I/O addressing mode. Writing to this field has no effect.

5.4.21 Interrupt Line register

Register Name:	Interrupt Line
Address Offset:	3Ch(8bit)
Default:	00h
Access:	R/W

The Interrupt Line register is read/write register used to communicate interrupt line routing information. This register must be initialized by BIOS software on the system configuration, so a default state is no specified. The value in this register indicates which input of the system interrupt controller the interrupt pin in the R5C485 is connected to. The default after reset is 00h.

Register Name: Interrupt Line
Address Offset: 3Ch (8bit)

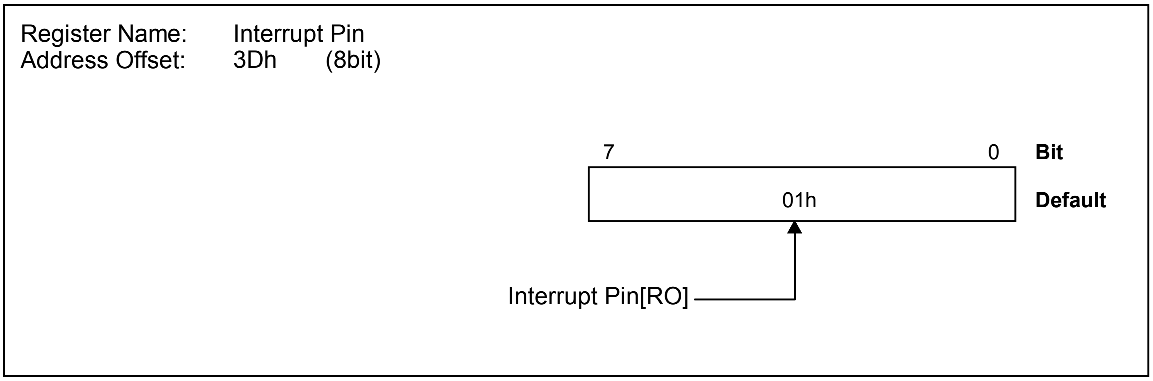


Bit	Field Name	Description
7-0	Interrupt Line	The value in this register indicates which input of the system interrupt controller the interrupt pin in the R5C485 is connected to. The default after reset is 00h.

5.4.22 Interrupt Pin register

Register Name:	Interrupt Pin
Address Offset:	3Dh(8bit)
Default:	01h
Access:	RO

The Interrupt Pin register is read-only register that adheres to the definition in the PCI Local Bus Specification. This register indicates which interrupt pin the R5C485 use. A value of 01h corresponding to INTA# is assigned to socket. The SR_PCI_INT_Select bit in the Misc Control register changes value of this register.

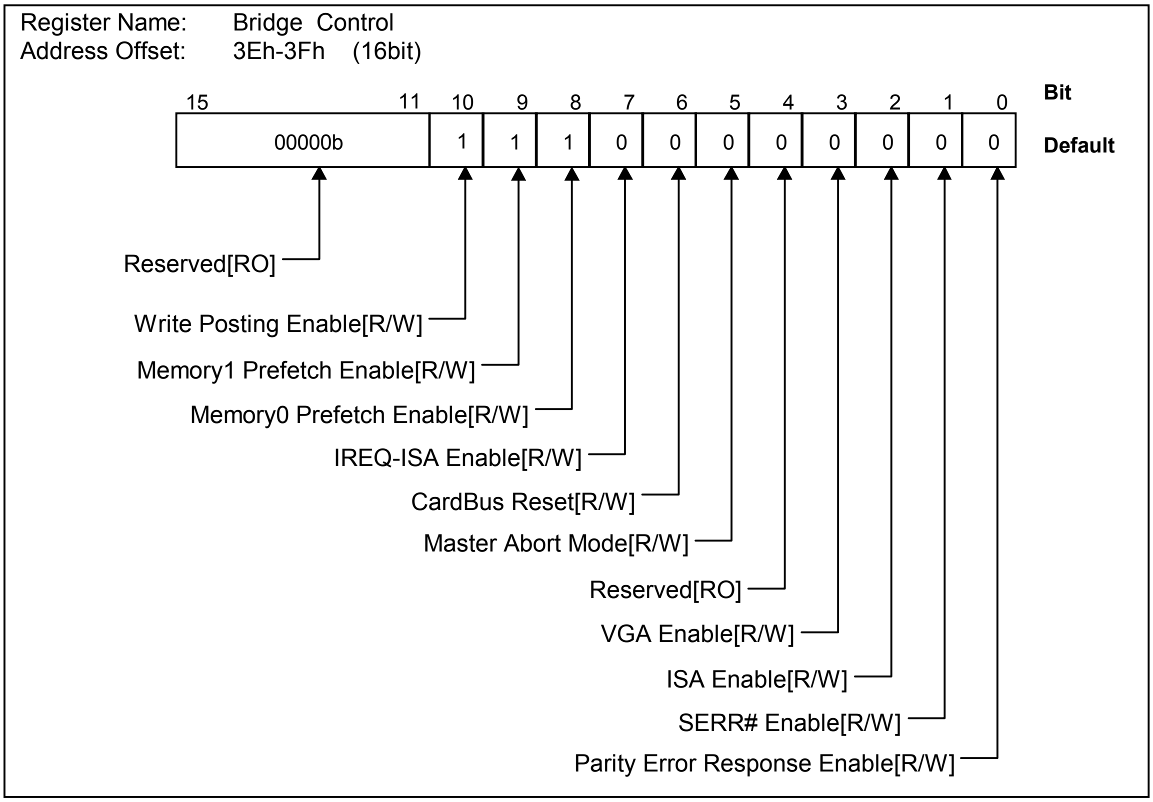

Register Name: Interrupt Pin
Address Offset: 3Dh (8bit)

Bit	Field Name	Description
7-0	Interrupt Pin	This field is read-only and returns 01h for socket. The SR_PCI_INT_Select bit in the Misc Control register changes value of this register.

5.4.23 Bridge Control register

Register Name:	Bridge Control
Address Offset:	3Eh-3Fh(16bit)
Default:	0700h
Access:	RO, R/W

The Bridge Control register provides control over the R5C485's bridging functions. Each bit in this register adheres to the definitions in the PC Card Standard.


Register Name: Bridge Control
Address Offset: 3Eh-3Fh (16bit)
15
11
10
9
8
7
6
5
4
3
2
1
0
Bit
00000b
1
1
1
0
0
0
0
0
0
0
0
Default
Reserved[RO]
Write Posting Enable[R/W]
Memory1 Prefetch Enable[R/W]
Memory0 Prefetch Enable[R/W]
IREQ-ISA Enable[R/W]
CardBus Reset[R/W]
Master Abort Mode[R/W]
Reserved[RO]
VGA Enable[R/W]
ISA Enable[R/W]
SERR# Enable[R/W]
Parity Error Response Enable[R/W]

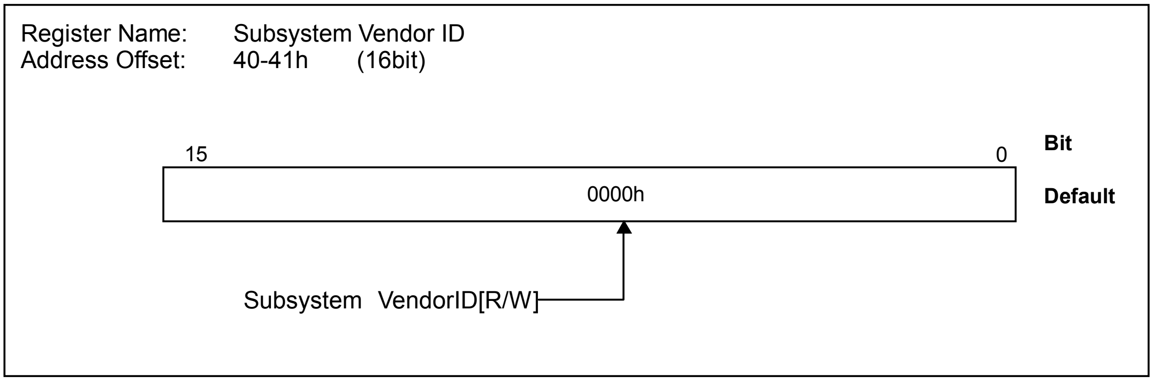
Bit	Field Name	Description
15-11	Reserved	This field is read-only and returns zeros. Writing to this field has no effect.
10	Write Posting Enable	This bit enables posting of Write data to and from the socket. If this bit is not set, the bridge must drain any data in its buffers before accepting data for or from the socket. The target must accept each data word before the bridge can accept the next word from the source master. The bridge must not release the source master, until the target accepts the last word. Operating with write posting disabled will inhibit system performance. This bit is encoded as: 0b Write Posting Disabled 1b Write Posting Enabled (default)
9	Memory 1 Prefetch Enable	This bit specifies whether the memory window #1 is prefetchable or non-prefetchable. This bit is encoded as: 0b the memory window #1 is non-prefetchable. 1b the memory window #1 is prefetchable. The default after reset is one.

Bit	Field Name	Description
8	Memory 0 Prefetch Enable	This bit specifies whether the memory window #0 is prefetchable or non-prefetchable. This bit is encoded as: 0b the memory window #0 is non-prefetchable. 1b the memory window #0 is prefetchable. The default after reset is one.
7	IREQ-ISA Enable	This bit controls the function interrupt for the PC Card-16/CardBus Card. When this bit is set to one, the IREQ#/CINT# interrupt is routed to the ISA system interrupt pins IRQ [15:3] that are indicated by the Interrupt General Control register. When it is set to zero, the IREQ# interrupt is routed to INTA# that is the PCI interrupt pin. When this bit controls the function interrupt output pin for the CardBus Card, CINT-ISA Disable bit must be cleared. The default after reset is zero.
6	CardBus Reset	When this bit is set to one, the R5C485 assert and hold CRST#. When this bit is cleared, they deassert CRST#. This bit can be set by software. It can also be set by hardware when the R5C485 executes the power down sequence. CRST# is a wired-OR of this bit and PCIRST#.
5	Master Abort Mode	When the R5C485 is a Master, this bit controls the behavior of the R5C485 when a master abort occurs on either PCI or CardBus interface. When this bit is cleared, the R5C485 returns ones if a master abort occurs during the read transaction, and the R5C485 annuls the data if a master abort occurs during the write transaction. When this bit is set to one, if the corresponding transaction on the opposite bus terminates with a master abort without completing the transaction on the source side (reads and non-posted writes), the R5C485 signals a target abort to the requesting master. And the R5C485 asserts SERR# on the PCI bus when the transaction on the source side and SERR# is enabled in the Command register. The default after reset is zero.
4	Reserved	This bit is read-only and returns zero. Writing to this bit has no effect.
3	VGA Enable	This bit controls the R5C485's response to VGA compatible addresses. When the VGA enable bit is set, the R5C485 forward transactions in the following ranges to the CardBus interface. Memory: 000A0000h to 000BFFFFh I/O: AD [9:0] = 3B0h to 3BBh, 3C0h to 3DFh (inclusive of ISA address aliases - AD [15:10] are not decoded.) On the other hand, the R5C485 make no response to transactions in the same ranges from the CardBus interface. The I/O and Memory Enable bit in the Command register affects the forwarding of these addresses. The default after reset is zero.
2	ISA Enable	This bit controls the R5C485's access to ISA compatible addresses that adhere to the first 64 Kbytes of PCI I/O space. When the ISA Enable bit is set, the R5C485 forward the only first 64 Kbytes from the PCI to the CardBus and block forwarding the last 768 bytes in 1 K block. In the opposite direction (CardBus to PCI) I/O transactions, the last 768 bytes in 1K block are forwarded. The default after reset is zero.
1	SERR# Enable	This bit controls whether or not the R5C485 forward an assertion of CSERR# on the CardBus interface to SERR# on the PCI interface. 0b CSERR# is not forwarded to PCI. 1b CSERR# is forwarded to PCI. The default after reset is zero.
0	Parity Error Response Enable	This bit controls the R5C485's response to parity errors on the CardBus interface. 0b Parity errors are ignored. 1b Parity errors are reported. The default after reset is zero.

5.4.24 Subsystem Vendor ID register

Register Name:	Subsystem Vendor ID
Address offset:	40h-41h(16bit)
Default:	0000h
Access:	R/W

The R5C485 supports Subsystem Vendor ID register in order to correspond to the PC 98/99/2001 Design requirements. Setting Subsystem ID Write Enable bit (Bit6 in the Misc Control register) enables the system to write into this register. And also, this register is reflected the written value of C0h (Writable Subsystem Vendor ID register) independent of Write Enable bit. On use of the Serial ROM, Data is read from the Serial ROM. Only GBRST# can initialize this register.

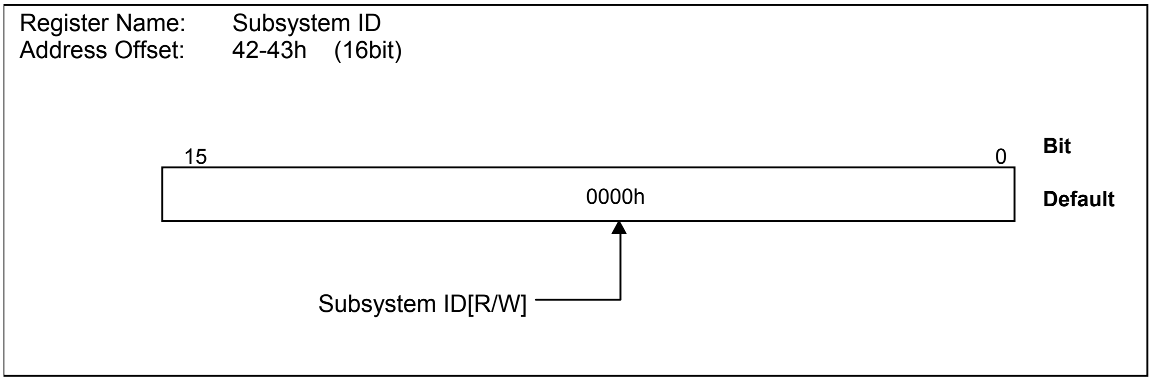

Register Name: Subsystem Vendor ID
Address Offset: 40-41h (16bit)
15
0
Bit
0000h
Default
Subsystem VendorID[R/W]

Bit	Field Name	Description
15-0	Subsystem Vendor ID	Setting Subsystem ID Write Enable bit (Bit6 in the Misc Control register) enables the system to write into this register. And also, this register is reflected the written value of C0h (Writable Subsystem Vendor ID register) independent of Write Enable bit. The default after reset is zeros.

5.4.25 Subsystem ID register

Register Name:	Subsystem ID
Address Offset:	42h-43h(16bit)
Default:	0000h
Access:	R/W

The R5C485 supports Subsystem ID register in order to correspond to the PC 98/99/2001 Design requirements. Setting Subsystem ID Write Enable bit (Bit6 in the Misc Control register) enabled to write into this register from the system. And also, this register is reflected the written value of C2h (Writable Subsystem Vendor ID register) independent of Write Enable bit. On use of the Serial ROM, Data is read from the Serial ROM. Only GBRST# can initialize this register.

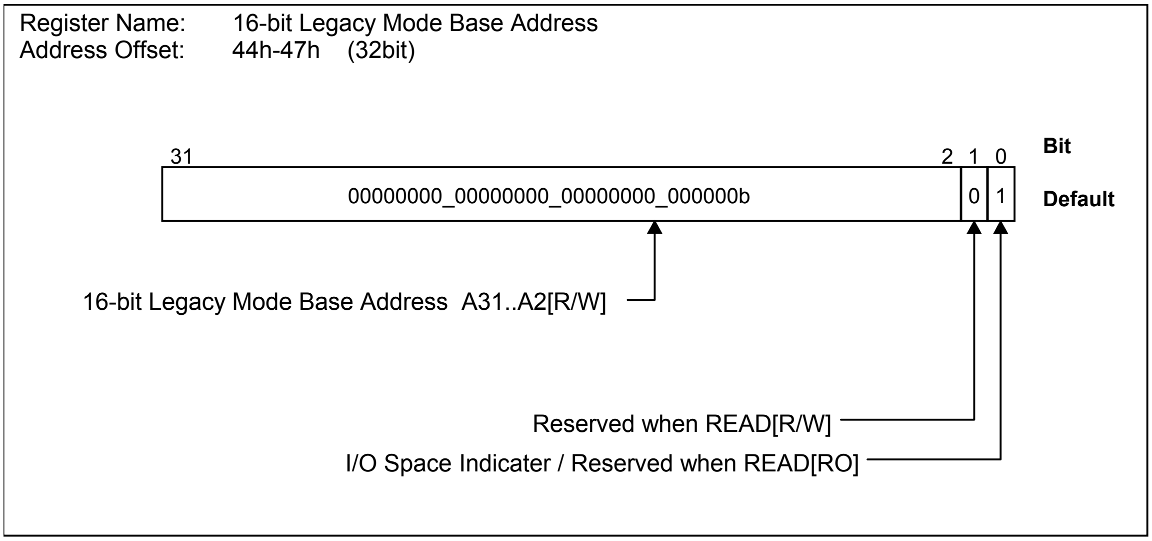


Bit	Field Name	Description
15-0	Subsystem ID	Setting Subsystem ID Write Enable bit (Bit6 in the Misc Control register) enabled to write into this register from the system. And also, this register is reflected the written value of C2h (Writable Subsystem Vendor ID register) independent of Write Enable bit. The default after reset is zeros.

5.4.26 16-bit Legacy Mode Base Address register

Register Name:	16-bit Legacy Mode Base Address
Address Offset:	44h-47h (32bit)
Default:	0000_0001h
Access:	RO, R/W

The 16-bit Legacy Mode Base Address register indicates the base address to map the Legacy Port on the PCI Card-16. Normally, this register is set to 3E0h or 3E2h in order to keep corresponding to the PCIC. The bits [31:2] are read/write, but the bits [1:0] are hardwired to 01b when read. It dose not respond to PCI cycles unless specifically loaded with a non-zero address after PCIRST# is deasserted.

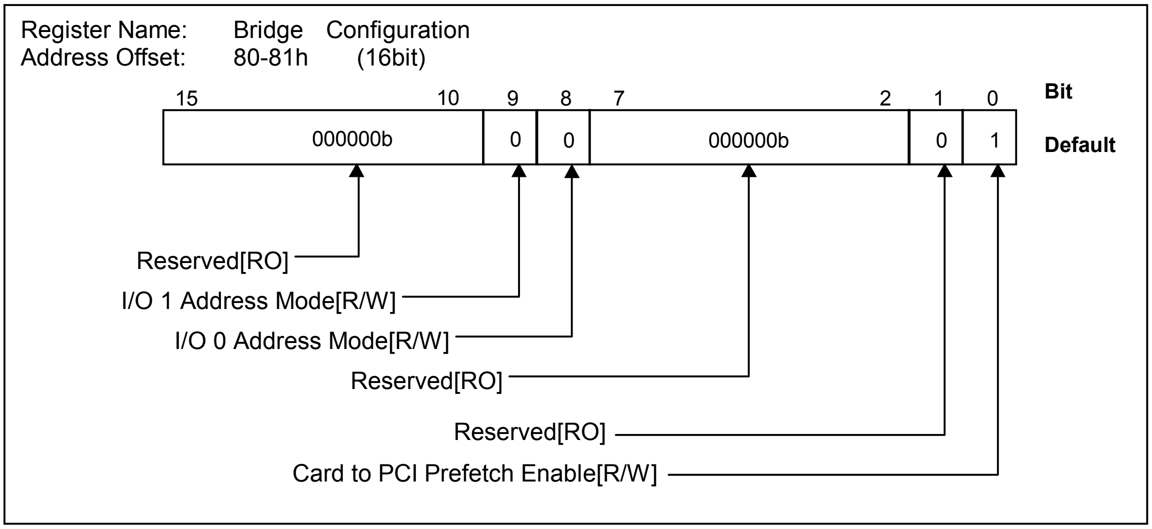

Register Name: 16-bit Legacy Mode Base Address
Address Offset: 44h-47h (32bit)
31
2
1
0
Bit
00000000_00000000_00000000_000000b
0
1
Default
16-bit Legacy Mode Base Address A31..A2[R/W]
Reserved when READ[R/W]
I/O Space Indicater / Reserved when READ[RO]

Bit	Field Name	Description
31-2	16-bit Legacy Mode Base Address A31..A2	This field indicates the base address to map INDEX/DATA port (3E0h, 3E1h) corresponding to the PCIC when the PCI Card-16 is inserted. This field is read/write, and writing to this field has no effect. The default after reset is zero.
1	Reserved	This bit is enabled to write in a data. Therefore, this register can be 03E0h or 03E2h. This bit returns zero when read.
0	I/O Space Indicator	This bit indicates whether or not the Card Control register space indicated by the Base Address register is I/O space. This bit returns one when read.

5.4.27 Bridge Configuration register

Register Name:	Bridge Configuration
Address Offset:	80h-81h(16bit)
Default:	0001h
Access:	RO, R/W

The Bridge Configuration register is used to control the bridge functions specific to the R5C485 like an I/O addressing mode and Prefetchable memory transactions from CardBus to PCI bus. Each socket has its own Bridge Configuration register. Only GBRST# can initialize this register.

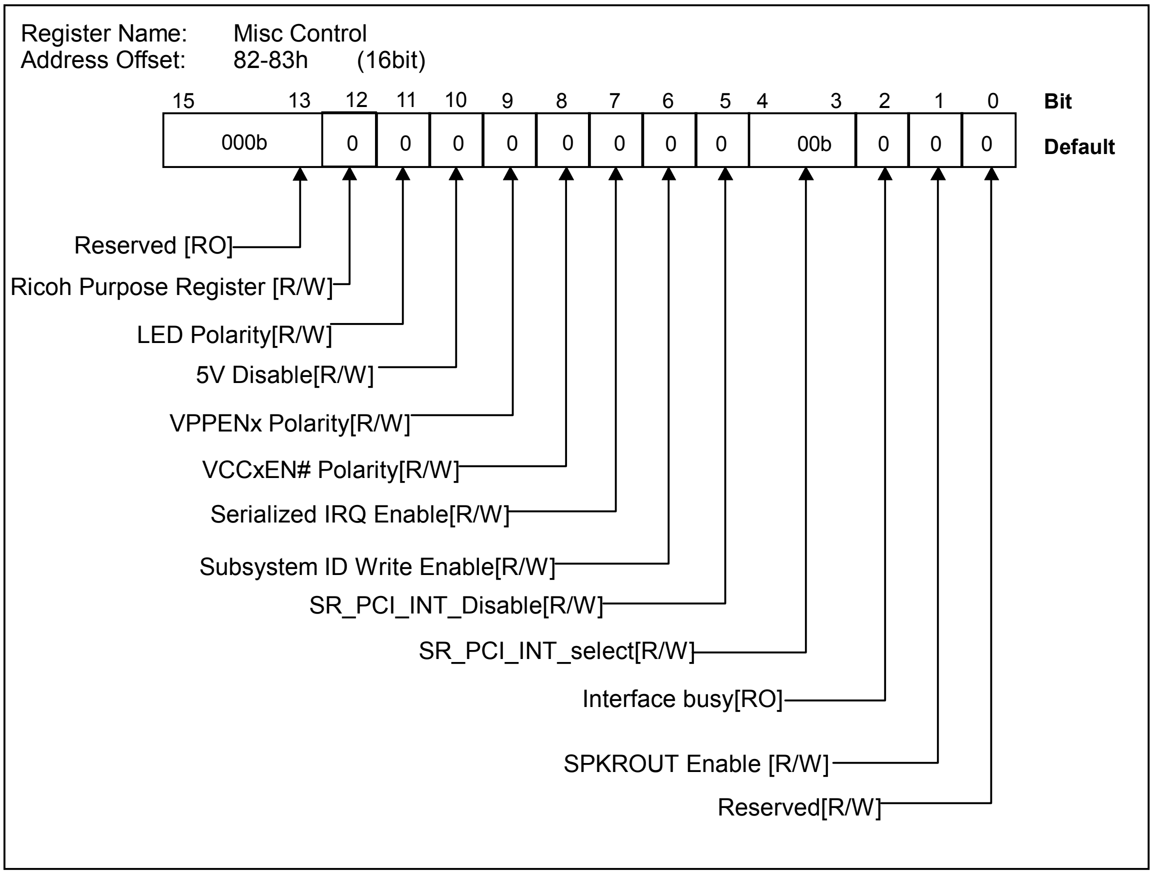

Register Name: Bridge Configuration
Address Offset: 80-81h (16bit)
15
10
9
8
7
2
1
0
Bit
000000b
0
0
000000b
0
1
Default
Reserved[RO]
I/O 1 Address Mode[R/W]
I/O 0 Address Mode[R/W]
Reserved[RO]
Reserved[RO]
Card to PCI Prefetch Enable[R/W]

Bit	Field Name	Description
15-10	Reserved	These bits are reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.
9	I/O 1Address Mode	This bit controls the address size of I/O window #1. When this bit is set to one, the I/O Base #1 Upper register and the I/O Limit #1 Upper register are enabled. When this bit is set to zero, the I/O Base #1 Upper register and the I/O Limit #1 Upper register are disabled, and the I/O transaction is forwarded only when the upper 16-bit address [31:16] is zero. The default after reset is zero.
8	I/O 0Address Mode	This bit controls the address size of I/O window #0. When this bit is set to one, the I/O Base #0 Upper register and the I/O Limit #0 Upper register are enabled. When this bit is set to zero, the I/O Base #0 Upper register and the I/O Limit #0 Upper register are disabled, and the I/O transaction is forwarded only when the upper 16-bit address [31:16] is zero. The default after reset is zero.
7-2	Reserved	These bits are reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.
1	Reserved	This bit is reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.
0	Card to PCI Prefetch Enable	When this bit is one, Read Prefetch is enabled from CardBus to PCI bus. The default after set is one.

5.4.28 Misc Control register

Register Name:	Misc Control
Address Offset:	82h-83h(16bit)
Default:	0000h
Access:	RO, R/W

The Misc Control register controls the power-down mode of the R5C485, the polarity of the card power enable signal, Serial IRQ and Subsystem ID write signals enable/disable. Only GBRST# can initialize this register.

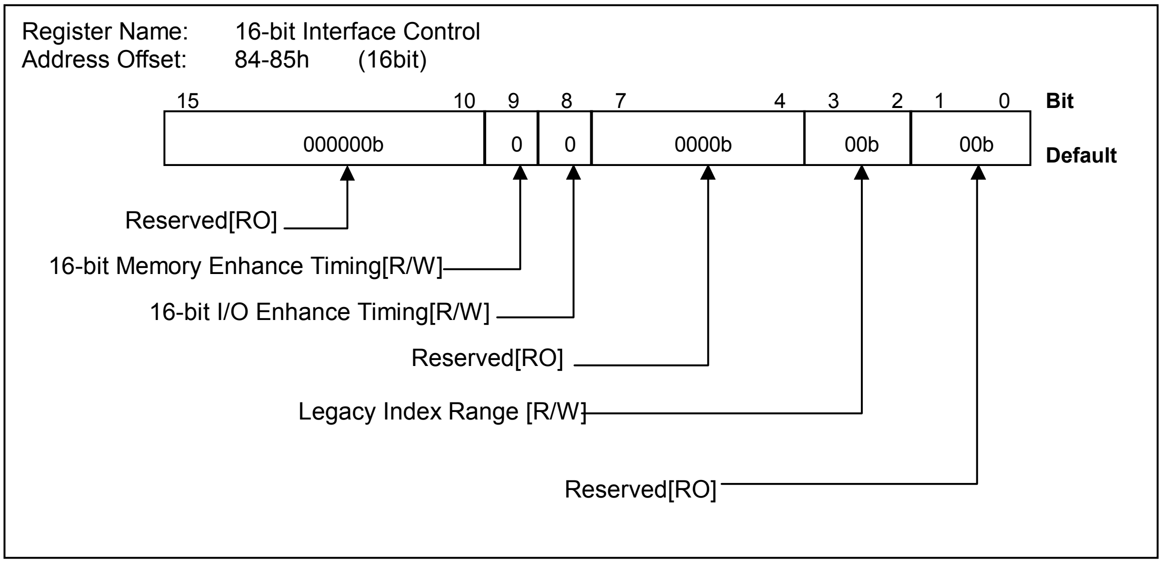

Register Name: Misc Control
Address Offset: 82-83h (16bit)
15 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Bit
000b 0 0 0 0 0 0 0 0 00b 0 0 0
Default
Reserved [RO]
Ricoh Purpose Register [R/W]
LED Polarity[R/W]
5V Disable[R/W]
VPPENx Polarity[R/W]
VCCxEN# Polarity[R/W]
Serialized IRQ Enable[R/W]
Subsystem ID Write Enable[R/W]
SR_PCI_INT_Disable[R/W]
SR_PCI_INT_select[R/W]
Interface busy[RO]
SPKROUT Enable [R/W]
Reserved[R/W]

Bit	Field Name	Description
15-13	Reserved	These bits are reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.
12	Ricoh Purpose Register	This bit is reserved for future use, and read/write. Don’t write any value excepting ‘0’ into this field. The default after reset is zero.
11	LED Polarity	This bit controls the polarity of LED signal. The default is zero and “low” active. When this bit is set to one, LED signal is “high” active.
10	5V Disable	In the card supplied 5V/3.3V, 5V is disabled when this bit is set.
9	VPPENx Polarity	This bit controls the polarity of VPPEN1 and VPPEN0 signals. When this bit is set to one, VPPEN1 and VPPEN0 are “low” active signals. When this bit is cleared, VPPEN1 and VPPEN0 are “high” active signals. The default after reset is zero.
8	VCCxEN# Polarity	This bit controls the polarity of VCC5EN# and VCC3EN# signals. When this bit is set to one, VCC5EN# and VCC3EN# are “high” active signals. When this bit is cleared, VCC5EN# and VCC3EN# are “low” active signals. The default after reset is zero.
7	SRIRQ Enable	When this bit is set, the Serial IRQ mode is enabled. IRQ9 is assigned as SIRQ# pin. The default after reset is zero.
6	Subsystem ID Write Enable	When this bit is set to one, Writing to Subsystem Vendor ID and Subsystem ID is enabled. The default after reset is zero.
5	SR_PCI_INT_Disable	When this bit is set to zero, The R5C485 can insert the frame of INTA#, INTB#, INTC#, and INTD#(PCI Interrupt signals) following IOCHK# frame. The default after reset is zero.
4-3	SR_PCI_INT_Select	These bits indicate which of PCI_INT# signals outputted from SRIRQ# is selected. 00b INTA#(Default) 01b INTB# 10b INTC# 11b INTD#
2	Interface Busy	This bit is read-only. When this bit is set to one, the card interface is busy. Returns zero when the internal buffers are empty. The default after reset is zero.
1	SPKROUT enable	When this bit is set to one, HWSPND# signal is reassigned as SPKROUT that is an output pin and either CAUDIO of CardBus card or SPKR# digital audio input data from 16bit I/O card is output. The default after reset is zero.
0	Reserved	This bit is reserved for future use. This field is read/write and returns zero when read. Writing to this field has no effect.

5.4.29 16-bit Interface Control register

Register Name:	16-bit Interface Control
Address Offset:	84h-85h(16bit)
Default:	0000h
Access:	RO, R/W

The 16-bit Interface Control register is used to set 16-bit interface timing and the PCIC compatible mode. Only GBRST# can initialize this register.

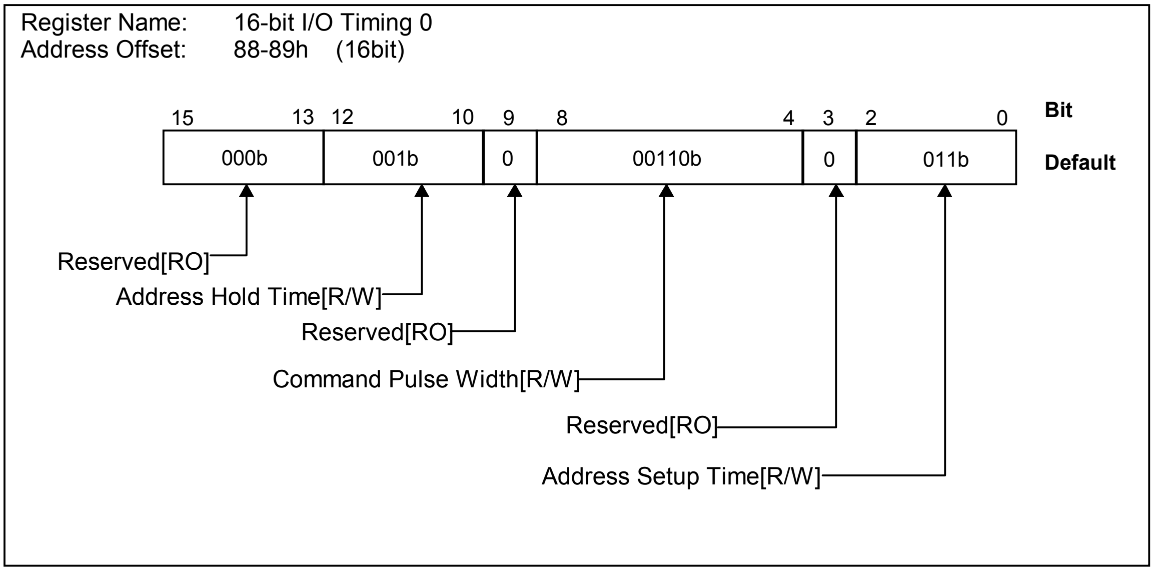

Register Name: 16-bit Interface Control
Address Offset: 84-85h (16bit)
15
10
9
8
7
4
3
2
1
0
Bit
000000b
0
0
0000b
00b
00b
Default
Reserved[RO]
16-bit Memory Enhance Timing[R/W]
16-bit I/O Enhance Timing[R/W]
Reserved[RO]
Legacy Index Range [R/W]
Reserved[RO]

Bit	Field Name	Description
15-10	Reserved	These bits are reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.
9	16-bit Memory Enhance Timing	When this bit is set to one, the 16-bit memory enhanced timing is enabled. 16-bit memory access timing is determined by 16-bit Memory Timing #0 register. When this bit is reset to zero, 16-bit memory access timing is reset to the default condition. The default after reset is zero.
8	16-bit I/O Enhance Timing	When this bit is set to one, the 16-bit I/O enhanced timing is enabled. 16-bit I/O access timing is determined by 16-bit I/O Timing #0 register. When this bit is reset to zero, 16-bit I/O timing is reset to the default condition. The default after reset is zero.
7-4	Reserved	These bits are reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.
3-2	Legacy Index Range	This bit indicates the index range that is accessed through PCIC compatible I/O port 3E0 or 3E2. Index range 00b 00h to 3Fh 01b 40h to 7Fh 10b 80h to BFh 11b C0h to FFh The default after reset is zero.
1-0	Reserved	These bits are reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.

5.4.30 16-bit I/O Timing 0 register

Register Name:	16-bit I/O Timing 0
Address Offset:	88h-89h(16bit)
Default:	0463h
Access:	RO, R/W

16-bit I/O access timing parameters are independently configured for each socket by programming this register. Only GBRST# can initialize this register.

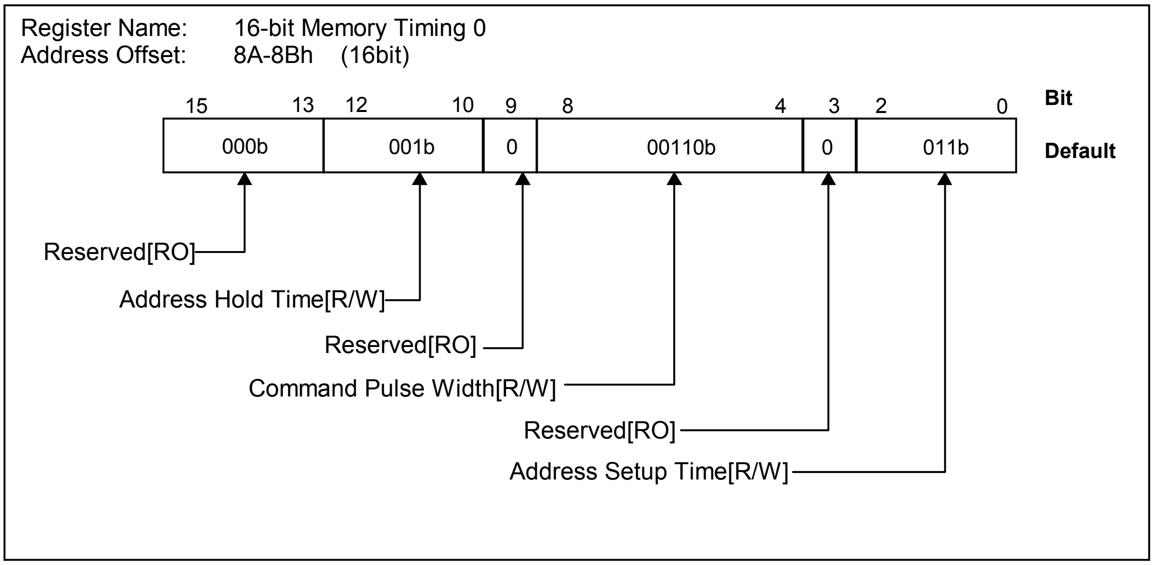

Register Name: 16-bit I/O Timing 0
Address Offset: 88-89h (16bit)
15
13
12
10
9
8
4
3
2
0
Bit
000b
001b
0
00110b
0
011b
Default
Reserved[RO]
Address Hold Time[R/W]
Reserved[RO]
Command Pulse Width[R/W]
Reserved[RO]
Address Setup Time[R/W]

Bit	Field Name	Description
15-13	Reserved	These bits are reserved for future use. This field is read-only and returns zeros when read. Writing to this field has no effect.
12-10	Address Hold Time	This field indicates the address hold time of 16-bit I/O cycle. The hold time can be set in a timer granularity of PCICLK. The default after reset is 001b.
9	Reserved	This bit is reserved for future use. This bit is read-only and returns zero when read. Writing to this bit has no effect.
8-4	Command Pulse Width	This field indicates the command pulse width of 16-bit I/O cycle for IORD# and IOWR#. The pulse width can be set in a timer granularity of PCICLK. The default after reset is 00110b.
3	Reserved	This bit is reserved for future use. This bit is read-only and returns zero when read. Writing to this bit has no effect.
2-0	Address Setup Time	This field indicates the address setup of 16-bit I/O cycle. The setup time can be set in a timer granularity of PCICLK. The default after reset is 011b.

5.4.31 16-bit Memory Timing 0 register

Register Name:	16-bit Memory Timing 0
Address offset:	8Ah-8Bh(16bit)
Default:	0463h
Access:	RO, R/W

16-bit Memory access timing parameters are independently configured for each socket by programming this register. Only GBRST# can initialize this register.

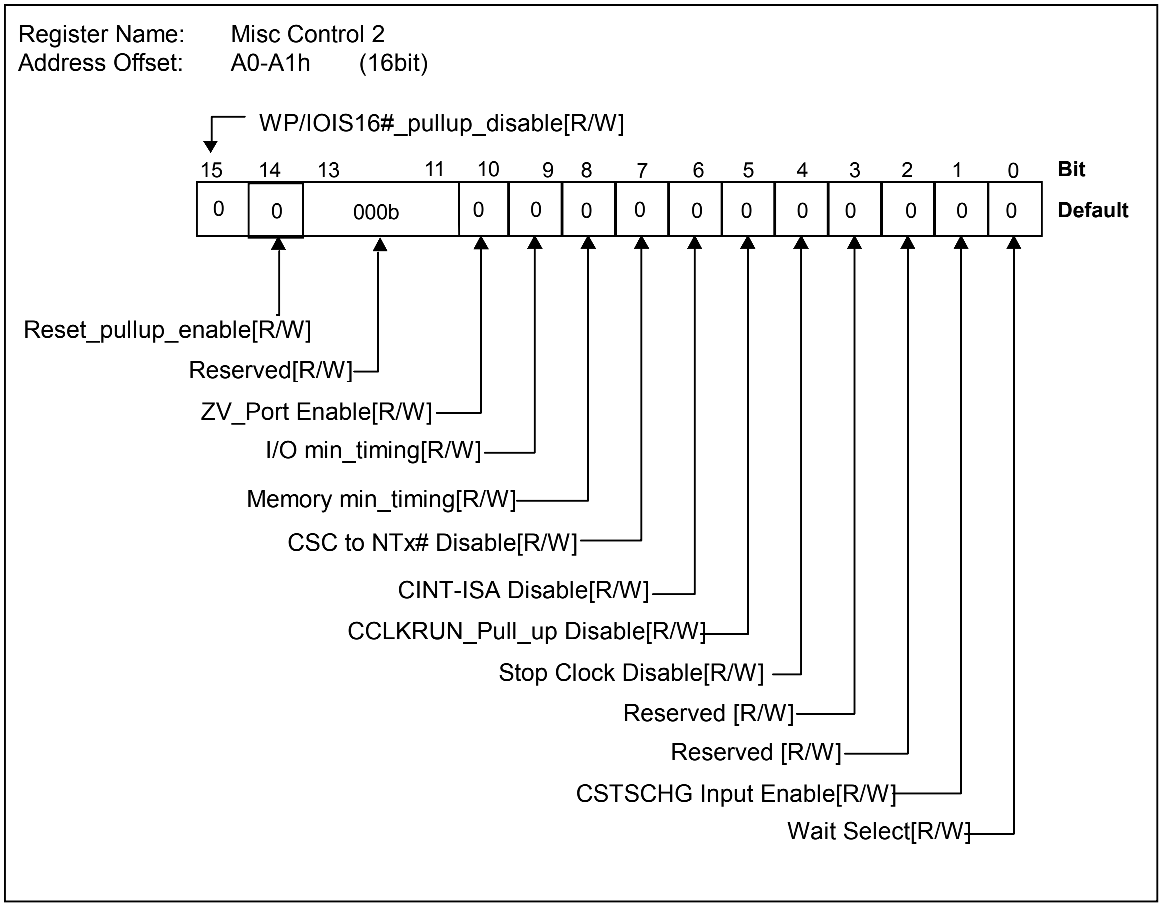

Register Name: 16-bit Memory Timing 0
Address Offset: 8A-8Bh (16bit)
15
13
12
10
9
8
4
3
2
0
Bit
000b
001b
0
00110b
0
011b
Default
Reserved[RO]
Address Hold Time[R/W]
Reserved[RO]
Command Pulse Width[R/W]
Reserved[RO]
Address Setup Time[R/W]

Bit	Field Name	Description
15-13	Reserved	These bits are reserved for future use. This field is read-only and returns zeros when read. Writing to this bit has no effect.
12-10	Address Hold Time	This field indicates the address hold time of 16-bit memory cycle. The hold time can be set in a timer granularity of PCICLK. The default after reset is 001b.
9	Reserved	This bit is reserved for future use. This bit is read-only and returns zero when read. Writing to this bit has no effect.
8-4	Command Pulse Width	This field indicates the command pulse width of 16-bit memory cycle for OE# and WE#. The pulse width can be set in a timer granularity of PCICLK. The default after reset is 00110b.
3	Reserved	This bit is reserved for future use. This bit is read-only and returns zero when read. Writing to this bit has no effect.
2-0	Address Setup Time	This field indicates the address setup time of 16-bit memory cycle. The setup time can be set in a timer granularity of PCICLK. The default after reset is 011b.

5.4.32 Misc Control 2 register

Register Name:	Misc Control 2
Address Offset:	A0h-A1h (16 bit)
Default:	0000h
Access:	R/W

The Misc Control 2 register indicates each kind of controls for the R5C485. Only GBRST# can initialize this register.

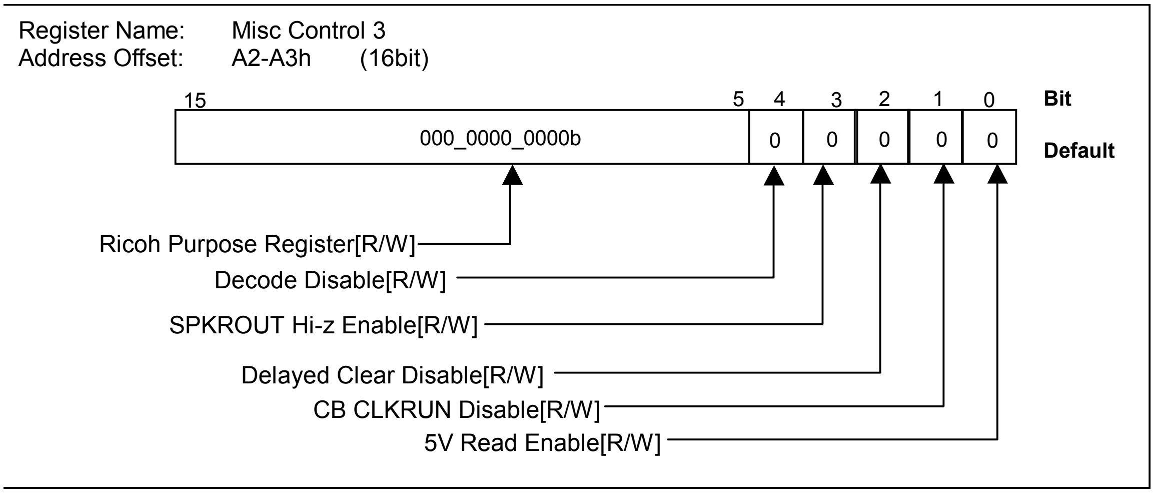

Register Name: Misc Control 2
Address Offset: A0-A1h (16bit)
WP/IOIS16#_pullup_disable[R/W]
15
14
13
11
10
9
8
7
6
5
4
3
2
1
0
Bit
0
0
000b
0
0
0
0
0
0
0
0
0
0
0
Default
Reset_pullup_enable[R/W]
Reserved[R/W]
ZV_Port Enable[R/W]
I/O min_timing[R/W]
Memory min_timing[R/W]
CSC to NTx# Disable[R/W]
CINT-ISA Disable[R/W]
CCLKRUN_Pull_up Disable[R/W]
Stop Clock Disable[R/W]
Reserved [R/W]
Reserved [R/W]
CSTSCHG Input Enable[R/W]
Wait Select[R/W]

Bit	Field Name	Description
15	WP/IOIS16#_pullup _disable	When this bit is set to one, an internal pull-up of the WP/IOIS16# signal on 16bit mode is disabled. The default after reset is zero. Therefore, inserting the 16bit card on default makes this signal pull-up.
14	Reset_pullup_enable	When this bit is set to one, an internal pull-up of the RESET signal is enabled. The default after reset is zero.
13-11	Reserved	These bits are reserved for future use. This field is read/write. The default after reset is zero.
10	ZV_Port Enable	When this bit is set to one, ZV Port is enabled as the Misc Control 1 (82Fh) in the EXCA register. (When either one is set, ZV Port isenabled.) The default after reset is zero.
9	I/O min_timing	When this bit is set to one, 16bit I/O Enhance Timing is enabled and Minimum timing is set compulsory. The default after reset is zero.
8	Memory min_timing	When this bit is set to one, 16bit Memory Enhance Timing is enabled and Minimum timing is set compulsory. The default after reset is zero.
7	CSC to INT# Disable	On the default, the 16bit status Change interrupt signal is output to INTA#. When this bit is set to one, it is output to the ISA interrupt signal only. The default after reset is zero.
6	CINT-ISA Disable	When this bit is set to one, CINT# is disabled to output to the ISA interrupt signal by the IREQ-ISA Enable bit of the Bridge Control register (3Eh). The default after reset is zero.
5	CCLKRUN_Pull-up Disable	When this bit is set to one, this pin must have an external pull-up. Because setting this bit to one disables an internal pull-up of the CCLKRUN pin on CardBus.
4	Stop Clock Disable	When this bit is set to one, the Stop Clock bit of the CardBus register is disabled. The default after reset is zero.
3-2	Reserved	This bit is reserved for future use. This field is read/write. The default after reset is zero.
1	CSTSCHG Input Enable	When this bit is set to one, CSTSCHG Input signal is enabled and WOL (Wake On LAN) is supported even if a VCC on the socket is off. When this bit is cleared, CSTSCHG Input signal is disabled. The default after reset is zero. But, when the card is removed, CSTSCHG Input signal is disabled even if this bit is set.
0	Wait Select	When this bit is set to one, the internal wait time of the device is extended for one clock. That is, when the WAIT# for the 16bit card is asserted, the width of command pulse is extended for one clock. The default after reset is zero.

5.4.33 Misc Control 3 register

Register Name:	Misc Control 3
Address Offset:	A2h-A3h (16 bit)
Default:	0000h
Access:	R/W

The Misc Control 3 register indicates each kind of controls for the R5C485 as the Misc Control 2. Only GBRST# can initialize this register.

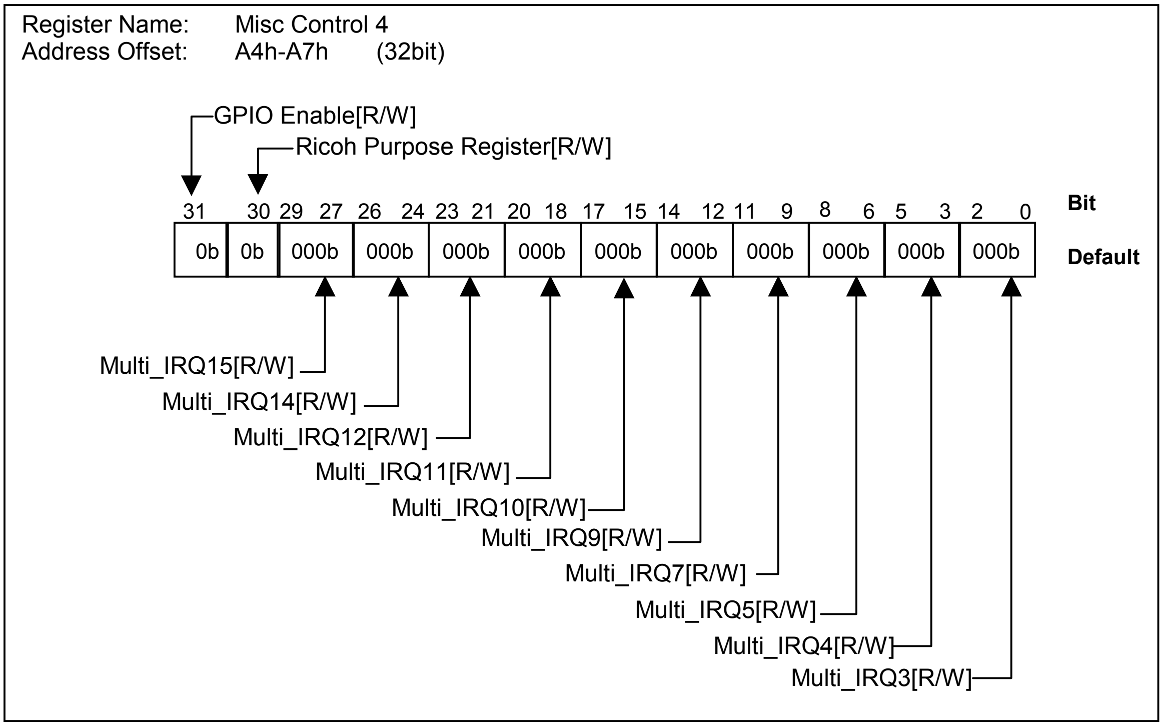

Register Name: Misc Control 3
Address Offset: A2-A3h (16bit)
15
5
4
3
2
1
0
Bit
000_0000_0000b
0
0
0
0
0
Default
Ricoh Purpose Register[R/W]
Decode Disable[R/W]
SPKROUT Hi-z Enable[R/W]
Delayed Clear Disable[R/W]
CB CLKRUN Disable[R/W]
5V Read Enable[R/W]

<table>
<tr><th>Bit</th><th>Field Name</th><th>Description</th></tr>
<tr><td>15-5</td><td>Ricoh Purpose Register</td><td>These bits are reserved for future use. This field is read/write. The default after reset is zero. Do not writing any value excepting “0”.</td></tr>
<tr><td>4</td><td>Decode Disable</td><td>When this bit is set to one, NotACard is enabled under the conditions of detecting the card. When this is cleared, as the 16bit card for 5V is detected. The default after reset is 0b.
<table>
<tr><td>CD2#</td><td>CD1#</td><td>VS2#</td><td>VS1#</td></tr>
<tr><td>ground</td><td>ground</td><td>ground</td><td>open</td></tr>
</table></td></tr>
<tr><td>3</td><td>SPKROUT Hi-z Enable</td><td>When this bit is set to one, SPKROUT output is forced to be Hi-z on HW_Suspend mode. But when this bit is cleared, it is not. The default after reset is 0b.</td></tr>
<tr><td>2</td><td>Delayed Clear Disable</td><td>The R5C485 repeats to retry on the Delayed transaction until the transaction for the CardBus Card is finished. On default, when the R5C485 recognizes an abnormality to repeat retrying for 2 msec, the R5C485 will stop the transaction. But, when this bit is set to one, the R5C485 will not stop the transaction, and repeat to retry until the transaction for CardBus card is finished. (This bit is usually used when WAIT# is long on the 16bit card is asserted.)</td></tr>
<tr><td>1</td><td>CB CLKRUN Disable</td><td>When this bit is set to one, Host’s CLKRUN request is refused on the CardBus card. The default after reset is 0b.</td></tr>
<tr><td>0</td><td>5V Read Enable</td><td>When the R5C485 is inserted a 3.3V/5V Card, as the 3V Card bit of the Socket Present State register (008h) is set to one, the 5V Card bit is not. But, both are enabled to set by setting this bit to one. When this bit is set to one, note that the 5V Card bit is set by inserting a 3V Card.</td></tr>
</table>

5.4.34 Misc Control 4 register

Register Name:	Misc Control 4
Address Offset:	A4h-A7h (32 bit)
Default:	0000_0000h
Access:	R/W

The Misc Control 4 register is used to define the IRQ3-15 pins. These pins are defined as the following functions. The default is IRQ3-15. Only GBRST# can initialize this register.


Register Name: Misc Control 4
Address Offset: A4h-A7h (32bit)
GPIO Enable[R/W]
Ricoh Purpose Register[R/W]
31
30 29 27
26 24
23 21
20 18
17 15
14 12
11 9
8 6
5 3
2 0
Bit
0b
0b
000b
000b
000b
000b
000b
000b
000b
000b
000b
000b
Default
Multi_IRQ15[R/W]
Multi_IRQ14[R/W]
Multi_IRQ12[R/W]
Multi_IRQ11[R/W]
Multi_IRQ10[R/W]
Multi_IRQ9[R/W]
Multi_IRQ7[R/W]
Multi_IRQ5[R/W]
Multi_IRQ4[R/W]
Multi_IRQ3[R/W]

Bit	Field Name	Description
31	GPIO Enable	When this bit is set to zero, GPIO outputs assigned to IRQ [3,4,5,7] pins become Hi-Z and GPIO inputs are disabled. When it is set to one, setting of the General Purpose I/O 1 register (the PCI Config.AAh) or the General Purpose I/O register (83Ah) is done.
30	Ricoh Purpose Register	This bit is reserved for future use. This bit is read/wirte. The default after reset is zero. Do not write any value excepting “0” into this bit.

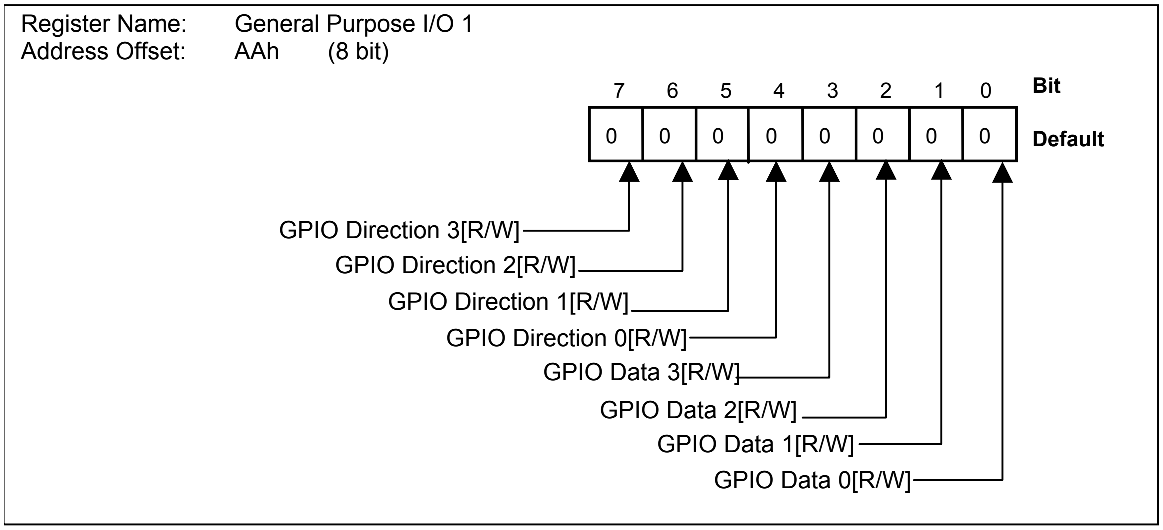
Bit	Field Name	Description
29-27	Multi_IRQ15	This field defines IRQ15 as follows. The default after reset is zero. 000b - IRQ15/ZVEN# (default)/(default on S-IRQ mode) 001b - SPKROUT 010b- D3STATE 011b - LED# 100b - ZVEN# 101b - Hi-z 110b - SPKROUT 111b - IRQ5
26-24	Multi_IRQ14	This field defines IRQ14 as follows. The default after reset is zero. 000b - IRQ14 (default) 001b - SPKROUT 010b - LED# 011b - ZVEN# 100b - IRQ4 101b - Hi-z 110b - SPKROUT 111b - D3STATE Notes: This field cannot be multiple if using Serial ROM.
23-21	Multi_IRQ12	This field defines IRQ12 as follows. The default after reset is zero. 000b - IRQ12 (LEDOUT) Setting Programmable bit (16bitReg.81Fh-bit1) (default) 001b - SPKROUT 010b - LED# 011b - ZVEN# 100b - IRQ3 101b - Hi-z 110b - SPKROUT 111b - D3STATE Notes: This field cannot be multiple if using Serial ROM.
20-18	Multi_IRQ11	This field defines IRQ11 as follows. The default after reset is zero. 000b - IRQ11 (default) 001b - SPKROUT 010b - D3STATE 011b - LED# 100b - ZVEN# 101b - Hi-z 110b - SPKROUT 111b - IRQ12 (LEDOUT) Setting Programmable bit (16bitReg.81Fh-bit1)
17-15	Multi_IRQ10	This field defines IRQ10 as follows. The default after reset is zero. 000b - IRQ10/LED# (default)/(default on S-IRQ mode) 001b - SPKROUT 010b - LED# 011b - ZVEN# 100b - IRQ12 (LEDOUT) Setting Programmable bit (16bitReg.81Fh-bit1) 101b - IRQ15 110b - SPKROUT 111b - Hi-z

Bit	Field Name	Description
14-12	Multi_IRQ9	This field defines IRQ9 as follows. On S-IRQ mode, this field cannot be multiple (fix on SRIRQ#). The default after reset is zero. 000b - IRQ9/SRIRQ# (default)/(default on S-IRQ mode) 001b - SPKROUT 010b - IRQ12 (LEDOUT) Setting Programmable bit (16bitReg.81Fh-bit1) 011b - ZVEN# 100b - LED# 101b - IRQ15 110b - SPKROUT 111b - Hi-z
11-9	Multi_IRQ7	This field defines IRQ7 as follows. The default after reset is zero. 000b - IRQ7/GPIO3 (default)/(default on S-IRQ mode) 001b - SPKROUT 010b - IRQ14 011b - LED# 100b - ZVEN# 101b - Hi-z 110b - SPKROUT 111b - GPIO3
8-6	Multi_IRQ5	This field defines IRQ5 as follows. The default after reset is zero. 000b - IRQ5/GPIO2 (default)/(default on S-IRQ mode) 001b - SPKROUT 010b - IRQ12 (LEDOUT) Setting Programmable bit (16bitReg.81Fh-bit1) 011b - LED# 100b - ZVEN# 101b - Hi-z 110b - SPKROUT 111b - GPIO2
5-3	Multi_IRQ4	This field defines IRQ4 as follows. The default after reset is zero. 000b - IRQ4/GPIO1 (default)/(default on S-IRQ mode) 001b - SPKROUT 010b - D3STATE 011b - LED# 100b - ZVEN# 101b - Hi-z 110b - SPKROUT 111b - GPIO1
2-0	Multi_IRQ3	This field defines IRQ3 as follows. The default after reset is zero. 000b - IRQ3/GPIO0 (default)/(default on S-IRQ mode) 001b - SPKROUT 010b - IRQ12 (LEDOUT) Setting Programmable bit (16bitReg.81Fh-bit1) 011b - LED# 100b- ZVEN# 101b - Hi-z 110b - SPKROUT 111b - GPIO0

5.4.35 General Purpose I/O 1 register

Register Name: General Purpose I/O 1
Address Offset: AAh (8bit)
Default: 00h
Access: R/W

The R5C485 assigns IRQ [3,4,5,7] pins to GPIO (General Purpose I/O) pins when Serialized IRQ mode is selected and GPIO Enable bit in the Misc Control 4 register is set. User can be free to use these I/O pins. When GPIO Enable bit is set to one, setting of GPIO is Input mode (default). And Bit [3:0] indicates the state of mode. In Output mode, GPIO [3:0] output the contents written in each bit. This register linking to the General Purpose I/O register reflects the General Purpose I/O register (83Ah). On the other hand, the General Purpose I/O register also reflects this register.

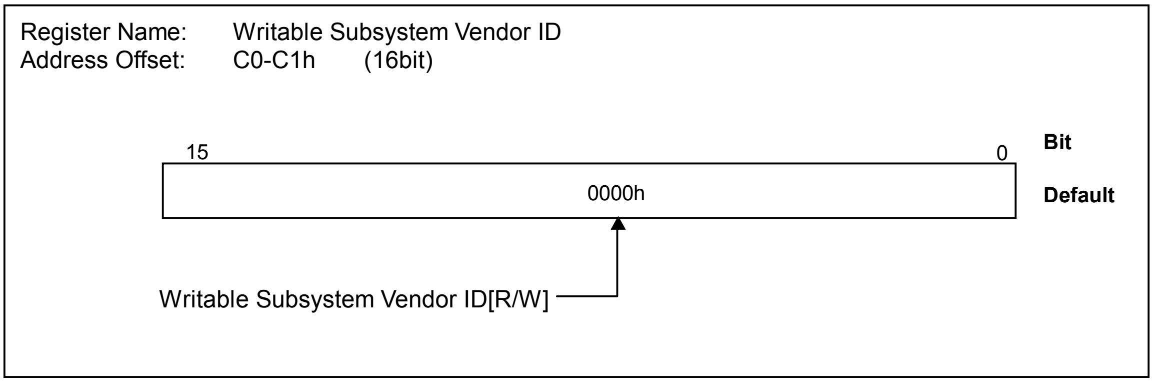

Register Name: General Purpose I/O 1
Address Offset: AAh (8 bit)
7 6 5 4 3 2 1 0
Bit
0 0 0 0 0 0 0 0
Default
GPIO Direction 3[R/W]
GPIO Direction 2[R/W]
GPIO Direction 1[R/W]
GPIO Direction 0[R/W]
GPIO Data 3[R/W]
GPIO Data 2[R/W]
GPIO Data 1[R/W]
GPIO Data 0[R/W]

Bit	Field Name	Description
7	GPIO Direction 3	This bit is an I/O changeover signal for GPIO Data 3. GPIO Data 3 is input when this bit is set to 0, and it is output when this bit is set to 1. The default after reset is 0b.
6	GPIO Direction 2	This bit is an I/O changeover signal for GPIO Data 2. GPIO Data 2 is input when this bit is set to 0, and it is output when this bit is set to 1. The default after reset is 0b.
5	GPIO Direction 1	This bit is an I/O changeover signal for GPIO Data 1. GPIO Data 1 is input when this bit is set to 0, and it is output when this bit is set to 1. The default after reset is 0b.
4	GPIO Direction 0	This bit is an I/O changeover signal for GPIO Data 0. GPIO Data 0 is input when this bit is set to 0, and it is output when this bit is set to 1. The default after reset is 0b.
3	GPIO Data 3	General Purpose I/O bit 3. The default is input.
2	GPIO Data 2	General Purpose I/O bit 2. The default is input.
1	GPIO Data 1	General Purpose I/O bit 1. The default is input.
0	GPIO Data 0	General Purpose I/O bit 0. The default is input.

5.4.36 Writable Subsystem Vendor ID register

Register Name:	Writable Subsystem Vendor ID
Address Offset:	C0h-C1h (16bit)
Default:	0000h
Access:	R/W

Writable Subsystem Vendor ID register operates as same as 40h(Subsystem Vendor ID register). The value written in this register can read through 40h as Subsystem Vendor ID. Only GBRST# can initialize this register.

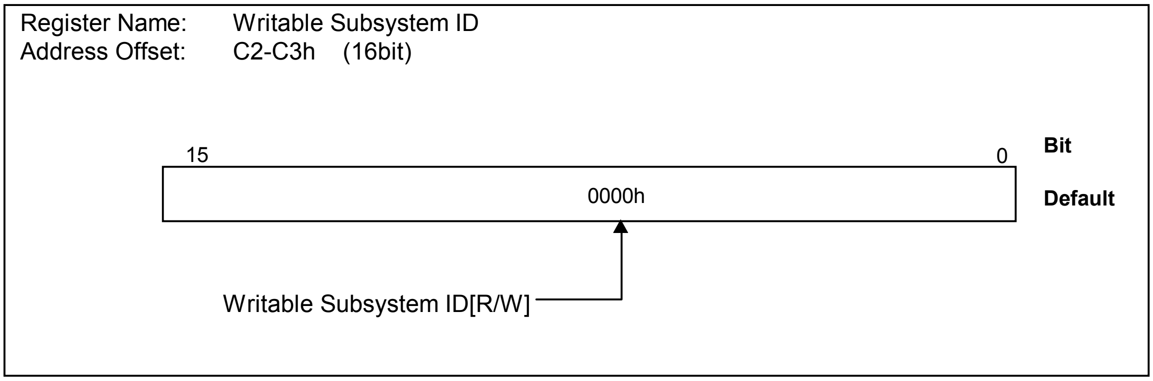

Register Name: Writable Subsystem Vendor ID
Address Offset: C0-C1h (16bit)
15
0
Bit
0000h
Default
Writable Subsystem Vendor ID[R/W]

Bit	Field Name	Description
15-0	Writable Subsystem Vendor ID	Writable Subsystem Vendor ID register operates as same as 40h (Subsystem Vendor ID register). The value written in this register can read through 40h as Subsystem Vendor ID. The default after reset is 0000h.

5.4.37 Writable Subsystem ID register

Register Name: Writable Subsystem ID
Address Offset: C2h-C3h (16bit)
Default: 0000h
Access: R/W

Writable Subsystem ID register operates as same as 42h(Subsystem ID register). The value written in this register can read through 42h as Subsystem ID. Only GBRST# can initialize this register.


Register Name: Writable Subsystem ID
Address Offset: C2-C3h (16bit)
15
0
Bit
0000h
Default
Writable Subsystem ID[R/W]

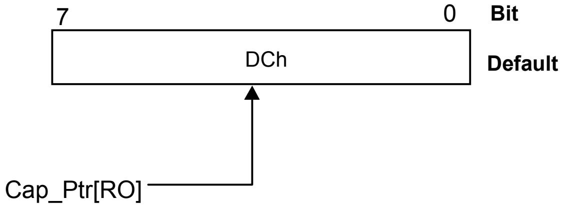
Bit	Field Name	Description
15-0	Writable Subsystem ID	Writable Subsystem ID register operates as same as 42h(Subsystem ID register). The value written in this register can read through 42h as Subsystem ID. The default after reset is 0000h.

5.4.38 Capabilities Pointer register

Register Name:	Capabilities Pointer
Address Offset:	14h (8 bit)
Default:	DCh
Access:	RO

The Capabilities Pointer register is read-only and provides an offset into the function's PCI Configuration Space for the location of the first item in the New Capabilities List. The R5C485 supports the PCI Power Management. This register is assigned a value of DCh for the PCI Power Management.

Register Name:	Capabilities Pointer register
Address Offset:	14h (8bit)



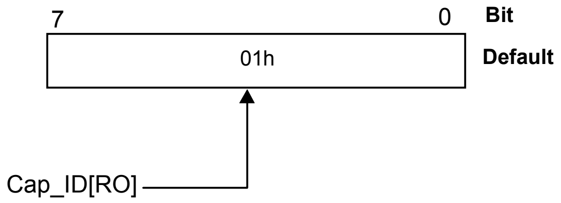
Bit	Field Name	Description
7-0	Capabilities Pointer	This field provides an offset into the function's PCI Configuration Space for the location of the first item in the New Capabilities Linked List. The R5C485 supports the PCI Power Management as a new function. This field is assigned a value of DCh for the PCI Power Management.

5.4.38.1 Capabilities Identifier register

Register Name: Capabilities Identifier
Address Offset: DCh (8 bit)
Default: 01h
Access: RO

The Capabilities Identifier register is read-only and indicates only one item in the linked list is the register defined for the PCI Power Management. This register is assigned the ID of 01h.

Register Name: Capabilities Identifier register
Address Offset: DCh (8bit)



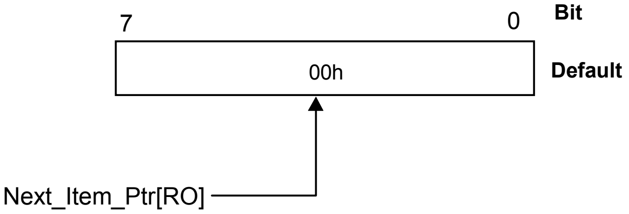
Bit	Field Name	Description
7-0	Capabilities Identifier	This field indicates the R5C485 support the PCI Power Management as a new function. This field is read-only and assigned the ID of 01h.

5.4.38.2 Next Item Pointer register

Register Name:	Next Item Pointer
Address Offset:	DDh (8 bit)
Default:	00h
Access:	RO

The Next Item Pointer register is read-only and indicates the location of the next item in the function's capability list. The R5C485 doesn't support items in the list except the PCI Power Management. So, this field is assigned a value of 00h.

Register Name: Next Item Pointer register
Address Offset: DDh (8bit)

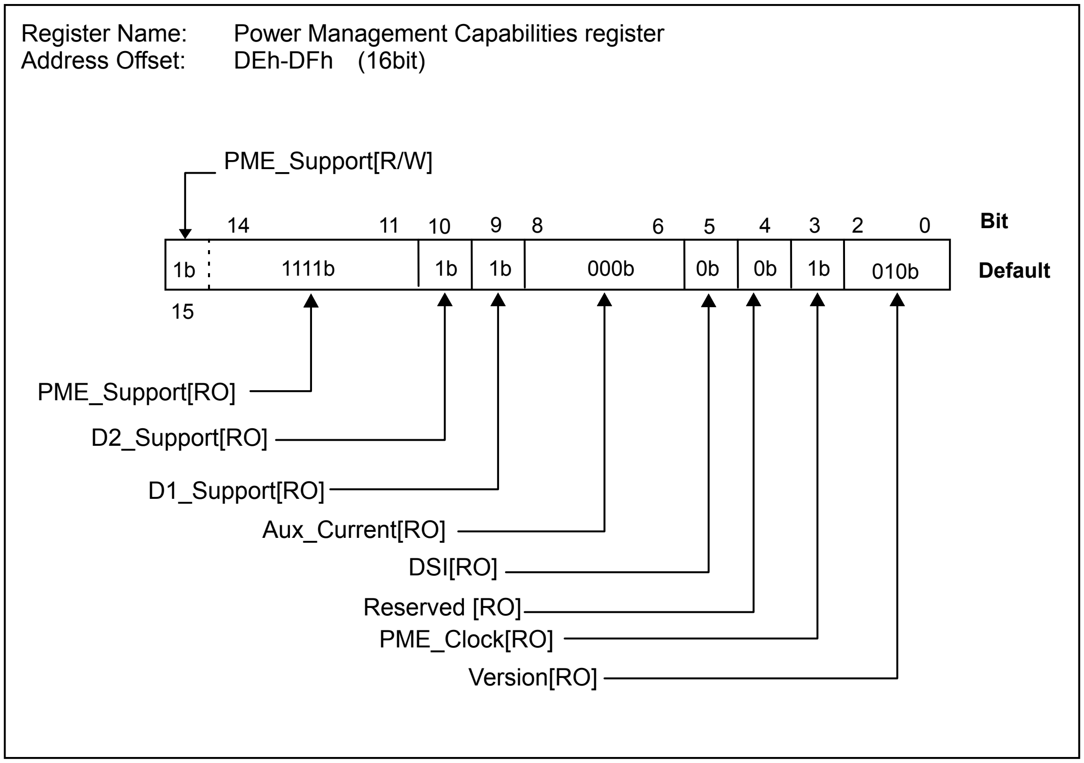


Bit	Field Name	Description
7-0	Next Item Pointer	This field indicates the location of the next item in the function's capability list. The R5C485 does not support items in the list except the PC Power Management. This field is read-only and assigned a value of 00h.

5.4.38.3 Power Management Capabilities register

Register Name:	Power Management Capabilities
Address Offset:	DEh-DFh (16 bit)
Default:	FE0Ah
Access:	RO, R/W

The Power Management Capabilities register is read-only and provides information on the capabilities of the function related to the PCI Power Management.

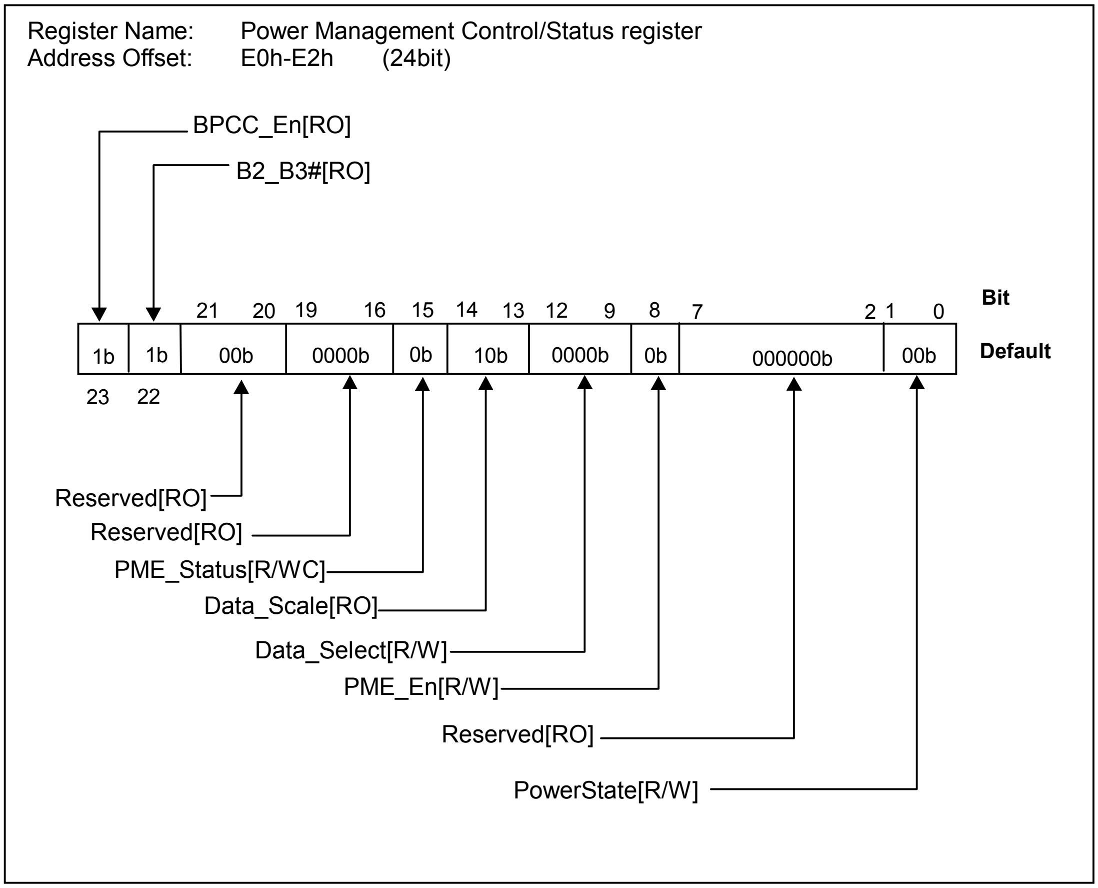

Register Name: Power Management Capabilities register
Address Offset: DEh-DFh (16bit)
PME_Support[R/W]
14
11
10
9
8
6
5
4
3
2
0
Bit
1b
1111b
1b
1b
000b
0b
0b
1b
010b
Default
15
PME_Support[RO]
D2_Support[RO]
D1_Support[RO]
Aux_Current[RO]
DSI[RO]
Reserved [RO]
PME_Clock[RO]
Version[RO]

Bit	Field Name	Description
15 14-11	PME_Support	This 4-bit field indicates the power states that the device supports asserting PME#. A value of 0 for any bit indicates that the function is not capable of asserting the PME# signal from that power state. XXX1b - PME# can be asserted from **D0** (bit 11) XX1Xb - PME# can be asserted from **D1** (bit 12) X1XXb - PME# can be asserted from **D2** (bit 13) 1XXXb - PME# can be asserted from **D3**hot (bit 14) Bit 15 is set to one if PME# can be asserted by the supply of auxiliary power, even if the PCI Vcc is turned off. If the auxiliary power is not supported, this bit must be set to zero because PME# is not asserted. The PME# signal indicates Wakeup events that include a "Ring Indication" from a Modem or the receipt of special packet by a Network card. When once PME# is asserted, it is kept at the state until Status bit (bit 15) is cleared or Enable bit (bit 8) is reset in the Power Management Control/Status register.
10	D2_Support	Returns one, because the R5C485 supports the D2 Power Management State.
9	D1_Support	Returns one, because the R5C485 supports the D1 Power Management State.
8-6	Aux_Current	This 3-bit field indicates the 3.3Vaux auxiliary current requirements for the PCI function. Return zeros on read.
5	DSI	This Device Specific Initialization bit is set to one when a device specific device driver is required to reinitialize a device after it leaves the D3 state. Returns zero, as it is not necessary to reinitialize in the R5C485.
4	Reserved	Reserved. Returns zero.
3	PME clock	When this bit is a "1" it indicates that the function relies on the presence of the PCI clock for PME# operation. When this bit is a "0" it indicates that no PCI clock is required for the function to generate PME#. This bit returns one because the R5C485 needs PCI clock to generate PME# when the power management event is caused by Card detect change, Ready/Busy change or Battery Warning. The R5C485 can generate PME# without PCI clock if PME is caused by Card status change.
2-0	Version	The R5C485 has 4 bytes of general purpose Power Management registers implemented as described in PCI Bus Power Management specification Rev1.1. These bits usually return 010b.

5.4.38.4 Power Management Control/Status register

Register Name:	Power Management Control/Status
Address Offset:	E0h-E2h (24 bit)
Default:	C04000h
Access:	RO, R/W, WC

The Power Management Control/Status register is used to control the current power state of the PCI function and inform the status information. The contents of this register are not affected by the internally generated reset caused by the transition from D3 to D0.


Register Name: Power Management Control/Status register
Address Offset: E0h-E2h (24bit)
BPCC_En[RO]
B2_B3#[RO]
Bit
21 20 19 16 15 14 13 12 9 8 7 2 1 0
1b 1b 00b 0000b 0b 10b 0000b 0b 000000b 00b
Default
23 22
Reserved[RO]
Reserved[RO]
PME_Status[R/WC]
Data_Scale[RO]
Data_Select[R/W]
PME_En[R/W]
Reserved[RO]
PowerState[R/W]

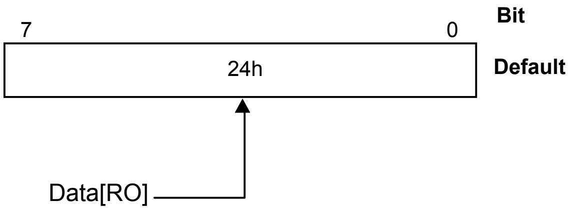
Bit	Field Name	Description
23	BPCC_En	This is Bus Power Clock Control Enable bit. Returns one as the bus power and clock control mechanism in the CardBus follows the power managing state of the R5C485.
22	B2_B3#	The state of this bit determines the action that is to occur as a direct result of programming the function to D3hot. A “1” indicates that when the bridge function is programmed to D3hot, its secondary bus’s PCI clock will be stopped (B2). A “0” indicates that when the bridge function is programmed to D3hot, its secondary bus will have its power removed (B3). Returns one, as the CardBus clock will be stopped when the R5C485 function is programmed to D3hot.
21-16	Reserved	Reserved. Return zeros when read.
15	PME_Status	This bit is set when the function normally asserts the PME# signal independent of the state of the PME_En bit (bit 8). Writing a one to this bit clears it and causes the function to stop asserting a PME# (if enabled). Writing a zero has no effect. The default after reset is zero.
14-13	Data_Scale	This 2-bits read-only field indicates the scaling factor to be used when interpreting the value of the Data register. Returns 10b as the R5C485 offers the information of power consumed in a 10mW step.
12-9	Data_Select	This 4-bits field is used to select which data is reported through the Data register and Data_Scale field. The default after reset is zero. 0000b D0 power consumed 0001b D1 power consumed 0010b D2 power consumed 0011b D3 power consumed 0100b D0 power dissipated 0101b D1 power dissipated 0110b D2 power dissipated 0111b D3 power dissipated 1xxxb Reserved
8	PME_En	When this bit is set, the function is enabled to assert PME#. When this bit is cleared, assertion of PME# is disabled. The default after reset is zero.
7-2	Reserved	Reserved. Return zeros when read.
1-0	PowerState	This field is used to set the function into a new power state. The definition of the field values is: 00b D0 01b D1 10b D2 11b D3 The default after reset is zeros.

5.4.38.5 Data Register

Register Name:	Data
Address Offset:	E3h (8 bit)
Default:	24h
Access:	RO

The Date register is read-only and provides a maximum value of the power consumed for each function from the PCI device by using with Data_Select bit fields and Data_Scale bit field.

Register Name: Data register
Address Offset: E3h (8bit)



Bit	Field Name	Description
7-0	Data	This read-only bit field provides the maximum value of the power consumed by the R5C485 for each function from the PCI device. The maximum value of the power consumed is 10mW times the value of Data_Scale bit field. The R5C485 returns the following value. D0 power state: 0010 0100b (360mW) D1 power state: 0010 0000b (320mW) D2 power state: 0000 0001b (10mW) D3 power state: 0000 0001b (10mW)

6 CARDBUS(PC CARD-32) SOCKET STATUS CONTROL REGISTERS

6.1 Overview

CardBus Socket Status/Control registers manage changed events, remote wakeup events, PC Card insertion/removal, and status information about the PC Card in the socket. These registers are used for PC Card-32 as well as PC Card-16.

6.2 Register Space mapping

PC Card Control Register Base Address register points to the 4Kbyte memory mapped I/O space that contains both the PC Card-32 and PC Card-16 Status and Control registers. Socket Status/Control Registers for PC Card-32 are placed in the bottom 2KByte of the 4KByte and start at offset 000h. The registers for PC Card-16 are placed in the upper 2KByte and start at offset 800h.

6.3 Register Configuration

Each socket has CardBus Socket Status/Control registers that consist of five DWORD registers. One set of registers is described in the following sections, with the address offset for each socket. Address offset [014h-7FCh] are assigned to the reserved registers. The reserved registers return 00000000h when read. Writing to the reserved registers has no effect.

Register Space Name: CardBus Socket Status / Control Register Space

31 24 23 16 15 8 7 0	**Bit**
Socket Event	000h
Socket Mask	004h
Socket Present State	008h
Socket Event Force	00Ch
Socket Control	010h
Reserved	014h ~ 7FCh

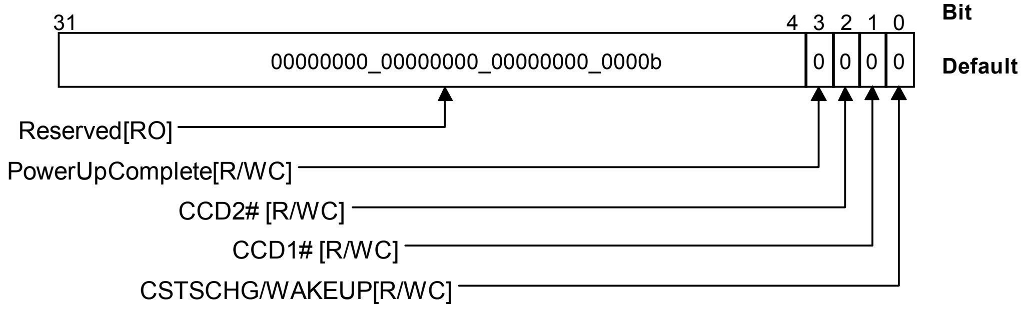
6.4 Register Description

CardBus Socket Status/Control registers manage status changed events, remote wakeup events, PC Card insertion/removal, and status information about the PC Card in the socket. These registers are used for PC Card-32 as well as PC Card-16.

6.4.1 Socket Event register

The Socket Event register indicates a change in socket status has occurred. These bits do not indicate what the change is, only that one has occurred. Software must read the Socket Present State register for current status. Writing a one to bit corresponding to each bits can clear each bit in this register. These bits can be set to a one by software through writing a one to the corresponding bit in the Socket Event Force register. All bits in this register are cleared by PCIRST#. They may be immediately set again, if when coming out of CRST# the bridge finds the status unchanged (i.e., CSTSCHG reasserted or Card Detects is still true). Software needs to clear this register before enabling interrupts. If it is not cleared, when interrupts are enabled an interrupt will be generated based on any bit set but not masked.

Register Name: Socket Event
Address Offset: 000-003h (32bit)

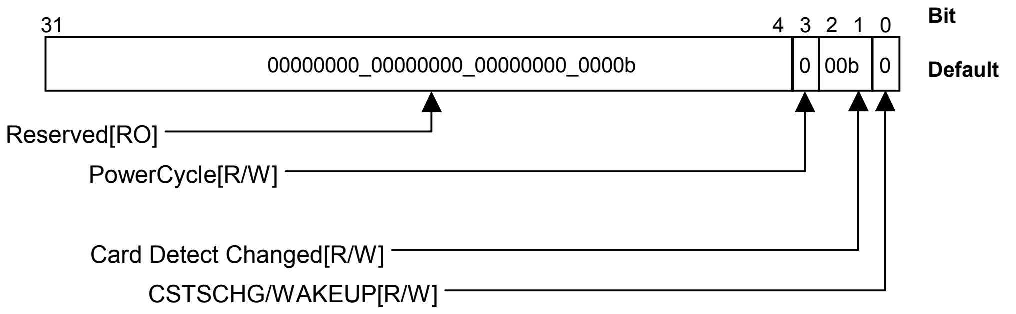


Bit	Field Name	Description
31-4	Reserved	These bits are reserved for future use. This field is read-only and returns zeros. Writing to this field has no effect.
3	PowerUpComplete	This bit is set when the R5C485 detected to complete powering up the PC Card-32 socket. The Socket Present State register should be read to determine whether or not the voltage requested was actually applied. Writing a one clears this bit. The default after reset is zero. This bit has no meaning when the 16-bit card is installed.
2	CCD2#	This bit is set whenever the CCD2# field in the Present State register changes state. Writing a one clears this bit. The default after reset is zero.
1	CCD1#	This bit is set whenever the CCD1# field in the Present State register changes state. Writing a one clears this bit. The default after reset is zero.
0	CSTSCHG/WAKEUP	This bit is set whenever the CSTSCHG/WAKEUP# was asserted, and indicates only the assertion event. However, this bit isn't directly reflected in a status change of the CSTSCHG/WAKEUP# in the Socket Present State register. And also, it isn't directly reflected in a status of the CSTSCHG bit from the card. This bit needs to be controlled by Software. Writing a one clears this bit. The default after reset is zero. This bit is meaningless when the 16-bit card is installed. If STSCHG# interrupt signal from the 16-bit card was occurred, this bit will be controlled by the 16-bit Card Status/Control register.

6.4.2 Socket Mask register

The Socket Mask register allows software to control the CardBus card events that generate a status change interrupt. If the Card Detect Changed bit is enabled at the time a card is removed, an interrupt is generated. After that, this bit is cleared automatically. This is to prevent spurious interrupts while cards are removed. If it is desired to have the bridge generate an interrupt at the time a new card is inserted, it is necessary that this bit be set again by software. This register is cleared by PCIRST#. The default after reset is zero.

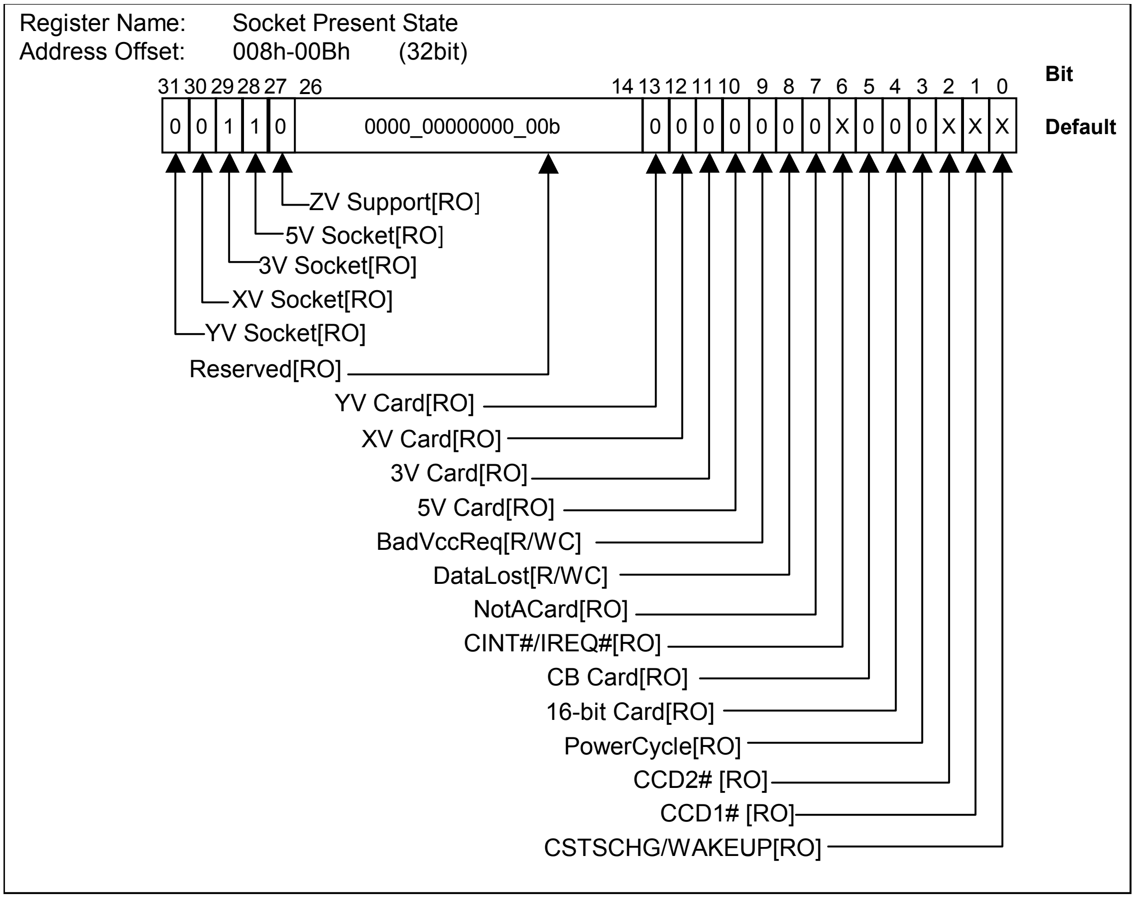
Register Name: Socket Mask
Address Offset: 004-007h (32bit)



Bit	Field Name	Description
31-4	Reserved	These bits are reserved for future use. This field is read-only and returns zeros. Writing to this field has no effect.
3	PowerCycle	This bit is masked a status changed interrupt caused by the event that indicates the end of power up process. When cleared (0), the status changed event signaling the power up process has completed is not generated, although the PowerCycle field in the Socket Event register is set. When this bit is set to one, an interrupt is generated after 256 cycles since a socket was finished powering up. The default after reset is zero.
2-1	Card Detect Changed	This field masks the CCD1# and CCD2# fields in the Socket Event register so that insertion and removal events will not cause a status changed interrupt to occur. The meaning of the bit is: 00b Mask the CCD1# and CCD2# fields in the Socket Event register. Card insertion/removal events will not cause a status change interrupt. 01b Undefined 10b Undefined 11b Unmask the CCD1# and CCD2# fields in the Socket Event register. Card insertion/removal events will cause a status change interrupt. The CCD1# and CCD2# fields in the Socket Event register are set in spite of setting of this field. The default after reset is zero.
0	CSTSCHG/WAKEUP	This bit masks a status changed interrupt of the CSTSCHG/WAKEUP#. When cleared (0), the assertion of CSTSCHG/WAKEUP# by the card is not cause a status changed interrupt to occur, although the CSTSCHG/WAKEUP field in the Socket Event register is set. This bit is set by writing a one, and is cleared when the socket PC card is removed, and also when the R5C485 is reset. This bit has no meaning when the 16-bit card is inserted.

6.4.3 Socket Present State register

The Socket Present State register reflects the current state of the socket. Some of the bits in this register are reflections of interface signals while others are flags set to indicate conditions associated with a status changed event. This register may be written by using the Force Event register.


Register Name: Socket Present State
Address Offset: 008h-00Bh (32bit)
Bit
31 30 29 28 27 26
14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0 0 1 1 0
0000_00000000_00b
0 0 0 0 0 0 0 X 0 0 0 X X X
Default
ZV Support[RO]
5V Socket[RO]
3V Socket[RO]
XV Socket[RO]
YV Socket[RO]
Reserved[RO]
YV Card[RO]
XV Card[RO]
3V Card[RO]
5V Card[RO]
BadVccReq[R/WC]
DataLost[R/WC]
NotACard[RO]
CINT#/IREQ#[RO]
CB Card[RO]
16-bit Card[RO]
PowerCycle[RO]
CCD2# [RO]
CCD1# [RO]
CSTSCHG/WAKEUP[RO]

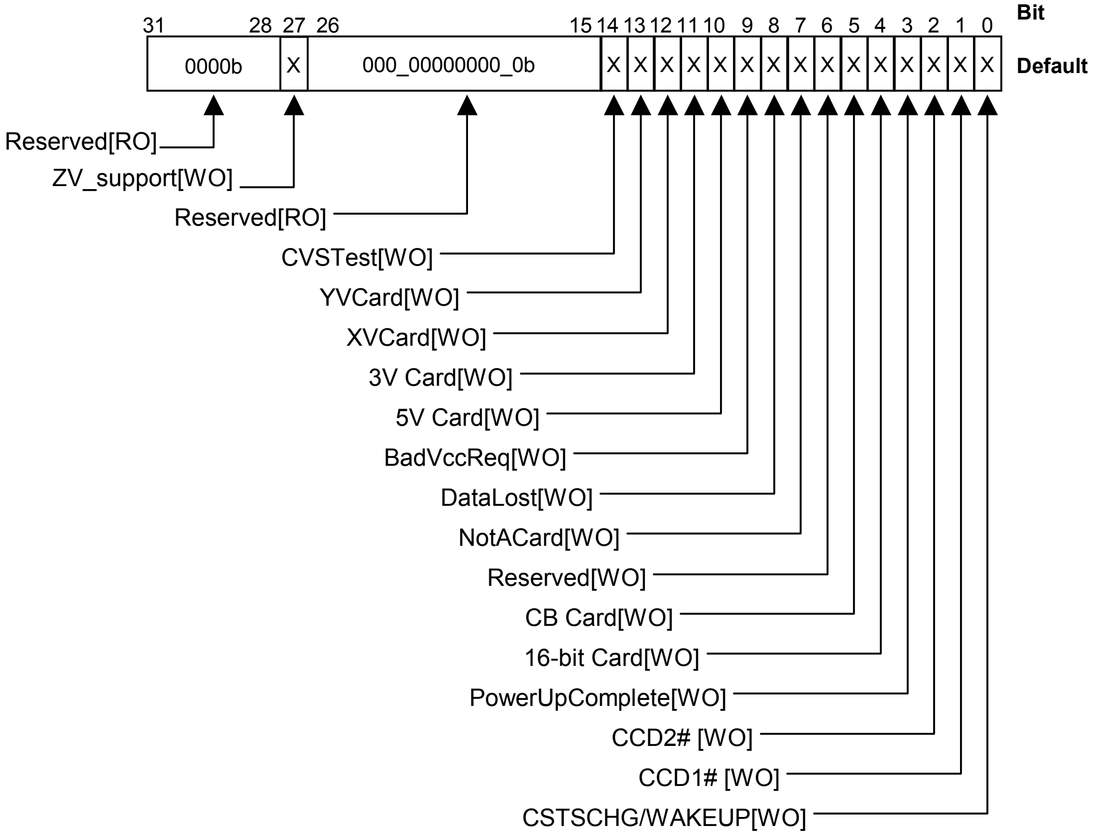
Bit	Field Name	Description
31	YVsocket	When set (1), indicates that the socket can supply Vcc=Y.YV. When cleared (0), indicates that the socket cannot supply Vcc=Y.YV. R5C485 does not support this function. So they always return zero when read.
30	XVsocket	When set (1), indicates that the socket can supply Vcc=X.XV. When cleared (0), indicates that the socket cannot supply Vcc=X.XV. R5C485 does not support this function. So they always return zero when read.
29	3Vsocket	When set (1), indicates that the socket can supply Vcc=3.3V. When cleared (0), indicates that the socket cannot supply Vcc=3.3V. R5C485 supports this function. So they always return one when read.
28	5Vsocket	When set (1), indicates that the socket can supply Vcc=5.0V. When cleared (0), indicates that the socket cannot supply Vcc=5.0V. R5C485 supports this function. So they always return one when read.
27	ZV_Support	This bit indicates whether the R5C485 supports the ZV port or not, and is read-only. The default after reset returns zero (= not support). Setting bit 27 of the Socket Event Force register to one enables to set this bit to one (= support).

Bit	Field Name	Description
26-14	Reserved	This field is reserved for future use. This field is read-only and returns zero when read. Writing to this field has no effect.
13	YVCard	The R5C485 does not support this field. Return zero when read.
12	XVCard	The R5C485 does not support this field. Return zero when read.
11	3VCard	Writing to this field cause the 3V Card field in the Present State register to be written. Setting this field disable the socket's ability to power up Vcc until the CVStest field is set. To change the voltage of a card, after forcing this bit, the bridge must either receive a PCIRST# or retest the card's supported voltages. The latter can be accomplished by forcing the CVStest bit. This is necessary to prevent software from applying an incorrect voltage to the R5C485.
10	5VCard	Writing to this field cause the 5V Card field in the Present State register to be written. Setting this field disable the socket's ability to power up Vcc until the CVStest field is set in the Force register. To change the voltage of a card, after forcing this bit, the bridge must either receive a PCIRST# or retest the card's supported voltages. The latter can be accomplished by forcing the CVStest bit. This is necessary to prevent software from applying an incorrect voltage to the R5C485.
9	BadVccReq	When set (1), indicates that software attempted to apply a Vcc voltage to a socket that was outside the range detected using the CVS [2:1] and CCD [2:1]# pins.
8	DataLost	When set (1), indicates that a PC card removal event may have caused data to be lost either because a transaction was not completed properly or data was left in the R5C485's buffers. It must be cleared by Card Services when the removal event status changed interrupt is serviced. Writing back a one to this field clears it.
7	NotACard	When set (1), indicates that the type of card inserted could not be determined, the R5C485 does not supply the power to the card. This value does not have to be updated until a recognizable card (e.g. 16-bit PC Card or CardBus PC Card) is inserted.
6	CINT#/IREQ#	When set (1), indicates that the inserted card is driving its interrupt pin true. This bit is not a registered bit and its assertion/deassertion must follow the interrupt pin from the card. This bit reflects the inverted state of CINT#/IREQ# pin as these signals are low true.
5	CBcard	When set (1), indicates that the card inserted was a CardBus PC Card. This value is not updated until a non-CardBus PC Card (e.g. 16-bit PC Card or unrecognized card) is inserted. When set, the R5C485 must configure the socket interface for CardBus PC Card.
4	16-bit Card	When set (1), indicates that the card inserted was a 16-bit PC Card. This value is not updated until a non-16-bit PC Card (e.g. CardBus PC Card or unrecognized card) is inserted. When set, the R5C485 configures the socket interface for 16-bit PC Card. Setting this field disables the R5C485's voltage checking hardware so extreme care must be taken when writing the Control register or the hardware could be damaged.
3	PowerCycle	When set (1), indicates that the interface is powered up, i.e. the power up process was successful. When cleared (0), indicates that the interface is powered down, i.e. the power up process was not successful. This field is updated by the R5C485 to communicate the status of each power up/power down request.
2	CCD2#	This field reflects the current state of the CCD2# pin on the interface. 1 indicates CCD2# is High (card is not present), 0 indicates CCD2# is low (card is present). Since the CCD2# pin could be shorted to either CVS1 or CVS2, the value stored here is for when the CVS [2:1] pins are held low.
1	CCD1#	This field reflects the current state of the CCD1# pin on the interface. 1 indicates CCD1# is High (card is not present), 0 indicates CCD1# is low (card is present). Since the CCD1# pin could be shorted to either CVS1 or CVS2, the value stored here is for when the CVS [2:1] pins are held low.
0	CSTSCHG/WAKEUP	This field reflects the current state of the CSTSCHG/WAKEUP# pin on the interface. 1 indicates CSTSCHG/WAKEUP# is asserted, 0 indicates it is deasserted. This bit is meaningless when a 16-bit PC Card is installed. CSTSCHG/WAKEUP# interrupts generated by 16-bit PC Cards are controlled via registers in that interface register space.

6.4.4 Socket Event Force register

The Socket Event Force register is a phantom register. This register provides software the ability to simulate events by forcing values in the socket's Event and Present State registers. And also, this register provides software the ability to test and restore status. Writing a one to a bit in this register sets the corresponding bit in the socket's Event and Preset State registers.

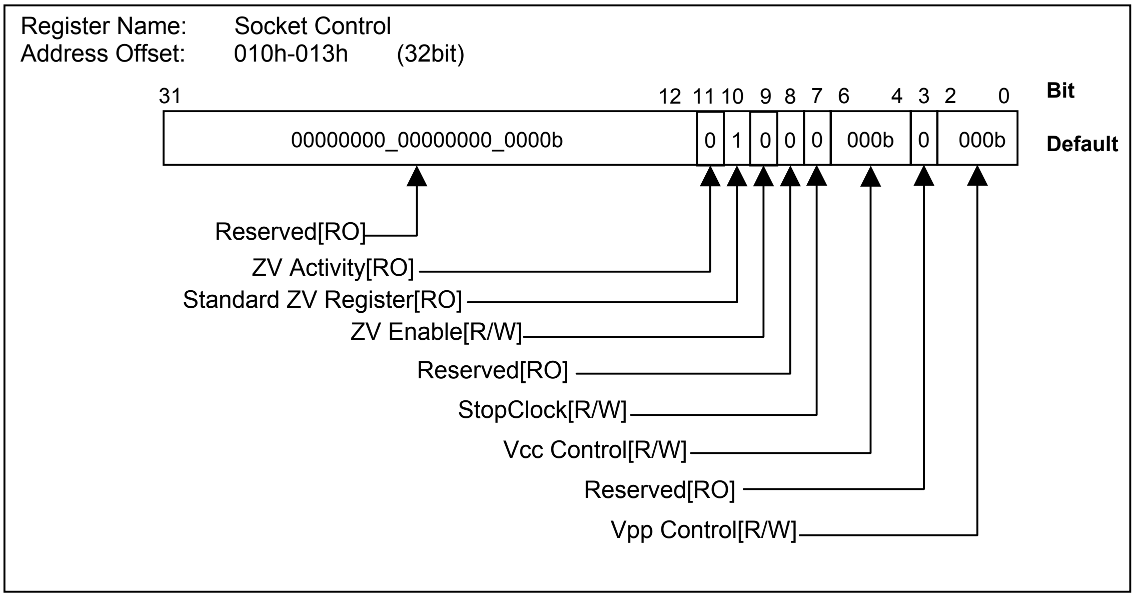
Register Name: Socket Event Force
Address Offset: 00Ch-00Fh (32bit)


Bit
31
28
27
26
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
Default
0000b
X
000_00000000_0b
X X X X X X X X X X X X X X X
Reserved[RO]
ZV_support[WO]
Reserved[RO]
CVSTest[WO]
YVCard[WO]
XVCard[WO]
3V Card[WO]
5V Card[WO]
BadVccReq[WO]
DataLost[WO]
NotACard[WO]
Reserved[WO]
CB Card[WO]
16-bit Card[WO]
PowerUpComplete[WO]
CCD2# [WO]
CCD1# [WO]
CSTSCHG/WAKEUP[WO]

Bit	Field Name	Description
31-28	Reserved	This field is reserved for future use. Writing to this field has no meaning.
27	ZV_support	Setting this bit to one enables to set the ZV Support bit of the Socket Present State register. When the socket supports the ZV port, the R5C485 must write this bit to one.
26-15	Reserved	This field is reserved for future use. Writing to this field has no meaning.
14	CVStest	When written to a 1, causes the R5C485 to interrogate the CVS [2:1] and CCD# pins and update the xVCard fields in the Present State register. This action also re-enables the socket to power up Vcc if the xVCard fields had been previously forced.
13	YVCard	The R5C485 doesn't support this function. Writing to this field has no meaning.
12	XVCard	The R5C485 doesn't support this function. Writing to this field has no meaning.
11	3VCard	Writing to this field cause the 3V Card field in the Present State register to be written. Setting this field disable the socket's ability to power up Vcc until the CVStest field is set. To change the voltage of a card, after forcing this bit, the bridge must either receive a PCIRST# or retest the card's supported voltages. The latter can be accomplished by forcing the CVStest bit. This is necessary to prevent software from applying an incorrect voltage to the R5C485.
10	5VCard	Writing to this field cause the 5V Card field in the Present State register to be written. Setting this field disable the socket's ability to power up Vcc until the CVStest field is set in the Force register. To change the voltage of a card, after forcing this bit, the bridge must either receive a PCIRST# or retest the card's supported voltages. The latter can be accomplished by forcing the CVStest bit. This is necessary to prevent software from applying an incorrect voltage to the R5C485.
9	BadVccReq	Writing to this field cause the BadVccReq field in the Present State register to be written.
8	DataLost	Writing to this field cause the DataLost field in the Present State register to be written.
7	NotACard	Writing to this field cause the NotACard field in the Present State register to be written. If a card is present in the socket (i.e. CCD1# and CCD2# are asserted), writing to this field is ignored.
6	Reserved	This field is reserved for future use. Writing to this field has no meaning.
5	CB Card	Writing to this field cause the CB Card field in the Present State register to be written. If a card is present in the socket (i.e. CCD1# and CCD2# are asserted), writing to this field is ignored.
4	16-bit Card	Writing to this field cause the 16-bit PC Card field in the Present State register to be written. If a card is present in the socket (i.e. CCD1# and CCD2# are asserted), writing to this field is ignored.
3	PowerUpComplete	Writing a 1 to this field simulates the successful completion of a power cycle event by causing the PowerCycle field in the Event register to be set. Note that the PowerCycle field in the Present State register is not affected and continues to reflect the present state of the interface power. Writing a 0 has no meaning.
2	CCD2#	Writing a 1 to this field causes the CCD2# field in the Event register to be set. Note that the CCD2# field in the Present State register is not affected and continues to reflect the present state of the CCD2# pin. Writing a 0 has no meaning.
1	CCD1#	Writing a 1 to this field causes the CCD1# field in the Event register to be set. Note that the CCD1# field in the Present State register is not affected and continues to reflect the present state of the CCD1# pin. Writing a 0 has no meaning.
0	CSTSCHG	Writing a 1 to this field simulates the assertion of the CSTSCHG pin. This results in the Event register's CSTSCHG field being set. Note that the CSTSCHG field in the Present State register is not affected and continues to reflect the present state of the CSTSCHG pin. Writing a 0 has no meaning.

6.4.5 Socket Control register

The Socket Control Register provides control of the socket's Vcc and Vpp. All bits in this register is cleared to zero and the power is removed from the socket when PCITST# is asserted. The supply voltage to the PC card is determined by the interrogation of CCD1#, CCD2#, CVS1, and CVS2 according to the card type detection mechanism described in the CardBus specification. The R5C485 do not supply a Vcc voltage that is not indicated by the VS decode.



Register Name: Socket Control
Address Offset: 010h-013h (32bit)

31
12 11 10 9 8 7 6 4 3 2 0
Bit
00000000_00000000_0000b
0 1 0 0 0 000b 0 000b
Default
Reserved[RO]
ZV Activity[RO]
Standard ZV Register[RO]
ZV Enable[R/W]
Reserved[RO]
StopClock[R/W]
Vcc Control[R/W]
Reserved[RO]
Vpp Control[R/W]

Bit	Field Name	Description
31-12	Reserved	This field is reserved for future use. This field is read-only and returns zero when read. Writing to this field has no meaning.
11	ZV_Actibity	When the ZV port is enabled, this bit is set to one.
10	Standard ZV Register	This bit indicates whether register's set for the standard ZV port is supported. The R5C485 returns one because the R5C485 supports.
9	ZV Enable	Setting this bit to one enables the ZV port of the socket.
8	Reserved	This field is reserved for future use. This field is read-only and returns zero when read. Writing to this field has no meaning.
7	StopClock	Setting this bit to one, stops the CardBus clock complying CCLKRUN# protocol. If the card does not support this protocol, the CardBus clock will be stopped regardless of the card status. The default after reset is zero.
6-4	Vcc Control	This field is used to control the Vcc power to the PC Card via external control logic. The bridge determines the voltages that can be applied by decoding the CD and VS signals per the CardBus specification. Those bits and the voltages available in the system determine the correct Vcc options. The value written to this register must agree with the value needed to apply the correct value of Vcc. The bridge must not allow an incorrect Vcc voltage to be applied to a socket. The voltages available are shown in the Status Register. Bit 654 VCC3EN# VCC5EN#* 000 Requested Vcc voltage = power off H H 001 Reserved H H 010 Requested Vcc voltage = 5.0V H L 011 Requested Vcc voltage = 3.3V L H 100 Reserved H H 101 Reserved H H 110 Reserved H H 111 Reserved H H * if permitted
3	Reserved	This bit is reserved for future use. This bit is read-only and returns zero. Writing to this field has no meaning.
2-0	Vpp Control	This field is used to switch the Vpp power using external Vpp control logic. The bridge has no knowledge of a card's Vpp voltage requirement. Software must determine the needed voltage from the card's CIS. Bit 210 VPPEN0 VPPEN1* 000 Requested Vpp voltage = power off L L 001 Requested Vpp voltage = 12.0V L H 010 Requested Vpp voltage = 5.0V H L 011 Requested Vpp voltage = 3.3V H L 100 Reserved L L 101 Reserved L L 110 Reserved L L 111 Reserved L L * if permitted

7 16-BIT (PC CARD-16) SOCKET STATUS/CONTROL REGISTERS

7.1 Overview

The PC Card-16 Socket Status/Control Registers manage status changed events, remote wakeup events, PC Card insertion/removal, and status information about the PC Card in the socket. These registers are used only for PC Card-16.

7.2 Register Space Mapping

The Socket Status/Control Registers for PC Card-16 are placed in the top 2Kbyte of the memory mapped I/O space of 4Kbyte pointed by the PC Card Control Register Base Address Register and start at offset 800h. (The bottom 2Kbyte is assigned to PC Card-32 Socket Status/Control Register set.) These registers can be also accessed through INDEX/DATA port residing I/O address 3E0/3E2, and maintain the backward compatibility with ISA-PCMCIA controllers.

7.3 Register Configuration

A socket has the PC Card-16 Socket Status/Control Register set that consist of 64 BYTE registers. One set of registers is described in the following sections. Address offset 845h through FFCh is assigned to reserved register. The reserved registers return 00000000h when read. Writing to the reserved registers has no effect.

Mapping Offset	Legacy Index A	Register Name	Mnemonic	Note
800h	00h	Identification and Revision	IDREVS	
801h	01h	Interface Status	IFSTAT	
802h	02h	Power Control	PWCTRL	
803h	03h	Interrupt and General Control	IGCTRL	
804h	04h	Card Status Change	CSCHG	
805h	05h	Card Status Change Interrupt Configuration	CSCINT	
806h	06h	Address Window Enable	AWINEN	
807h	07h	I/O control	IOCTRL	
808h	08h	I/O address 0 Start Low Byte	IOSTL0	
809h	09h	I/O address 0 Start High Byte	IOSTH0	
80Ah	0Ah	I/O address 0 Stop Low Byte	IOSPL0	
80Bh	0Bh	I/O address 0 Stop High Byte	IOSPH0	
80Ch	0Ch	I/O address 1 Start Low Byte	IOSTL1	
80Dh	0Dh	I/O address 1 Start High Byte	IOSTH1	
80Eh	0Eh	I/O address 1 Stop Low Byte	IOSPL1	
80Fh	0Fh	I/O address 1 Stop High Byte	IOSPH1	
810h	10h	System Memory Address 0 Mapping Start Low Byte	SMSTL0	
811h	11h	System Memory Address 0 Mapping Start High Byte	SMSTH0	
812h	12h	System Memory Address 0 Mapping Stop Low Byte	SMSPL0	
813h	13h	System Memory Address 0 Mapping Stop High Byte	SMSPH0	
814h	14h	Card Memory Offset Address 0 Low Byte	MOFFL0	
815h	15h	Card Memory Offset Address 0 High Byte	MOFFH0	
816h	16h	Card Detect and General Control	CDGENC	

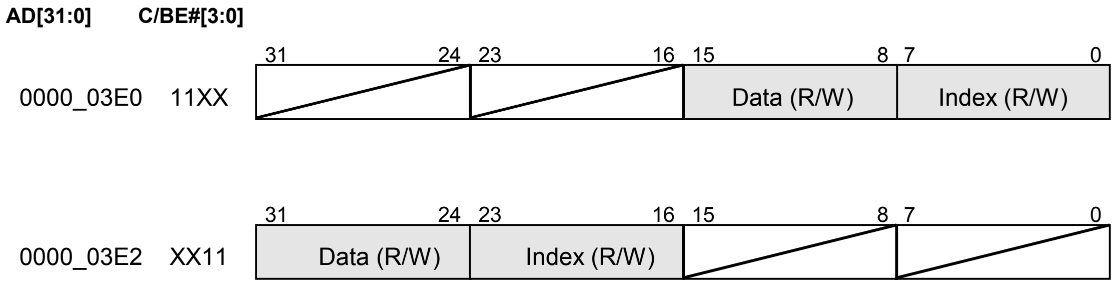
Mapping Offset	Legacy Index A	Register Name	Mnemonic	Note
817h	17h	Reserved	RSRVD	
818h	18h	System Memory Address 1 Mapping Start Low Byte	SMSTL1	
819h	19h	System Memory Address 1 Mapping Start High Byte	SMSTH1	
81Ah	1Ah	System Memory Address 1 Mapping Stop Low Byte	SMSPL1	
81Bh	1Bh	System Memory Address 1 Mapping Stop High Byte	SMSPH1	
81Ch	1Ch	Card Memory Offset Address 1 Low Byte	MOFFL1	
81Dh	1Dh	Card Memory Offset Address 1 High Byte	MOFFH1	
81Eh	1Eh	16 bit Global Control	GLCTRL	
81Fh	1Fh	ATA Control	ATCTRL	
820h	20h	System Memory Address 2 Mapping Start Low Byte	SMSTL2	
821h	21h	System Memory Address 2 Mapping Start High Byte	SMSTH2	
822h	22h	System Memory Address 2 Mapping Stop Low Byte	SMSPL2	
823h	23h	System Memory Address 2 Mapping Stop High Byte	SMSPH2	
824h	24h	Card Memory Offset Address 2 Low Byte	MOFFL2	
825h	25h	Card Memory Offset Address 2 High Byte	MOFFH2	
826h	26h	Reserved	RSRVD	
827h	27h	Reserved	RSRVD	
828h	28h	System Memory Address 3 Mapping Start Low Byte	SMSTL3	
829h	29h	System Memory Address 3 Mapping Start High Byte	SMSTH3	
82Ah	2Ah	System Memory Address 3 Mapping Stop Low Byte	SMSPL3	
82Bh	2Bh	System Memory Address 3 Mapping Stop High Byte	SMSPH3	
82Ch	2Ch	Card Memory Offset Address 3 Low Byte	MOFFL3	
82Dh	2Dh	Card Memory Offset Address 3 High Byte	MOFFH3	
82Eh	2Eh	Reserved	RSRVD	
82Fh	2Fh	Misc Control 1	MISCC1	
830h	30h	System Memory Address 4 Mapping Start Low Byte	SMSTL4	
831h	31h	System Memory Address 4 Mapping Start High Byte	SMSTH4	
832h	32h	System Memory Address 4 Mapping Stop Low Byte	SMSPL4	
833h	33h	System Memory Address 4 Mapping Stop High Byte	SMSPH4	
834h	34h	Card Memory Offset Address 4 Low Byte	MOFFL4	
835h	35h	Card Memory Offset Address 4 High Byte	MOFFH4	
836h	36h	Card I/O Offset Address 0 Low Byte	IOFFL0	
837h	37h	Card I/O Offset Address 0 High Byte	IOFFH0	
838h	38h	Card I/O Offset Address 1 Low Byte	IOFFL1	
839h	39h	Card I/O Offset Address 1 High Byte	IOFFH1	
83Ah	3Ah	General Purpose I/O	GPIO	
83Bh	3Bh	Reserved	RSRVD	
83Ch	3Ch	Reserved	RSRVD	
83Dh	3Dh	Reserved	RSRVD	
83Eh	3Eh	Reserved	RSRVD	
83Fh	3Fh	Reserved	RSRVD	
840h	NA	System Memory Page Address 0	SMPGA0	
841h	NA	System Memory Page Address 1	SMPGA1	
842h	NA	System Memory Page Address 2	SMPGA2	

Mapping Offset	Legacy Index A	Register Name	Mnemonic	Note
843h	NA	System Memory Page Address 3	SMPGA3	
844h	NA	System Memory Page Address 4	SMPGA4	

7.4 PCIC Compatible mode (Legacy Mode)

The R5C485 supports the PCIC compatible mode, i.e. Legacy mode, that all 16-bit Card Sockets Status/Control registers can be accessed through INDEX/DATA ports that is located at I/O address 03E0h or 03E2h. Writing a non-zero address to 16-bit Legacy Mode Base Address register enables the PCIC compatible mode. The index register and the data register are contiguous in the I/O address space so that a single 16-bit instruction can simultaneously write to the index and data registers. Setting the Legacy Index Range bit (bit3-2) in the 16-bit Interface Control register in the PCI configuration space enables the index range to set to which one of 00h to 3Fh, 40h to 7Fh, 80h to BFh and C0h to FFh.
The below figure shows the status of INDEX/DATA ports when the Legacy Base Address register is set to either 03E0h or 03E2h.

Register Name: Legacy Index/Data Port
PCI I/O Address : 03E0h (or 03E2h)

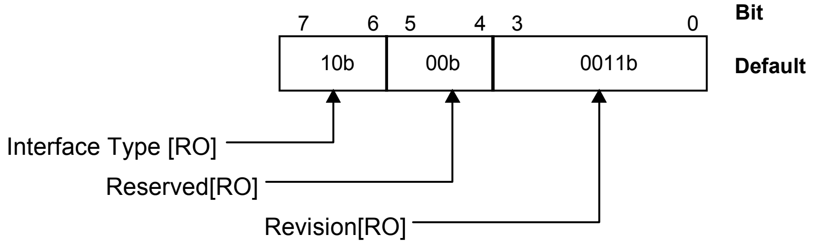


7.5 General Setup Registers

7.5.1 Identification and Revision register

This register provides the software with information on PC Card-16.

Register Name: Identification and Revision
Address Offset: 800h

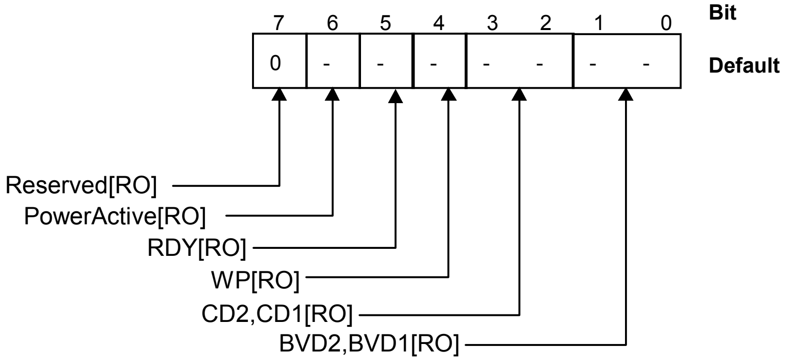


Bit	Field Name	Description
7-6	InterfaceType	This field indicates the type of PC Card-16 supported by the R5C485. The R5C485 supports the 16-bit card on the Memory and I/O interface and return 10b when read. 00b I/O only 01b Memory 10b Memory & I/O 11b Reserved
5-4	Reserved	These bits are reserved for future use. This field is read-only and returns zero when read.
3-0	Revision	This field indicates PCIC revision number. This filed is read-only and returns 0011b when read.

7.5.2 Interface Status register

This register provides information on the status of the PC Card interface.

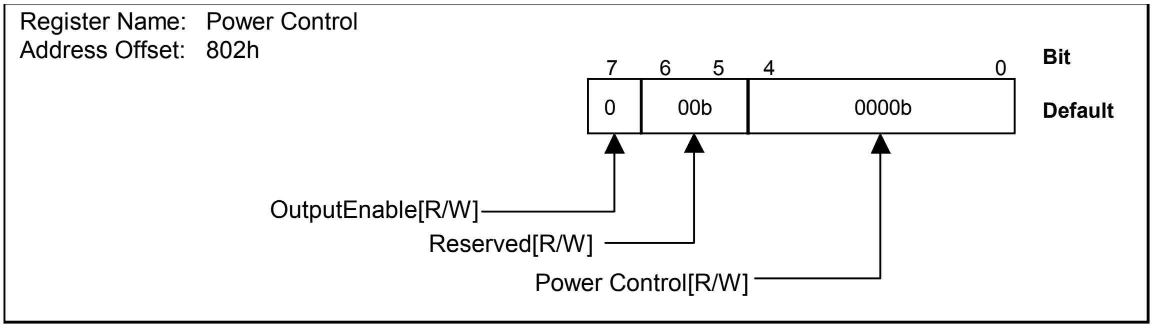
Register Name: Interface Status
Address Offset: 801h



Bit	Field Name	Description
7	Reserved	This bit is reserved for future use. This bit is read-only and returns zero when read. Writing to this field has no effect.
6	PowerActive	This bit indicates whether or not the socket power is on (3.3V or 5V). This bit is set to one when either VCC3EN# or VCC5EN# is turned on, and set to zero when the socket power is turned off.
5	RDY	This bit indicates the state of the READY/IREQ# input signal. This bit is available only on the PC Card-16 memory interface, and has no meaning on the I/O interface. 0b memory card is busy. 1b memory card is ready.
4	WP	This bit indicates the state of the WP/IOIS16# input signal. The memory card will not be write protected unless the WriteProtect bit in the Card Memory Offset High Byte register is set to one, even if the WP signal is a one to maintain the compatibility with 82365SL B-Step. This bit is available only on the PC Card-16 memory interface.
3-2	CD2, CD1	This field returns the inverse state of CD2# and CD1# when read.
1-0	BVD2, BVD1	These bits have meanings that depend on the type of the PC Card-16 inserted in the socket. When a 16-bit memory card is inserted, this field indicates the state of the battery voltage detect signals (BVD1, BVD2) as follows: BVD2 BVD1 bit1 bit0 Card Battery Low Low 0 0 Battery Dead Low High 0 1 Warning High Low 1 0 Battery Dead High High 1 1 Battery Good When a 16-bit I/O card is inserted, Bit 0 in this field indicates the state of the BVD1#/STSCHG#/RI# input signal when the Ring Indicate Enable bit in the Interrupt and General Control register is a zero.

7.5.3 Power Control register

This register controls the output of the R5C485 to the PC Card-16 socket. This register can also control the socket power to maintain the compatibility with the PCIC.



Register Name: Power Control
Address Offset: 802h

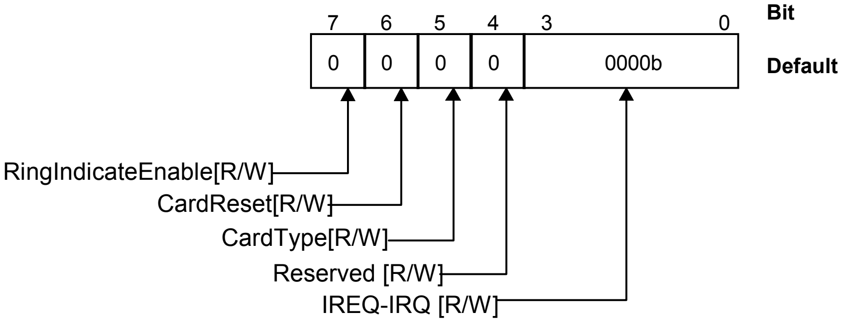
Bit	Field Name	Description
7	OutputEnable	When the R5C485 is on the 16-bit card mode, the output signals listed below are tri-stated when this bit is set to zero, and they are not tri-stated when this bit is set to one. The following output signals are the object: CE1#, CE0#, IORD#, IOWR#, OE#, WE#, RESET, ADR [25:0], DATA [15:0], REG#
6-5	Reserved(R/W)	This read/write bit is reserved for future use. Writing to this bit has no effect. The default after reset is zero.
4-0	Power Control	This bit field is used with Bit 0 in the Misc Control 1 register to control VCC3EN#, VCC5EN#, VPPEN0 and VPPEN1. Writing to these bits is enabled only either when the power is on or the voltage is changed. The following table shows the relation between power control signals and this bit field.

Bit4	Bit3	Bit2	Bit1	Bit0	Misc Control 1 Bit0	VCC3EN#	VCC5EN#	VPPEN1	VPPEN0
1	X	X	0	0	0	1	0	0	0
1	X	X	0	0	1	0	1	0	0
1	X	X	0	1	0	1	0	0	1
1	X	X	0	1	1	0	1	0	1
1	X	X	1	0	0	1	0	1	0
1	X	X	1	0	1	0	1	1	0
1	X	X	1	1	0	1	0	0	1
1	X	X	1	1	1	0	1	0	1
0	X	X	X	X	X	1	1	0	0

7.5.4 Interrupt and General Control register

This register controls Ring Indicate Enable, Card Reset, Card Type and Interrupt Steering of IRQs from I/O PC Card-16.

Register Name: Interrupt and General Control
Address Offset: 803h



Bit	Field Name	Description
7	RingIndicateEnable	On the I/O card interface mode, when this bit is set to one, the STSCHG#/RI# from the PC Card-16 signal is used as a Ring Indicator signal, and is passed through to the RI_OUT# pin. When this bit is set to zero, the STSCHG#/RI# from the I/O PC Card-16 signal is used as the status change signal STSCHG#. The current status of the signal is then available to the read from the Interface Status register and this signal can be configured as a source for the card status change interrupt. This bit has no meaning on the memory card interface mode.
6	CardReset	When this bit is set to zero, the Reset signal to the PC Card-16 is activates. This signal will be active until this bit is set to one,
5	CardType	This bit indicates the PC Card type. When this bit is set to zero, a memory card interface is selected. When this bit is set to one, an I/O card interface is selected.
4	Reserved(R/W)	This read/write bit is reserved for future use.
3-0	IREQ-IRQ	This field selects the interrupt routing for the IREQ#/CINT# signal from I/O PC Card-16. These bits are available only when the IREQ-ISA Enable bit in the Bridge control register is set bit3 bit2 bit1 bit0 IRQ selection 0 0 0 0 IRQ disabled 0 0 0 1 Reserved 0 0 1 0 Reserved 0 0 1 1 IRQ3 0 1 0 0 IRQ4 0 1 0 1 IRQ5 0 1 1 0 Reserved 0 1 1 1 IRQ7 1 0 0 0 Reserved 1 0 0 1 IRQ9 1 0 1 0 IRQ10 1 0 1 1 IRQ11 1 1 0 0 IRQ12 1 1 0 1 Reserved 1 1 1 0 IRQ14 1 1 1 1 IRQ15

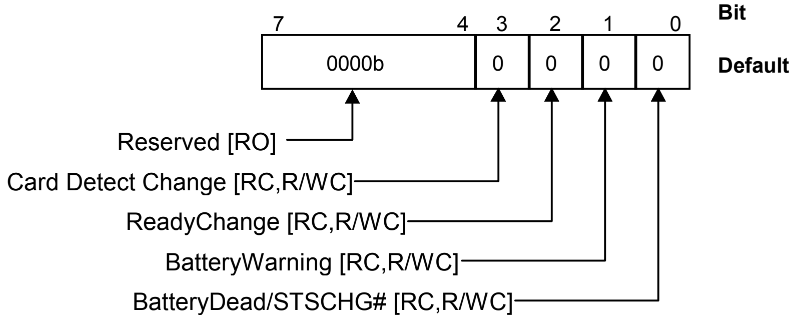
7.5.5 Card Status Change register

This register contains the status for sources of the card status change interrupts. These sources can be enabled to generate a card status change interrupt by setting the corresponding bit in the Card Status Change Interrupt Configuration register. Each bits in this register read back 0 when the corresponding status enable bits in the Card Status change Interrupt Configuration are set to 0.

When the Card Status Change Acknowledge mode bit in the 16-bit Global Control register is set to 1, the acknowledgment of sources for the Card Status Change Interrupt is performed by writing back 1 to the appropriate bit in the Cad Status Change Register that was read as 1b. Once the internal source is acknowledged by writing a 1 to the bit, the bit reads back as 0. The interrupt signal INTA# or IRQx responding to the card status change maintains to be active, if enabled on a system IRQ line, until all of the bits in this register are zero. When the Card Status Change Acknowledge mode bit in the 16-bit Global Control register is not set, the Card Status Change Interrupt signal maintains to be active, if enabled on a system IRQ line, until the Card Status Change register is read. The read operation to the Card Status Change register resets all bits in the register.

If two or more Card Status Change Interrupts are pending or a Card Status Change Interrupt condition occurs while another is being serviced, the R5C485 does not generate a second interrupt. The interrupt service routing must read the Card Status Change register to ensure that all interrupt request is serviced before exiting the service routines.

Register Name: Card Status Change
Address Offset: 804h

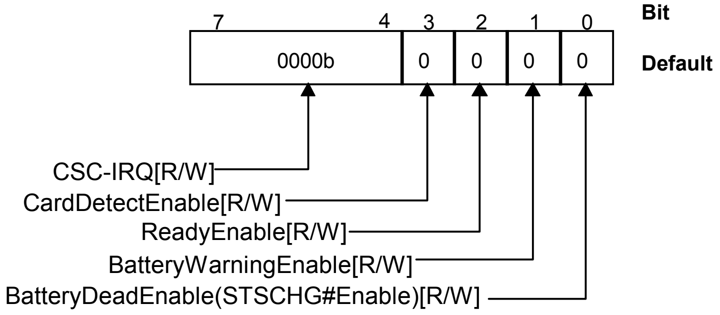


Bit	Field Name	Description
7-4	Reserved	This field is reserved for future use. This field is read-only and returns zeros when read.
3	Card Detect Change	This bit is set to 1 when a change on either CD1# or CD2# signals occurs. This bit is not set unless the Card Detect Enable bit in the Card Status Change Interrupt Configuration register is set. Both CCD1# and CCD2# bits in the Socket Event register are cleared by a read clear or a write back clear. And also, this bit is cleared when either CCD1# or CCD2#, or both of CCD1# and CCD2# are cleared by a write back clear.
2	ReadyChange	This bit is set to1 when a low-to-high transition occurs on the RDY/BSY# signal, indicating that the memory PC Card-16 is ready to accept a new data transfer. This bit is not set unless the Ready Enable bit in the Card Status Change Interrupt Configuration register is set. This bit is always zero on I/O PC Card-16.
1	BatteryWarning	This bit is set to1 when a battery warning condition is detected. This bit is not set unless the Battery Warning Enable bit in the Card Status Change Interrupt Configuration register is set. This bit is always zero on I/O PC Card-16.
0	BatteryDead /STSCHG#	On the memory PC Card-16 interface mode, this bit is set to 1 when a battery dead condition is detected. On the I/O PC Card-16 interface mode, this bit is set to 1 when the BVD1/STSCHG# signal is asserted “low”, but then, this bit reads back as 0 if the Ring Indicate Enable bit in the Interrupt and General Control register is set to 1. This bit is not set unless the Battery Enable bit in the Card Status Change Interrupt Configuration register is set.

7.5.6 Card Status Change Interrupt Configuration register

This register controls the steering of Card Status Change Interrupt and the enabling of Card Status Change Interrupt.

Register Name: Card Status Change Interrupt Configuration
Address Offset: 805h

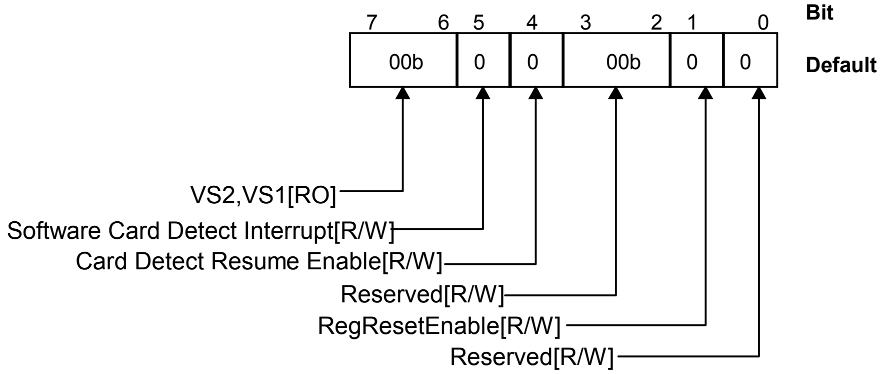


Bit	Field Name	Description
7-4	CSC-IRQ	This field selects the interrupt routing for card status change interrupts. When this field is set to the reserved value or 0000b, the card status change interrupt is routed to INTA#. The default after reset is 0000b. This field is reset when the RegResetEnable bit in the Card Detect and General Control register is set and the card is removed. bit7 bit6 bit5 bit4 IRQ selection 0 0 0 0 IRQ disabled 0 0 0 1 Reserved 0 0 1 0 Reserved 0 0 1 1 IRQ3 0 1 0 0 IRQ4 0 1 0 1 IRQ5 0 1 1 0 Reserved 0 1 1 1 IRQ7 1 0 0 0 Reserved 1 0 0 1 IRQ9 1 0 1 0 IRQ10 1 0 1 1 IRQ11 1 1 0 0 IRQ12 1 1 0 1 Reserved 1 1 1 0 IRQ14 1 1 1 1 IRQ15
3	CardDetectEnable	When this bit is set to 1, the interrupt is generated when a change is detected on either CD1# or CD2#.
2	ReadyEnable	Setting this bit to 1 enables the card status change interrupt when a low-to-high transaction occurs on the RDY/BSY# signal. This bit has no meaning on the I/O PC Card-16 interface.
1	BatteryWarningEnable	Setting this bit to 1 enables the card status change interrupt when a battery warning conditions is detected. This bit has no meaning on the I/O PC-Card-16 interface.
0	BatteryDeadEnable (STSCHG#Enable)	Setting this bit to 1 enables a Card Status Change Interrupt when a battery dead condition is detected in a memory PC Card-16. In an I/O PC Card-16, setting this bit to 1 enables a Card Status Change Interrupt when the BVD1/STSCHG# signal is pulled “Low”. Setting this bit to 0 disables the interrupt.

7.5.7 Card Detect and General Control register

This register is used to reset the configuration registers and report the selected status of voltage stored to the card.

Register Name: Card Detect and General Control
Address Offset: 816h

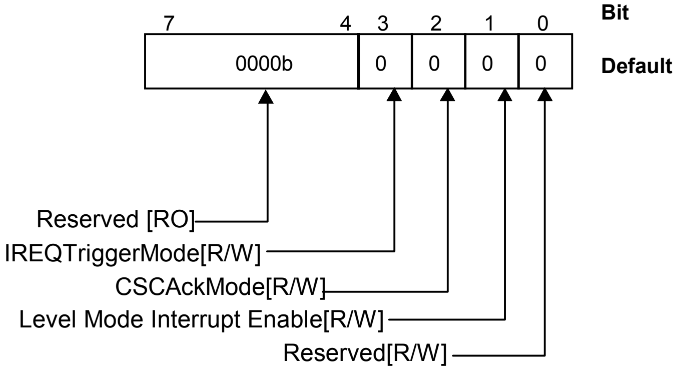


Bit	Field Name	Description
7-6	VS2, VS1	These bits indicate the state of VS2 and VS1. The default after reset is zero.
5	Software Card Detect Interrupt	Setting this bit to 1 enables to generate the Card Detected Interrupt, and then one should note that both CCD1# and CCD2# bits in the Socket Event register are set by writing to this bit. This bit is a phantom bit and returns zero when read.
4	Card Detect Resume Enable	When this bit is set to1, then once a card detect change is detected on the CD1# or CD2# inputs, RI_OUT# output goes from “high” to “low”.
3-2	Reserved(R/W)	This read/write field is reserved for future use. The default after reset is zero.
1	RegResetEnable	When this bit is set to 1, a reset pulse is generated to reset the following configuration registers for the socket to their default state (zero’s) when both the CD1# and CD2# inputs for the socket go “high”. Interrupt and General Control Card Detect Interrupt Configuration (CSC-IRQ bits only*) Address Window Enable I/O Control I/O Address {0,1} Start Low Byte I/O Address {0,1} Start High Byte I/O Address {0,1} Stop Low Byte I/O Address {0,1} Stop High Byte System Memory Address {0,1,2,3,4} Start Low Byte System Memory Address {0,1,2,3,4} Start High Byte System Memory Address {0,1,2,3,4} Stop Low Byte System Memory Address {0,1,2,3,4} Stop High Byte Card Memory Offset Address {0,1,2,3,4} Start Low Byte Card Memory Offset Address {0,1,2,3,4} Start High Byte Card Memory Offset Address {0,1,2,3,4} Stop Low Byte Card Memory Offset Address {0,1,2,3,4} Stop High Byte
0	Reserved(R/W)	This read/write bit is reserved for future use. The default after reset is zero.

7.5.8 16 bit Global Control register

This register controls both PC Card sockets, and is not duplicated for each socket. PCI reset clears all bits in this register.

Register Name: 16 bit Global Control
Address Offset: 81Eh

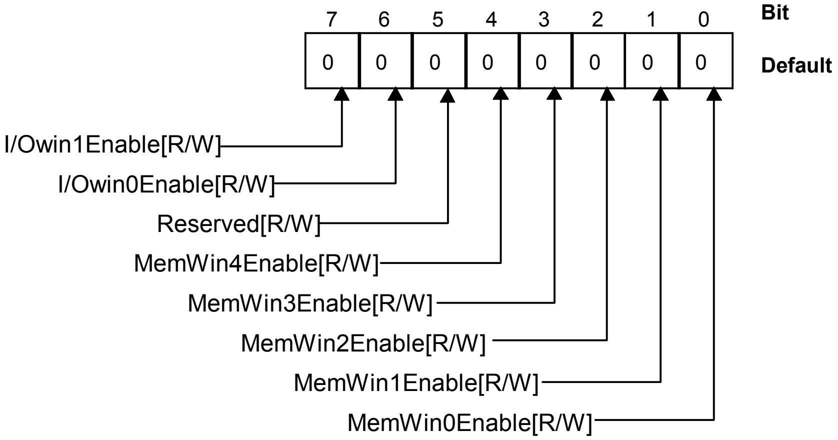


Bit	Field Name	Description
7-4	Reserved	This field is reserved for future use. This field is read-only and returns zero when read.
3	IREQTriggerMode	This bit selects level mode interrupts for IRQx generated by the particular PC card interrupts. When this bit is set to 1, it selects level mode. And also when this bit is set to 0, it selects edge mode. The default is zero.
2	CSCAckMode	When this bit is set to 1, each Card Status Change Interrupt is acknowledged with an explicit write of 1 to the Card Status Change register bit that identifies the interrupt. - A corresponding bit is reset to 0. When this bit to 0, each Card Status Change Interrupt is acknowledged by reading the Card Status Change register. - All bits are reset to 0.
1	Level Mode Interrupt Enable	When this bit is set to1, level mode is selected. And IRQx goes from tri-stated to low whenever the interrupt is active. When this bit is set to 0, edge mode is selected. And IRQx go from tri-stated to low when the interrupt is enabled, and go from low to high when the interrupt is active, and also go to low when the interrupt is inactive. This bit is tri-stated when the interrupt is disabled.
0	Reserved(R/W)	This read/write bit is reserved for future use.

7.5.9 Address Window Enable register

This register controls enabling of the memory and I/O mapping windows to the PC Card memory or I/O space. All bits in this register are cleared after reset.

Register Name: Addres Window Enable
Address Offset: 806h


7 6 5 4 3 2 1 0
Bit
0 0 0 0 0 0 0 0
Default
I/Owin1Enable[R/W]
I/Owin0Enable[R/W]
Reserved[R/W]
MemWin4Enable[R/W]
MemWin3Enable[R/W]
MemWin2Enable[R/W]
MemWin1Enable[R/W]
MemWin0Enable[R/W]

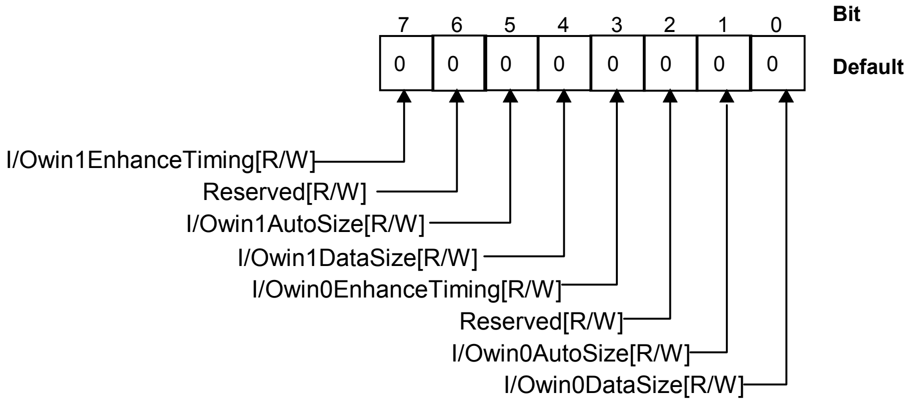
Bit	Field Name	Description
7	I/Owin1Enable	This bit controls whether or not the I/O window 1 is enabled. When this bit is set to 0, the card enable signal is inhibited to access to the PC Cards through the I/O window 1. When this bit is set to 1, the card enable signal is not inhibited when access addresses to the PC Cards are passed to the I/O window 1. Start and Stop registers in the corresponding window must be set to the proper value before setting this bit.
6	I/Owin0Enable	This bit controls whether or not the I/O window 0 is enabled. When this bit is set to 0, the card enable signal is inhibited to access to the PC Cards through the I/O window 0. When this bit is set to 1, the card enable signal is not inhibited when access addresses to the PC Cards are passed to the I/O window 0. Start and Stop registers in the corresponding window must be set to the proper value before setting this bit.
5	Reserved(R/W)	This read/write bit is reserved for future use. The default after reset is zero.
4	MemWin4Enable	This bit controls whether or not the memory window 4 is enabled. When this bit is set to 0, the card enable signal is inhibited to access to the PC Cards through the memory window 4. When this bit is set to 1, the card enable signal is not inhibited when access addresses to the PC Cards are passed to the memory window 4. Start and Stop registers in the corresponding window must be set to the proper value before setting this bit.
3	MemWin3Enable	This bit controls whether or not the memory window 3 is enabled. When this bit is set to 0, the card enable signal is inhibited to access to the PC Cards through the memory window 3. When this bit is set to 1, the card enable signal is not inhibited when access addresses to the PC Cards are passed to the memory window 3. Start and Stop registers in the corresponding window must be set to the proper value before setting this bit.
2	MemWin2Enable	This bit controls whether or not the memory window 2 is enabled. When this bit is set to 0, the card enable signal is inhibited to access to the PC Cards through the memory window 2. When this bit is set to 1, the card enable signal is not inhibited when access addresses to the PC Cards are passed to the memory window 2. Start and Stop registers in the corresponding window must be set to the proper value before setting this bit.
1	MemWin1Enable	This bit controls whether or not the memory window 1 is enabled. When this bit is set to 0, the card enable signal is inhibited to access to the PC Cards through the memory window 1. When this bit is set to 1, the card enable signal is not inhibited when access addresses to the PC Cards are passed to the memory window 1. Start and Stop registers in the corresponding window must be set to the proper value before setting this bit.
0	MemWin0Enable	This bit controls whether or not the memory window 0 is enabled. When this bit is set to 0, the card enable signal is inhibited to access to the PC Cards through the memory window 0. When this bit is set to 1, the card enable signal is not inhibited when access addresses to the PC Cards are passed to the memory window 0. Start and Stop registers in the corresponding window must be set to the proper value before setting this bit.

7.6 I/O Window Control Register Description

7.6.1 I/O Control register

This register controls the I/O data path size and the access timing specification for the I/O windows 0 and 1. All bits in this register are cleared after reset.

Register Name: I/O Control
Address Offset: 807h

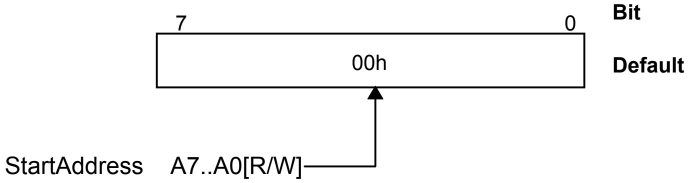


Bit	Field Name	Description
7	I/Owin1Enhance Timing	When this bit is set to 1, 16-bit I/O card access timing for I/O window 1 is determined by user defined timing in the 16-bit I/O timing 0 register. When this bit is set to 0, the default timing is selected. The default after reset is zero. User defined timing is valid when 16-bit I/O Enhance Timing bit in the 16-bit Interface Control register is set to 1 regardless of this bit being set to 0.
6	Reserved(R/W)	This read/write bit is reserved for future use. The default after reset is zero.
5	I/Owin1AutoSize	This bit indicates how to select the I/O data path size to the PC Card-16. When this bit is set to 1, the data path size for I/O window 1 is determined by the IOIS16# signal from PC Card-16. When this bit is set to 0, it is determined by the I/Owin1DataSize bit.
4	I/Owin1DataSize	This bit selects the I/O data path size to the PC Card-16. When this bit is set to 1, 16-bit data path is selected. When this bit is set to 0, 8-bit data path is selected. This bit is ignored when I/Owin1AutoSize is 1b. This bit takes precedence of PCI command.
3	I/Owin0Enhance Timing	When this bit is set to 1, 16-bit I/O card access timing for I/O window 0 is determined by user defined timing in the 16-bit I/O timing 0 register. When this bit is set to 0, the default timing is selected. The default after reset is zero. User defined timing is valid when 16-bit I/O Enhance Timing bit in the 16-bit Interface Control register is set to 1 regardless of this bit being set to 0.
2	Reserved(R/W)	This read/write bit is reserved for future use. The default after reset is zero.
1	I/Owin0AutoSize	This bit indicates how to select the I/O data path size to the PC Card-16. When this bit is set to 1, the data path size for I/O window 0 is determined by the IOIS16# signal from PC Card-16. When this bit is set to 0, it is determined by the I/Owin0DataSize bit.
0	I/Owin0DataSize	This bit selects the I/O data path size to the PC Card-16. When this bit is set to 1, 16-bit data path is selected. When this bit is set to 0, 8-bit data path is selected. This bit is ignored when I/Owin0AutoSize is 1b. This bit has priority over the PCI command.

7.6.2 I/O Address 0-1 Start Low Byte register

These two registers contain the lower address bits that are used to determine the start address of the corresponding I/O address windows 0 and 1. This provides a minimum 1 byte window for the corresponding I/O address window if the start address and stop address are the same.

Register Name: I/O Address 0-1 Start Low Byte
Address Offset: 808h,80Ch



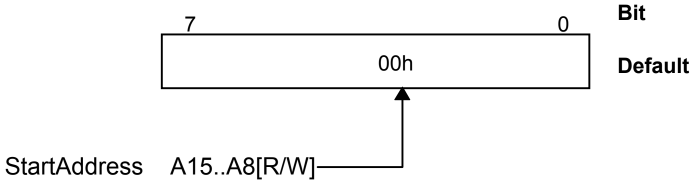
	Window 0	*Window 1*
Offset	808h	80Ch

Bit	Field Name	Description
7-0	StartAddress A7..A0	I/O Window 0-1 Start Address A7 .. A0:

7.6.3 I/O Address 0-1 Start High Byte register

These two registers contain the upper address bits that are used to determine the start address of the corresponding I/O address windows 0 and 1.

Register Name: I/O Address 0-1 Start High Byte
Address Offset: 809h,80Dh



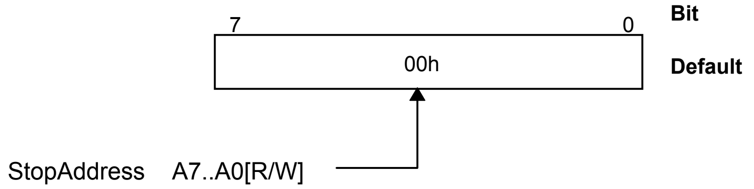
	Window 0	*Window 1*
Offset	809h	80Dh

Bit	Field Name	Description
7-0	StartAddress A15..A8	I/O Window 0-1 Start Address A15..A8:

7.6.4 I/O Address 0-1 Stop Low Byte register

These two registers contain the lower address bits that are used to determine the top address of the corresponding I/O address windows 0 and 1. This provides a minimum 1 byte window for the corresponding I/O address window if the start address and stop address are the same.

Register Name: I/O Address 0-1 Stop Low Byte
Address Offset: 80Ah,80Eh



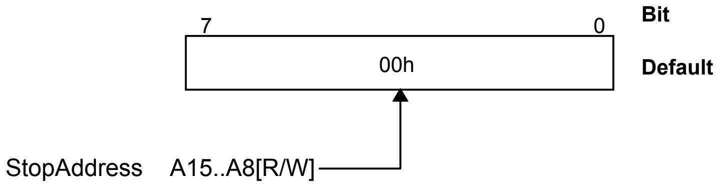
	Window 0	*Window 1*
Offset	80Ah	80Eh

Bit	Field Name	Description
7-0	StopAddress A7..A0	I/O Window 0-1 Stop Address A7 .. A0:

7.6.5 I/O Address 0-1 Stop High Byte register

These two registers contain the upper address bits that are used to determine the stop address of the corresponding I/O address windows 0 and 1.

Register Name: I/O Address 0-1 Stop High Byte
Address Offset: 80Bh,80Fh



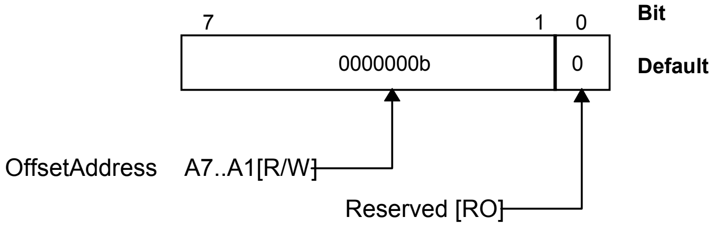
	Window 0	*Window 1*
Offset	80Bh	80Fh

Bit	Field Name	Description
7-0	StopAddress A15..A8	I/O Window 0-1 Stop Address A15..A8:

7.6.6 Card I/O Offset Address 0-1 Low Byte register

These two registers contain the lower offset address bits that are added to system address bits A [7:1] to generate the PC Card-16 I/O address for I/O address windows 0 and 1.

Register Name: Card I/O Offset Address 0-1 Low Byte
Address Offset: 836h,838h



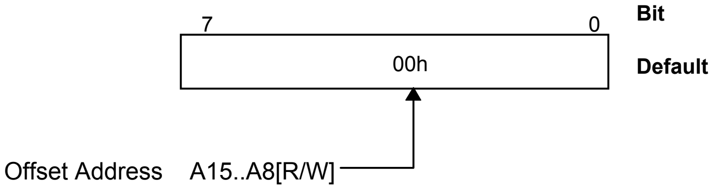
	Window 0	*Window 1*
Offset	836h	838h

Bit	Field Name	Description
7-1	Offset Address A7..A1	I/O Window 0-1 Card I/O Offset Address A7..A1:
0	Reserved	This bit is reserved and returns zero when read.

7.6.7 Card I/O Offset Address 0-1 High Byte register

These two registers contain the upper offset address bits that are added to the system address bits A [15:8] to generate the PC Card-16 I/O address for I/O address windows 0 and 1.

Register Name: Card I/O Offset Address 0-1 High Byte
Address Offset: 837h,839h



	Window 0	*Window 1*
Offset	837h	839h

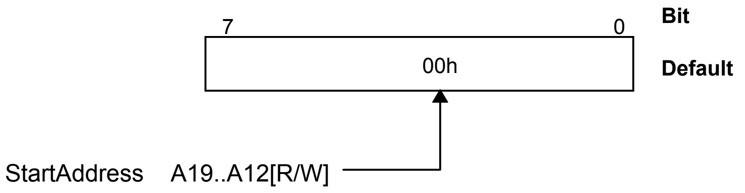
Bit	Field Name	Description
7-0	OffsetAddress A15..A8	I/O Window 0-1Offset Address A15..A8:

7.7 Memory Window Control Registers

7.7.1 System Memory Address 0-4 Mapping Start Low Byte register

These five registers contain the lower address bits that indicate the start address of the system memory address mapping windows 0,1,2,3 and 4. The register's contents correspond to PCI memory address bits A [19:12], and are used to determine whether memory accesses are valid. Therefore mapping of each system memory can start and stop on any 4Kbyte boundary of the system memory.

Register Name: System Memory Address 0-4 Mapping Start Low Byte
Address Offset: 810h,818h,820h,828h,830h



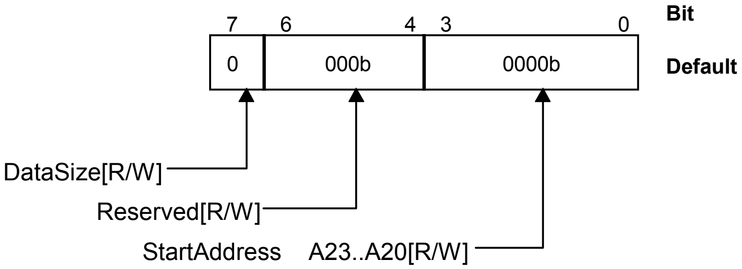
	Window0	*Window1*	*Window2*	*Window3*	*Window4*
Offset	810h	818h	820h	828h	830h

Bit	Field Name	Description
7-0	StartAddress A19..A12	System Memory Address Mapping Window 0-4 Start Address A19 .. A12:

7.7.2 System Memory Address 0-4 Mapping Start High Byte register

These five registers contain the upper address bits that indicate the start address of the system memory address mapping windows 0,1,2,3 and 4. The register's contents correspond to PCI memory address bits A [23:20], and are used to determine whether memory accesses are valid. And also, bits of corresponding register control the data path size for each window.

Register Name: System Memory Address 0-4 Mapping Start High Byte
Address Offset: 811h,819h,821h,829h,831h



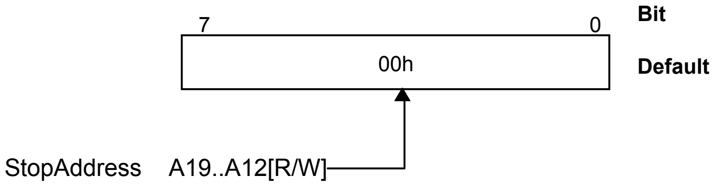
	Window0	*Window1*	*Window2*	*Window3*	*Window4*
Offset	811h	819h	821h	829h	831h

Bit	Field Name	Description
7	DataSize	This bit selects the memory data path size to the PC Card-16. When this bit is set to 1, 16-bit data path is selected. When this bit is set to 0, 8-bit data path is selected. This bit has priority over the PCI command.
6-4	Reserved(R/W)	This read/write bit field is reserved.
3-0	StartAddress A23..A20	System Memory Address Mapping Window 0-4 Start Address A23 .. A20:

7.7.3 System Memory Address 0-4 Mapping Stop Low Byte register

These five registers contain the lower address bits that indicate the stop address of the corresponding system memory address mapping windows 0,1,2,3 and 4. The register's contents correspond to PCI memory address bits A [19:12], and are used to determine whether memory accesses are valid.

Register Name: System Memory Address 0-4 Mapping Stop Low Byte
Address Offset: 812h,81Ah,822h,82Ah,832h



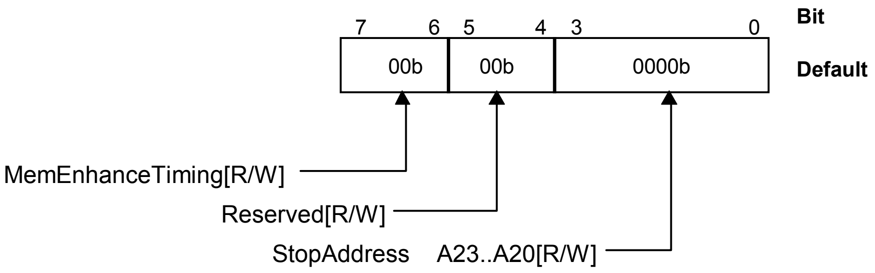
	Window0	***Window1***	***Window2***	***Window3***	***Window4***
Offset	812h	81Ah	822h	82Ah	832h

Bit	**Field Name**	**Description**
7-0	StopAddress A19..A12	System Memory Address Mapping Window 0-4 Stopt Address A19 .. A12:

7.7.4 System Memory Address 0-4 Mapping Stop High Byte register

These five registers contain the upper address bits that indicate the stop address of the corresponding system memory address mapping windows 0,1,2,3 and 4. The register's contents correspond to PCI memory address bits A [23:20], and are used to determine whether memory accesses are valid. Two bits in each of the registers select the PC Card-16 access timing for the corresponding system memory window.

Register Name: System Memory Address 0-4 Mapping Stop High Byte
Address Offset: 813h,81Bh,823h,82Bh,833h



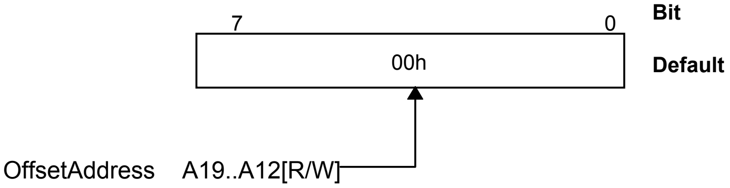
	Window0	Window1	Window2	Window3	Window4
Offset	813h	81Bh	823h	82Bh	833h

Bit	Field Name	Description
7-6	MemEnhanceTiming	Timing parameters for memory PC Card-16 are independently configured for each Common Memory Window by programming these timing bits. The default timing mode is 00b, and only the default timing is used for Attribute memory. User defined timing is valid when 16-bit Memory Enhance Timing bit in the 16-bit Interface Control register is set to 1 regardless of this bit being set to 0. 00b = Default Timing 01b = Enhance Timing 10b = Enhance Timing 11b = Enhance Timing
5-4	Reserved(R/W)	This read/write bit field is reserved.
3-0	StopAddress A23..A20	System Memory Address Mapping Window 0-4 Stop Address A23 .. A20:

7.7.5 Card Memory Offset Address 0-4 Low Byte register

These five registers contain the lower offset address bits that are added to system address bits A [19:12] to generate the PC Card-16 memory address for memory windows 0,1,2,3 and 4.

Register Name: Card Memory Offset Address 0-4 Low Byte
Address Offset: 814h,81Ch,824h,82Ch,834h



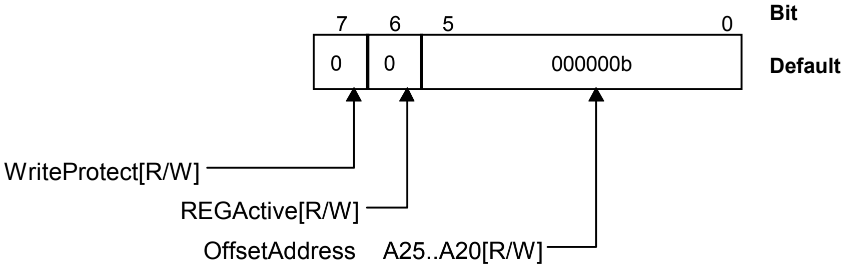
	Window0	*Window1*	*Window2*	*Window3*	*Window4*
Offset	814h	81Ch	824h	82Ch	834h

Bit	Field Name	Description
7-0	OffsetAddress A19..A12	Card Memory Offset Address A19 .. A12:

7.7.6 Card Memory Offset Address 0-4 High Byte register

These five registers contain the upper offset address bits that are added to system address bits A [23:20] to generate the PC Card-16 memory address for memory windows 0,1,2,3 and 4. These register also control PC Card-16 memory software write protect for the corresponding system memory windows, and select whether the memory windows are mapped to attribute memory, or to common memory on the PC Card-16.

Register Name: Card Memory Offset Address 0-4 High Byte
Address Offset: 815h,81Dh,825h,82Dh,835h (8 bit)



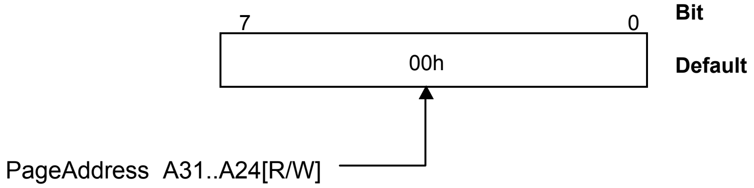
	Window0	*Window1*	*Window2*	*Window3*	*Window4*
Offset	815h	81Dh	825h	82Dh	835h

Bit	Field Name	Description
7	WriteProtect (WP)	When this bit is set to 1, write transactions to the PC Card-16 through the corresponding system memory window are inhibited. When this bit is set to 0, write transactions are allowed. The WP switch on the memory card sets the Memory Write Protect bit in the Interface Status register, but setting it can block the memory write cycles.
6	REGActive	When this bit is set to 1, accesses to the system memory window are changed over accesses to the attribute memory on the PC Card by asserting REG# "low". When this bit is set to 0, accesses to the system memory window are changed over accesses to the common memory on the PC Card by asserting REG# "high".
5-0	OffsetAddress A25..A20	Card Memory Offset Address A25 .. A20:

7.7.7 System Memory Page Address 0-4 register

This register contains an 8-bit page address that allows selection of a 16 Mbyte window page in the 4 Gbyte memory address space in which socket memory window is mapped. Access to a window is allowed only when the page address in the corresponding Card Memory Page Address register matches PCI memory address bits A [31:24], indicating a page hit. Reset clears all bits in this register, so that the default page is the first page (i.e., 0-16 Mbyte address range). This register cannot be accessed through I/O address 3E0h/3E2h ports.

Register Name:	System Memory Page Address 0-4
Address Offset:	840h, 841h, 842h, 843h, 844h (8bit)



	Window0	Window1	Window2	Window3	Window4
Offset	840h	841h	842h	843h	844h

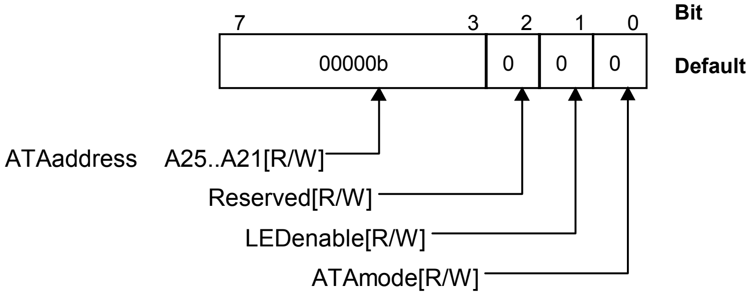
Bit	Field Name	Description
7-0	PageAddress A31..A24	System Memory Page Address A31 .. A24:

7.8 Special Function Registers

7.8.1 ATA Control register

This register contains the information that is used for PCMCIA-ATA mode.

Register Name: ATA Control
Address Offset: 81Fh (8 bit)

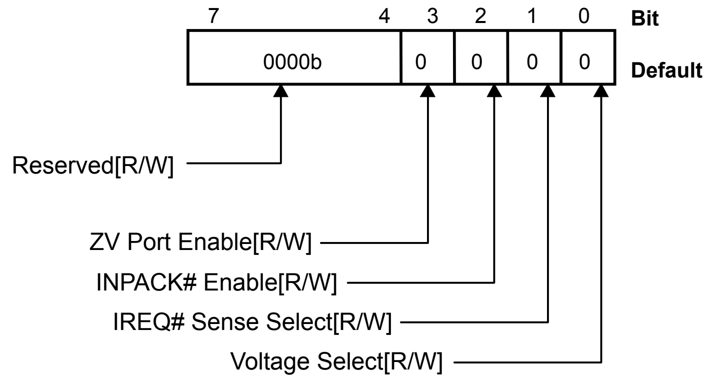

7
3
2
1
0
Bit
00000b
0
0
0
Default
ATAaddress A25..A21[R/W]
Reserved[R/W]
LEDenable[R/W]
ATAmode[R/W]

Bit	**Field Name**	**Description**
7-3	ATAaddressA25..A21	This field contains the card address 25-21 in PCMCIA-ATA mode. This field has no effect excepting this meaning.
2	Reserved(R/W)	This read/write bit is reserved.
1	LEDenable	When this bit is set to1, IRQ12 becomes open drain output suitable for driving an LED (driven whenever the card-SPKR output is turned on, and corresponding SPKR# is LED input bit is set). This bit works independent of Bit 0 (ATA mode).
0	ATAmode	When this bit is set to 1, PCMCIA-ATA mode is selected.

7.8.2 Misc Control 1 register

This register controls the miscellaneous signals like INPCK# and IREQ# for the PC Card-16.

Register Name: Miscellaneous Control 1
Address Offset: 82Fh (8 bit)

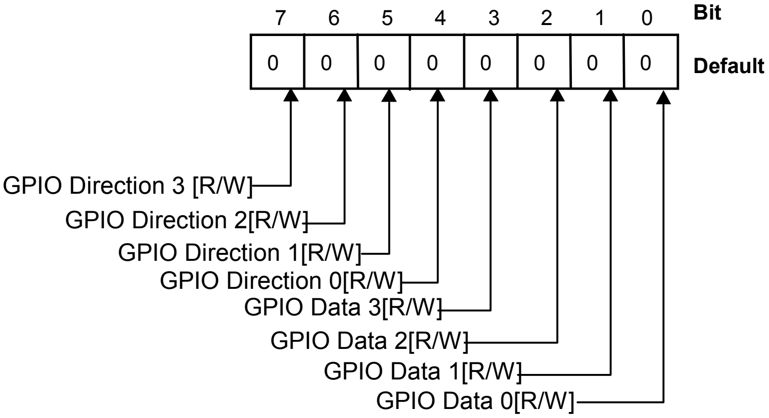


Bit	Field Name	Description
7-4	Reserved(R/W)	This read/write bit is reserved for future use.
3	ZV Port Enable	When this bit is set to 1, the PC Card-16 interface is Zoomed Video Port mode. Therefore, the card address lines CADR [25:4] are put in tri-state, and then replaced by Zoomed Video Port signals, with BVD2/SPKR# and INPACK#, which carry video/audio data from the PC Card-16 to the ZV port. The default is zero.
2	INPACK# Enable	When this bit is set to 1, the INPACK# signal is enabled on the PC Card-16 interface. The R5C485 returns ones on I/O read unless INPACK# is asserted, and ends normally. When this bit is set to 0, the INPACK# signal is disabled.
1	IREQ Sense Select	When this bit is set to 1, the IREQ# signal is “high” active. When this bit is set to 0, the IREQ# signal is “low” active.
0	Voltage Select	This bit is used with Bit4-0 in the Power Control register in order to control the Socket voltage. The setting is described in Power Control Register section.

7.8.3 General Purpose I/O register

The R5C485 assigns IRQ [3,4,5,7] pins to GPIO (General Purpose I/O) pins when Serialized IRQ mode is selected and the Misc Control 4 register is set. User can be free to use these I/O pins. When GPIO Enale bit is set to one, setting of GPIO is Input mode (default). And Bit [3:0] indicates the state of mode. In Output mode, GPIO [3:0] output the contents written in each bit. This register linking to the General Purpose I/O 1 register reflects the General Purpose I/O 1 register (AAh). On the other hand, the General Purpose I/O 1 register also reflects this register.

Register Name: General Purpose I/O
Address Offset: 83Ah (8 bit)



Bit	Field Name	Description
7	GPIO Direction 3	GPIO Data 3 I/O change signal. When this bit is set to 0, GPIO Data 3 is input. When this bit is set to 1, CPIO Data 3 is output. The default is zero.
6	GPIO Direction 2	GPIO Data 2 I/O change signal. When this bit is set to 0, GPIO Data 2 is input. When this bit is set to 1, CPIO Data 2 is output. The default is zero.
5	GPIO Direction 1	GPIO Data 1 I/O change signal. When this bit is set to 0, GPIO Data 1 is input. When this bit is set to 1, CPIO Data 1 is output. The default is zero.
4	GPIO Direction 0	GPIO Data 0 I/O change signal. When this bit is set to 0, GPIO Data 0 is input. When this bit is set to 1, CPIO Data 0 is output. The default is zero.
3	GPIO Data 3	General Purpose I/O bit 3. The default is input.
2	GPIO Data 2	General Purpose I/O bit 2. The default is input.
1	GPIO Data 1	General Purpose I/O bit 1. The default is input.
0	GPIO Data 0	General Purpose I/O bit 0. The default is input.

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Rating

Symbol	Parameter	Min	Unit	Condition	Note
Vcc 1	Supply Voltage Range 1	-0.3 ~ 3.6	V	GND=0V	1
Vcc 2	Supply Voltage Range 2	-0.3 ~ 4.6	V	GND=0V	2
Vte	Voltage on Any Pin	-0.3 ~ 5.8	V	GND=0V	
Topr	Ambient Temperature under bias	-40 ~ 85	°C		
Tstg	Storage Temperature Range	-55 ~ 125	°C		
ESD1	Human Body Model	±2.0	KV	C=100pF R=1.5KΩ	
ESD2	Charged Device Model	±1.0	KV		
LATUP	Latch-up	±100	mA	5ms	3

Note 1: Applied for VCC_CORE18.
Note 2: Applied for VCC_3V and VCC_PCI3V.
Note 3: The clamping voltage of the trigger pulse power source should be below a value of Vte.

Note: Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

8.2 DC Characteristics

8.2.1 Recommended Operating Conditions for Power Supply

Power Pin	Parameter	Min	Typ	Max	Unit	Note
VCC_PCI3V	Supply Voltage for PCI interface (3.3V Operation)	3.0	3.3	3.6	V	
VCC_CORE18V	Supply Voltage for Core Logic (1.8V Operation)	1.65	1.8	1.95	V	
VCC_CORE18V	Supply Voltage for Core Logic (2.5V Operation)	2.3	2.5	2.7	V	
VCC_3V	Supply Voltage for System interface and Card Socket Signals	3.0	3.3	3.6	V	

8.2.2 PCI Interface

For 3.3V signaling
(VCC_CORE18V=1.65~1.95V or 2.3~2.7V, VCC_PCI3V=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
VIH	Input High Voltage	0.5VCC_PCI3V	5.75	V		1
VIL	Input Low Voltage	-0.5	0.3VCC_PCI3V	V		1
VOH	Output High Voltage	0.9VCC_PCI3V		V	Iout=-500μA	1
VOL	Output Low Voltage		0.1VCC_PCI3V	V	Iout=1500μA	1
IILk	Input Leakage Current		±10	μA	Vin=0~VCC_ PCI3V	1
Cin	Input Pin Capacitance		10	pF		1
Cclk	PCICLK Pin Capacitance		12	pF		1

Note 1: Applied for PCICLK, CLKRUN#, PCIRST#, AD [31:0], C/BE#[3:0], PAR, FRAME#,
IRDY#, TRDY#,STOP#, DEVSEL#, IDSEL, PERR#, SERR#, REQ#, GNT#,
INTA# pins

8.2.3 16-bit PC Card Interface

For 3.3V signaling
(VCC_CORE18V=1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition	Note
VIH	Input High Voltage	2.0		5.5	V		2
VIL	Input Low Voltage	-0.3		0.6	V		2
VOH1	Output High Voltage	2.4			V	Iout=-4mA	2
VOH2	Output High Voltage	2.4			V	Iout=-2mA	3
VOL1	Output Low Voltage			0.4	V	Iout=4mA	2
VOL2	Output Low Voltage			0.4	V	Iout=2mA	3
IILk	Input Leakage Current			±10	μA	Vin=0~VCC_3V	2
IIL1	Input Leakage Current (Pull-up)		-50		μA	Vin=0	4
Cin	Input Pin Capacitance			10	pF		2

Note 2: Applied for CADR [25:0], CDATA [15:0], CE [2:1]#, IOR#, IOW#, OE#, WE#, REG#,
RDY/IREQ#, WAIT#, WP/IOIS16#, BVD1/STSCHG#/RI#,
BVD2/SPKR#, INPACK# pins,
if Card interface is configured as a 16-bit Card Socket.
Note 3: Applied for RESET pin
Note 4: Applied for RDY/IREQ#, WAIT#, BVD1/STSCHG#/RI#, BVD2/SPKR#, INPACK# pins

8.2.4 CardBus PC Card Interface

(VCC_CORE18V=1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition	Note
VIH	Input High Voltage	0.475x VCC_3V		VCC_3V +0.5	V		6
VIL	Input Low Voltage	-0.5		0.325xVCC_3V	V		6
VOH	Output High Voltage	0.9xVCC_3V			V	Iout=-150µA	6
VOL	Output Low Voltage			0.1xVCC_3V	V	Iout=700µA	6
IILk	Input Leakage Current			±10	µA	Vin=0~VCC_3V	6
IIL1	Input Leakage Current (Pull-up)		-230		µA	Vin=0	7
Cin	Input Pin Capacitance			10	pF		6
IIL2	Input Leakage Current (Pull-down)		16.5		µA	Vin=VCC_3V	8
IIL3	Input Leakage Current (Pull-up)		-70		µA	Vin=0	9

Note 6: Applied for CCLK, CCLKRUN#, CRST#, CAD [31:0], CC/BE#[3:0], CPAR, CFRAME#, CIRDY#,CTRDY#,CSTOP#, CDEVSEL#, CPERR#, CSERR#, CREQ#, CGNT#, CINT#, CAUDIO, CSTSCHG pins, if Card interface is configured as a CardBus Card Socket.

Note 7: Applied for CIRDY#, CTRDY#, CSTOP#, CDEVSEL#, CPERR#, CSERR#, CREQ#, CINT#, CAUDIO pins

Note 8: Applied for CSTSCHG pin

Note 9: Applied for CCLKRUN# pin

8.2.5 PC Card Interface Card detect Pins and System Interface Pins

PC Card Interface Card Detect Pins and System Interface Pins
(VCC_CORE18V=1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition	Note
VIH1	Input High Voltage	0.8x VCC_3V		VCC_3V+0.3	V		10
VIL1	Input Low Voltage	-0.3		0.3xVCC_3V	V		10
VIH2	Input High Voltage	2.4		VCC_3V+0.3	V		12
VIL2	Input Low Voltage	-0.3		0.8	V		12
VIH3	Input High Voltage	2.4		5.75	V		13
VIL3	Input Low Voltage	-0.3		0.8	V		13
VOH1	Output High Voltage	2.4			V	Iout=-4mA	11
VOH2	Output High Voltage	2.4			V	Iout=-1mA	12
VOL1	Output Low Voltage			0.4	V	Iout=4mA	11
VOL2	Output Low Voltage			0.4	V	Iout=1mA	12
IILk	Input Leakage Current			±10	µA	Vin=0~VCC_3V	12
IIL1	Input Leakage Current (Pull-up)		-80		µA	Vin=0	10
IOZ	Hi-Z Output Leakage Current			±10	µA	Vout=0~VCC_3 V	11

Note 10: Applied for CD1#(CCD1#), CD2#(CCD2#) pins
Note 11: Applied for RI_OUT#, SPKROUT#,VCC5EN#, VCC3EN#, VPPEN0, VPPEN1 pins
Note 12: Applied for VS1#(CVS1#), VS2#(CVS2#) pins
Note 13: Applied for GBRST#, HWSPND# pins

8.2.6 IRQ3-15 pin

(VCC_CORE18V=1.65~1.95V or 2.3~2.7V, VCC_PCI3V=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
VOH	Output High Voltage	2.4		V	Iout=-4mA	14
VOL	Output Low Voltage		0.4	V	Iout=4mA	14
IOZ	Hi-Z Output Leakage Current		±10	µA	Vout=0~VCC_3V	14
VIH	Input High Voltage	0.5VCC_3V	5.75	V		15
VIL	Input Low Voltage	-0.5	0.3VCC_3V	V		15
IILK	Input Leakage Current		±10	µA	Vin=0~VCC_3V	15

Note 14: Applied for IRQ3-15 pins

Note 15: Applied for IRQ3-9 pins.

8.2.7 Power Consumption

Power Supply Current

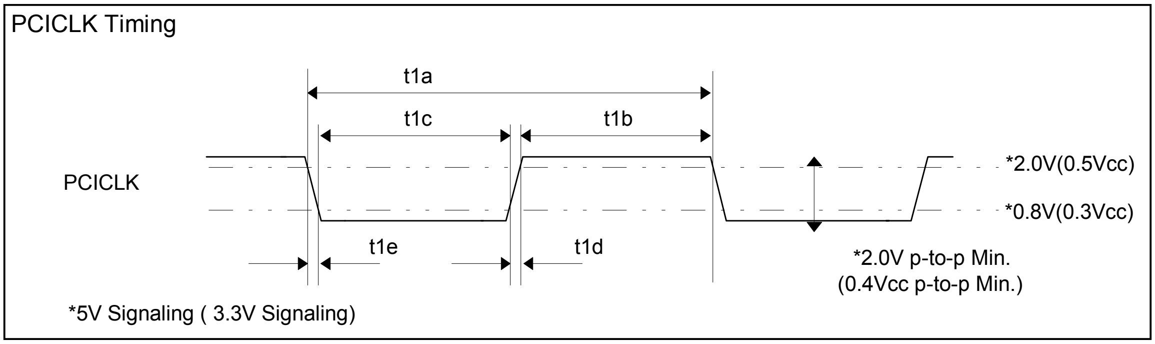
Power Pin	Parameter	Min	Typ	Max	Unit	Condition
Iccstd	Power Supply Current, Standby			150	μA	fclk (PCICLK)=0, Vin=0or Vcc
Iccsusp	Power Supply Current, Hardware Suspend Mode			150	μA	Mode = H/W BridgeSuspend VCC_3V=3.6V VCC_PCI3V=0V VCC_CORE18V=2.7V Vin=0 or Vcc
Icc	Power Supply Current, Operating			22	mA	fclk (PCICLK)=33Mhz VCC_3V=3.6V VCC_PCI3V=3.6V VCC_CORE18V=1.95V Vin=0 or Vcc

8.3 AC Characteristics

8.3.1 PCI Interface

PCI Clock
(VCC_CORE18V=1.65~1.95V or 2.3~2.7V, VCC_PCI3V=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	PCICLK				
t1a	Cycle Time, PCICLK	30		ns	
t1b	Pulse Width Duration, PCICLK High	11		ns	
t1c	Pulse Width Duration, PCICLK Low	11		ns	
t1d	Slew Rate, PCICLK Rising Edge	1	4	V/ns	
t1e	Slew Rate, PCICLK Falling Edge	1	4	V/ns	

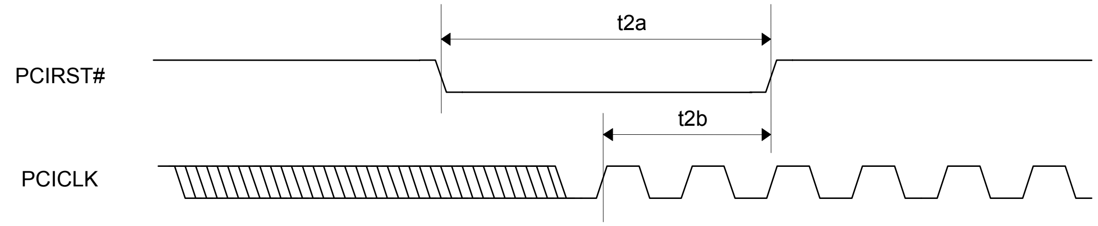

PCICLK Timing
t1a
t1c
t1b
PCICLK
*2.0V(0.5Vcc)
*0.8V(0.3Vcc)
t1e
t1d
*2.0V p-to-p Min.
(0.4Vcc p-to-p Min.)
*5V Signaling (3.3V Signaling)

PCICLK Timing

PCI Reset
(VCC_CORE18V=1.65~1.95V or 2.3~2.7V, VCC_PCI3V=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	PCIRST#				
t2a	Pulse Duration, PCIRST#	1		ms	
t2b	Setup Time,PCICLK active at PCIRST# Negation	100		µs	

PCI Reset Timing

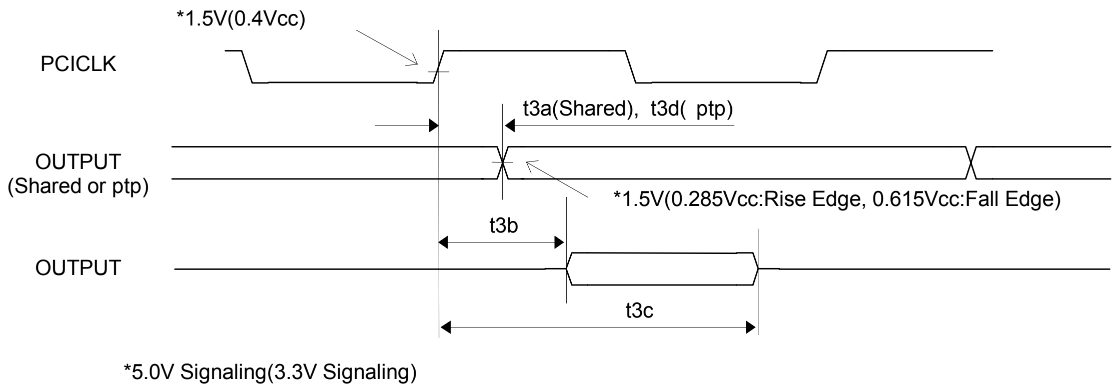

t2a
PCIRST#
t2b
PCICLK

PCI Reset Timing

PCI Interface Output Signals
(VCC_CORE18V=1.65~1.95V or 2.3~2.7V, VCC_PCI3V=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	AD [31:0], C/BE#[3:0], PAR, FRAME#,DEVSEL#, IRDY#, TRDY#,STOP#, PERR#, SERR#, CLKRUN#				
t3a	Shared Signal Valid delay time from PCICLK	2	11	ns	Min: CL=0 pF Max: CL=50 pF (10 pF 3.3v)
t3b	Enable Time, Hi-Z to active delay from PCICLK	2		ns	
t3c	Disable Time, Active to Hi-Z delay from PCICLK		28	ns	
	REQ#				
t3d	Point to Point Signal Valid delay time from PCICLK	2	12	ns	Min: CL=0 pF Max: CL=50 pF (10 pF 3.3v)

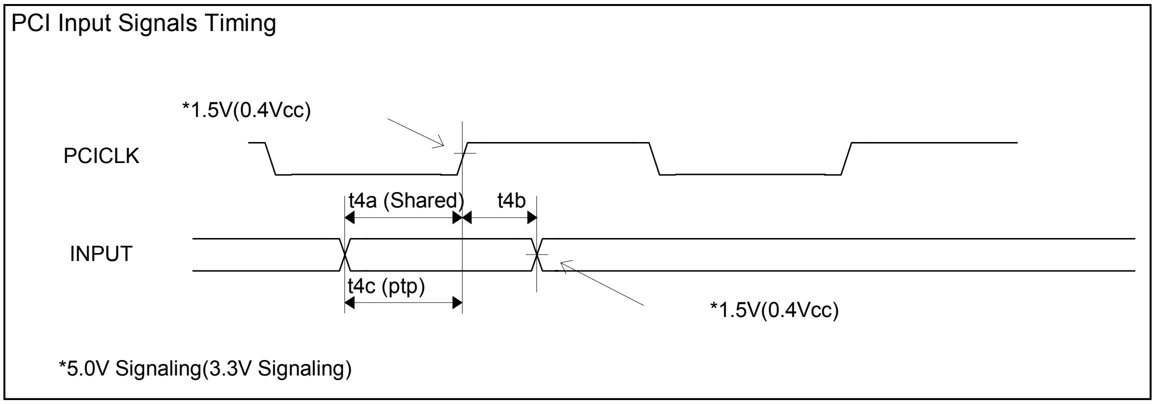
PCI Output Signals Timing


*1.5V(0.4Vcc)
PCICLK
t3a(Shared), t3d(ptp)
OUTPUT
(Shared or ptp)
*1.5V(0.285Vcc:Rise Edge, 0.615Vcc:Fall Edge)
t3b
OUTPUT
t3c
*5.0V Signaling(3.3V Signaling)

PCI Output Signals Timing

PCI Interface Input Signals (VCC_CORE18V=1.65~1.95V or 2.3~2.7V, VCC_PCI=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	CAD [31:0], C/BE#[3:0], PAR, FRAME#,DEVSEL#, IRDY#, TRDY#,STOP#, IDSEL, PERR#, SERR#, CLKRUN#				
t4a	Setup Time, Shared Signal Valid before PCICLK	7		ns	
t4b	Hold Time, Shared Signal Hold Time after PCICLK High	0		ns	
	GNT#				
t4c	Setup Time, Point to Point Signal Valid before PCICLK	10		ns	


PCI Input Signals Timing
*1.5V(0.4Vcc)
PCICLK
t4a (Shared)
t4b
INPUT
t4c (ptp)
*1.5V(0.4Vcc)
*5.0V Signaling(3.3V Signaling)

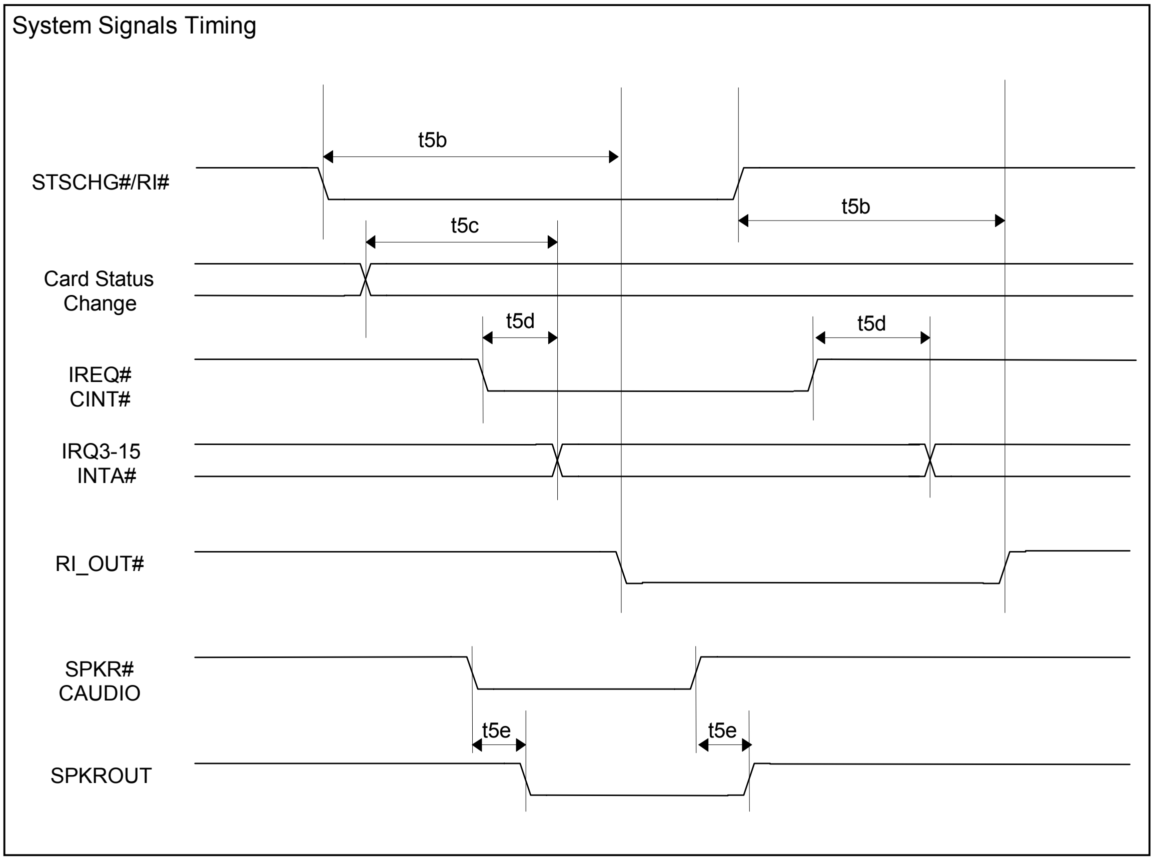
PCI Input Signals Timing

8.3.2 System Interface

System Interface Signals AC Characteristics
(VCC_CORE18V=1.65~1.95V or 2.3~2.7V, VCC_PCI3V=3.0~3.6V, VCC_3V=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	RI_OUT#, IRQ3-15, INTA#				
t5b	RI# to RI_OUT# Delay		50	ns	
t5c	Card Status Change to IRQ3-15/INTA# Delay		2Tcyc+0	ns	1
t5d	Card IREQ#/CINT# to IRQ3-15/INTA# Delay		50	ns	
	SPKROUT				
t5e	SPKR#/CAUDIO to SPKROUT Delay		50	ns	

Note1: Tcyc is PCICLK cycle time. (Typically 30ns)


System Signals Timing
t5b
STSCHG#/RI#
t5b
t5c
Card Status Change
t5d
t5d
IREQ#
CINT#
IRQ3-15
INTA#
RI_OUT#
SPKR#
CAUDIO
t5e
t5e
SPKROUT

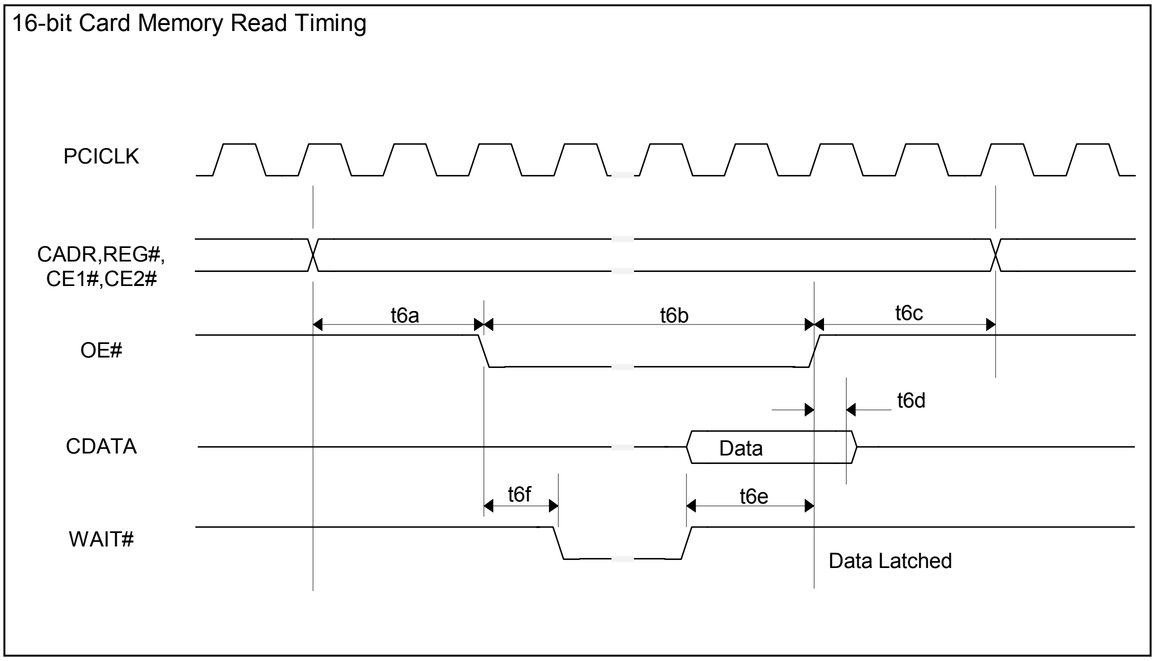
System Signals Timing

8.3.3 16-bit PC Card Interface

Memory Read
(VCC_CORE18V=1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	CADR [25:0], REG#, CE [2:1]#				
t6a	Setup Time, CADR [25:0], REG# and CE [2:1]# before OE# Low	Tsu-20		ns	1,2 Tsu=1~7Tcyc Programmable
t6c	Hold Time, CADR [25:0], REG# and CE [2:1]# after OE# High	Thl-10		ns	1,2 Thl=1~7Tcyc Programmable
	OE#				
t6b	Pulse Duration, OE# Low	Tpw-20		ns	1,2 Tpw=3~31Tcyc Programmable
	CDATA [15:0]				
t6d	Hold Time, CDATA [15:0] after OE# High	0		ns	
	WAIT#				
t6e	Hold Time, OE# Low after WAIT# High	1Tcyc+0		ns	1
t6f	Valid Delay, OE# Low to WAIT# Low		50	ns	

Note1: Tcyc is PCICLK cycle time. (Typically 30ns)
Note2: Tsu, Tpw, Thl can be programmed by setting 16-bit Memory Timing 0 register.


16-bit Card Memory Read Timing
PCICLK
CADR,REG#,
CE1#,CE2#
OE#
CDATA
WAIT#
t6a
t6b
t6c
t6d
Data
t6f
t6e
Data Latched

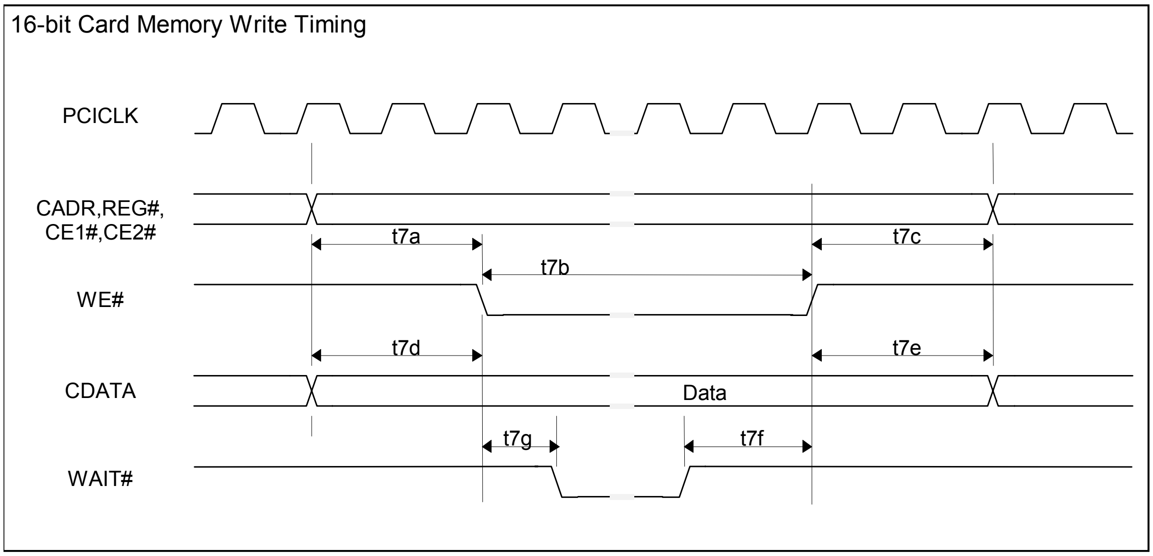
16-bit Card Memory Read Timing

Memory Write
(VCC_CORE18V=1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	CADR [25:0], REG#, CE [2:1]#				
t7a	Setup Time, CADR [25:0], REG# and CE [2:1]# before WE# Low	Tsu-20		ns	1,2 Tsu=1~7Tcyc Programmable
t7c	Hold Time, CADR [25:0], REG# and CE [2:1]# after WE# High	Thl-10		ns	1,2 Thl=1~7Tcyc Programmable
	WE#				
t7b	Pulse Duration, WE# Low	Tpw-20		ns	1,2 Tpw=3~31Tcyc Programmable
	CDATA [15:0]				
t7d	Setup Time, CDATA [15:0] before WE# Low	Tsu-20		ns	1,2 Tsu=1~7Tcyc Programmable
t7e	Hold Time, CDATA [15:0] after WE# High	Thl-10		ns	1,2 Thl=1~7Tcyc Programmable
	WAIT#				
t7f	Hold Time, WE# Low after WAIT# High	Tcyc+0		ns	1
t7g	Valid Delay, WE# Low to WAIT# Low		50	ns	

Note1: Tcyc is PCICLK cycle time. (Typically 30ns)

Note2: Tsu, Tpw, Thl can be programmed by setting 16-bit Memory Timing 0 register.


16-bit Card Memory Write Timing
PCICLK
CADR,REG#,
CE1#,CE2#
t7a
t7c
t7b
WE#
t7d
t7e
CDATA
Data
t7g
t7f
WAIT#

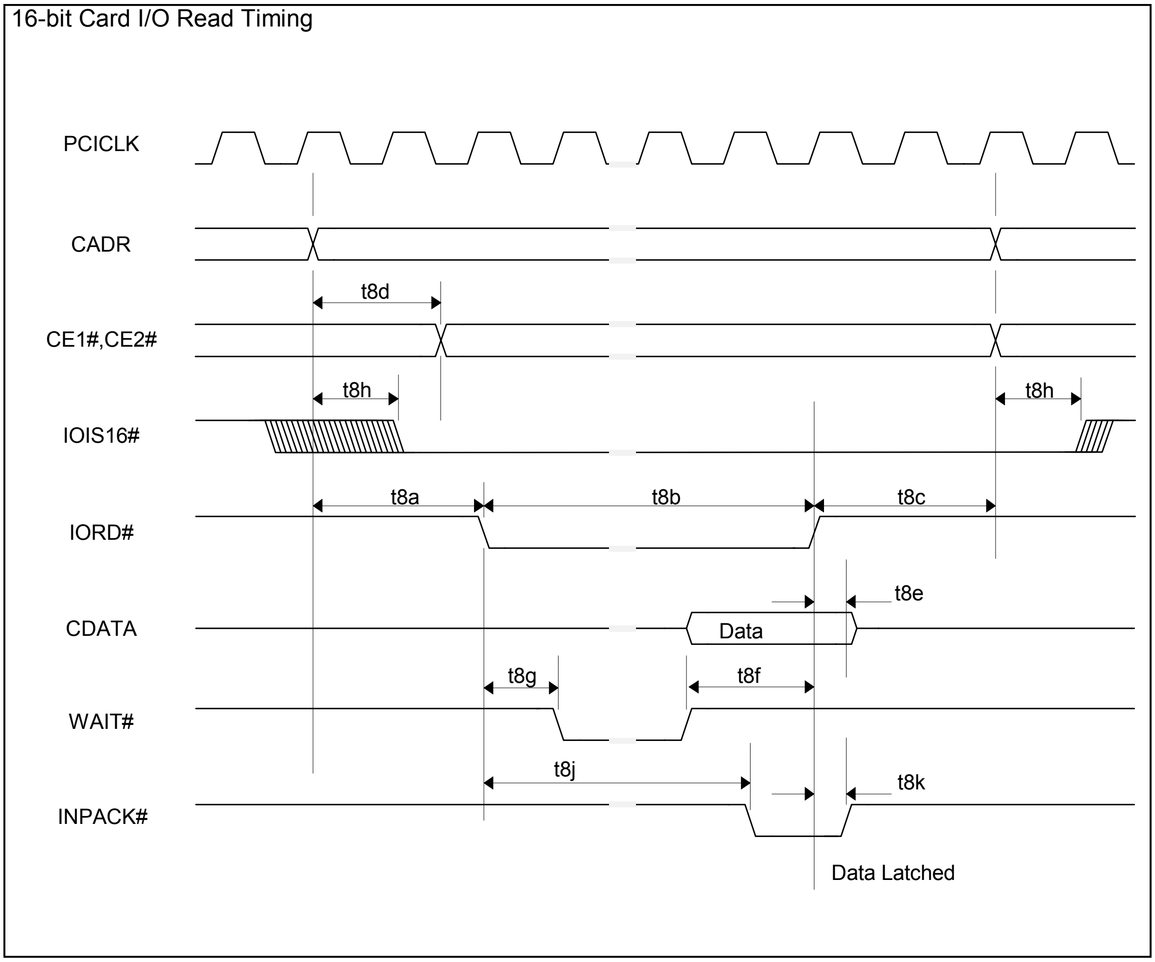
16-bit Card Memory Write Timing

I/O Read
(VCC_CORE18V=1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	CADR [25:0], REG#				
t8a	Setup Time, CADR [25:0] and REG# before IORD# Low	Tsu-20		ns	1,3 Tsu=2~7Tcyc Programmable
t8c	Hold Time, CADR [25:0] and REG# after IORD # High	Thl-10		ns	1,3 Thl=1~7Tcyc Programmable
	IORD#				
t8b	Pulse Duration, IORD # Low	Tpw-20		ns	1,3 Tpw=3~31Tcyc Programmable
	CE [2:1]#				
t8d	Valid Delay, CADR [15:0] and REG# to CE [2:1]#	1Tcyc-10		ns	1
	CDATA [15:0]				
t8e	Hold Time, CDATA [15:0] after IORD # High	0		ns	
	WAIT#				
t8f	Hold Time, IORD # Low after WAIT# High	1Tcyc+0		ns	1
t8g	Valid Delay, IORD # Low to WAIT# Low		50	ns	
	IOIS16#				
t8h	Valid Delay, CADR [25:0] to IOIS16# Low		50	ns	
	INPACK#				
t8k	Hold Time, INPCK# Low afterIORD# High	0		ns	
t8j	Valid Delay, IORD # Low to INPACK# Low		50	ns	

Note1: Tcyc is PCICLK cycle time. (Typically 30ns)

Note3: Tsu, Tpw, Thl can be programmed by setting 16-bit I/O Timing 0 register.


16-bit Card I/O Read Timing
PCICLK
CADR
t8d
CE1#,CE2#
t8h
t8h
IOIS16#
t8a
t8b
t8c
IORD#
t8e
CDATA
Data
t8g
t8f
WAIT#
t8j
t8k
INPACK#
Data Latched

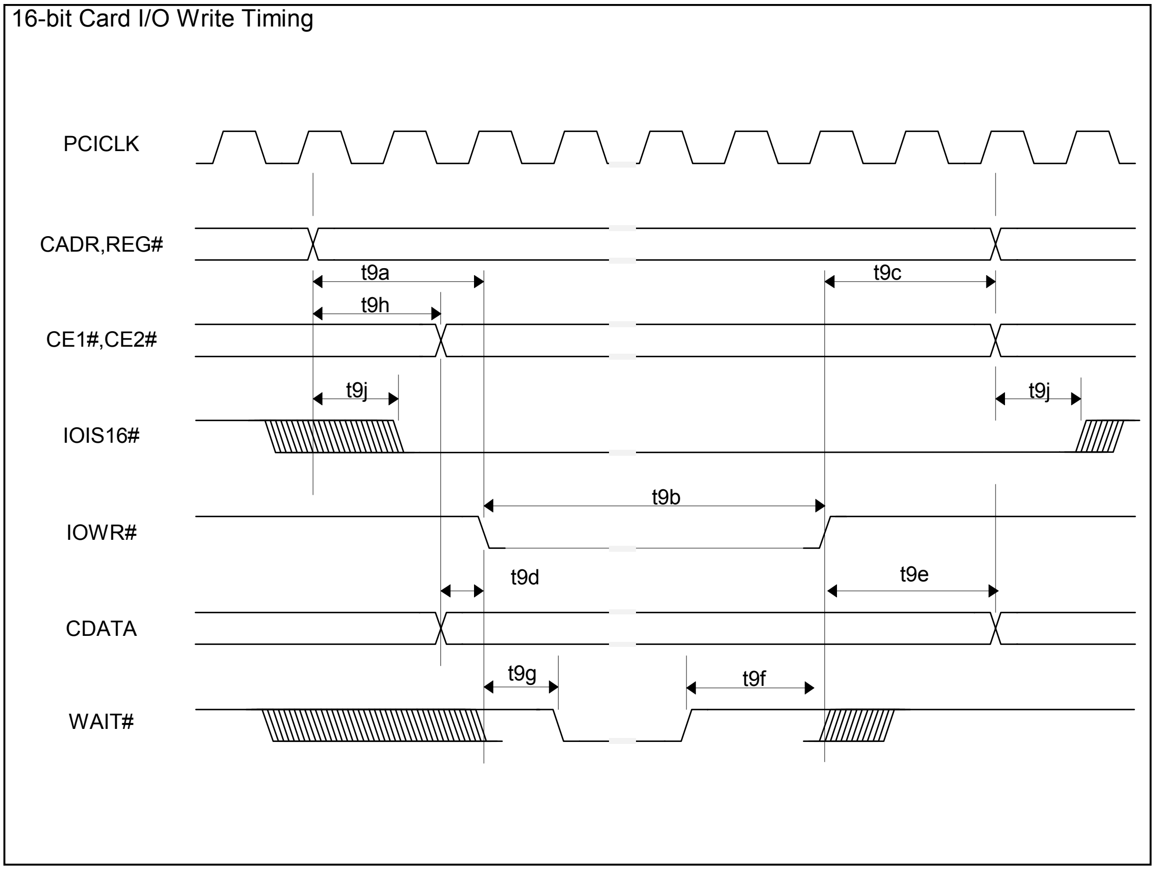
16-bit Card I/O Read Timing

I/O Write
(VCC_CORE18V=1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	CADR [25:0], REG#				
t9a	Setup Time, CADR [25:0] and REG# before IOWR # Low	Tsu-20		ns	1,3 Tsu=2~7Tcyc Programmable
t9c	Hold Time, CADR [25:0], REG# and CE [2:1]# after IOWR # High	Thl-10		ns	1,3 Thl=1~7Tcyc Programmable
	IOWR#				
t9b	Pulse Duration, IOWR# Low	Tpw-20		ns	1,3 Tpw=3~31Tcyc Programmable
	CE [2:1]#				
t9h	Valid Delay, CADR [15:0] and REG# to CE [2:1]#	1Tcyc-10		ns	1
	CDATA [15:0]				
t9d	Setup Time, CDATA [15:0] before IOWR # Low	Tsu-2Tcyc-10		ns	1,3 Tsu=3~7Tcyc Programmable
t9e	Hold Time, CDATA [15:0] after IOWR # High	Thl-10		ns	1,3 Thl=1~7Tcyc Programmable
	WAIT#				
t9f	Hold Time, IOWR # Low after WAIT# High	1Tcyc+0		ns	3
t9g	Valid Delay, IOWR # Low to WAIT# Low		50	ns	
	IOIS16#				
t9j	Valid Delay, CADR [25:0] and REG# to IOIS16# Low		50	ns	

Note1: Tcyc is PCICLK cycle time. (Typically 30ns)

Note3: Tsu, Tpw, Thl can be programmed by setting 16-bit I/O Timing 0 register.


16-bit Card I/O Write Timing
PCICLK
CADR,REG#
t9a
t9c
t9h
CE1#,CE2#
t9j
t9j
IOIS16#
t9b
IOWR#
t9d
t9e
CDATA
t9g
t9f
WAIT#

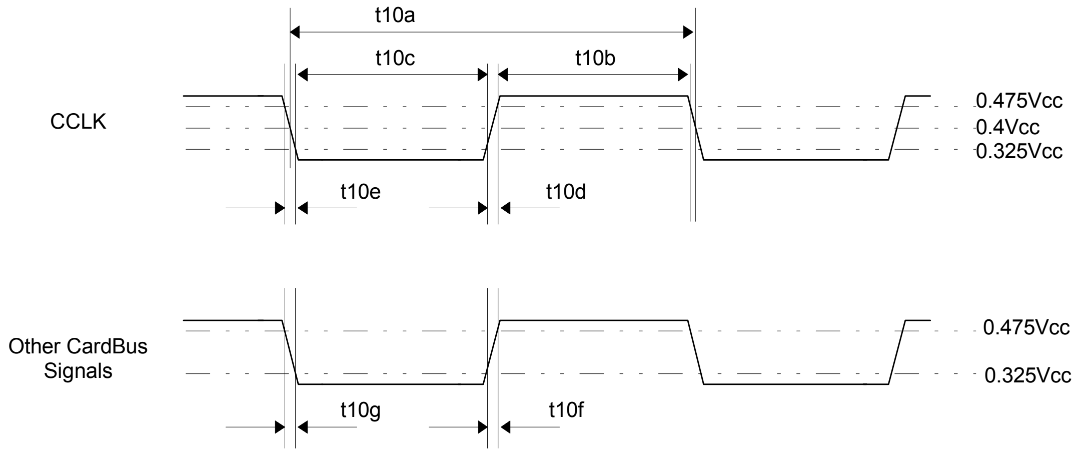
16-bit Card I/O Write Timing

8.3.4 CardBus PC Card Interface

Clock and Signal Slew Rate
(VCC_CORE18V=1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70°C)

Symbol	Parameter	Min	Max	Unit	Notes
	CCLK				
t10a	Cycle Time, CCLK	30		ns	
t10b	Pulse Width Duration, CCLK High	12		ns	
t10c	Pulse Width Duration, CCLK Low	12		ns	
t10d	Slew Rate, CCLK Rising Edge	1	4	V/ns	
t10e	Slew Rate, CCLK Falling Edge	1	4	V/ns	
	Other CardBus Signals				
t10f	Slew Rate, Rising Edge	0.25	1	V/ns	
t10g	Slew Rate, Falling Edge	0.25	1	V/ns	

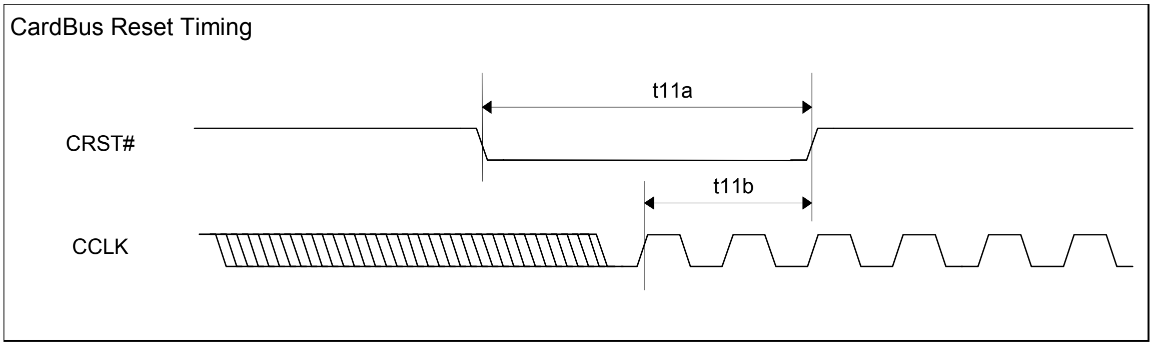
CCLK Timing and CardBus Signals Slew Rate


t10a
t10c
t10b
CCLK
0.475Vcc
0.4Vcc
0.325Vcc
t10e
t10d
Other CardBus Signals
0.475Vcc
0.325Vcc
t10g
t10f

CCLK Timing and CardBus Slew Rate

Card Reset
(VCC_CORE18V=1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70°C)

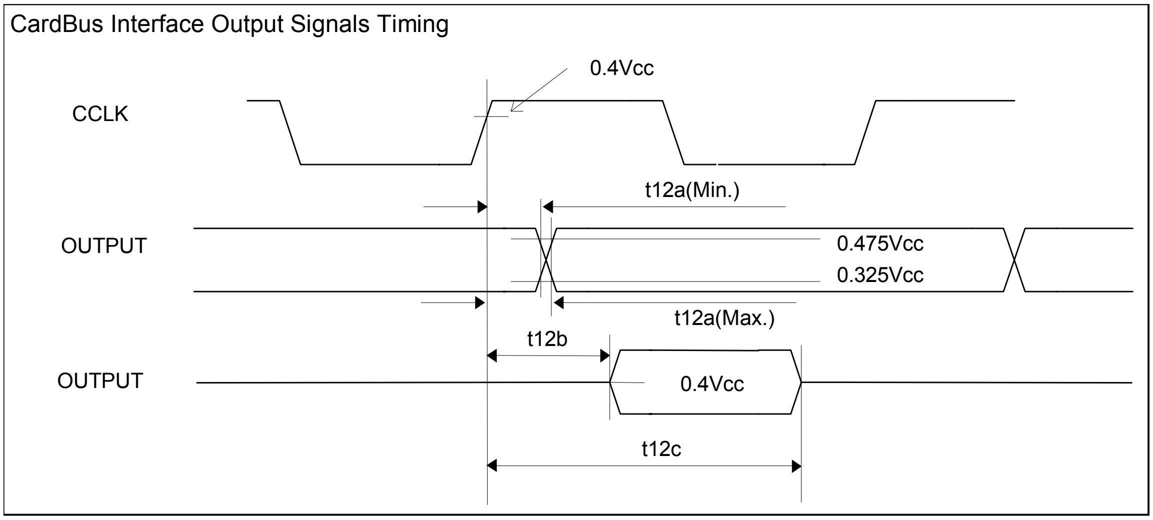
Symbol	Parameter	Min	Max	Unit	Notes
	CRST#				
t11a	Pulse Duration, CRST#	1		ms	
t11b	Setup Time, CCLK active at CRST# Negation	100		clocks	


CardBus Reset Timing
t11a
CRST#
t11b
CCLK

CardBus Reset Timing

Card Output
(VCC_CORE18V=1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70°C)

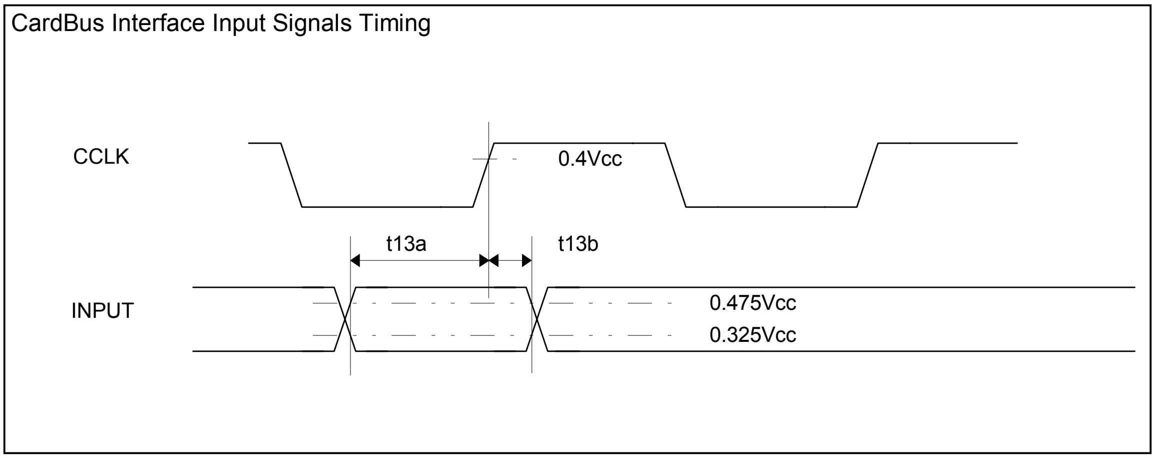
Symbol	Parameter	Min	Max	Unit	Notes
	CAD [31:0], CC/BE#[3:0], CPAR, CFRAME#, CDEVSEL#, CIRDY#, CTRDY#, CSTOP#, CPERR#, CSERR#, CCLKRUN#, CGNT#				
t12a	Valid delay time from CCLK	2	18	ns	Min: CL=0 pF Max: CL=30 pF
t12b	Enable Time, Hi-Z to active delay from CCLK	2		ns	
t12c	Disable Time, Active to Hi-Z delay from CCLK		28	ns	


CardBus Interface Output Signals Timing
0.4Vcc
CCLK
t12a(Min.)
OUTPUT
0.475Vcc
0.325Vcc
t12a(Max.)
t12b
OUTPUT
0.4Vcc
t12c

CardBus Interface Output Signals Timing

Card Input
(VCC_CORE18V=1.65~1.95V or 2.3~2.7V, VCC_3V=3.0~3.6V, Ta=0~70°C)

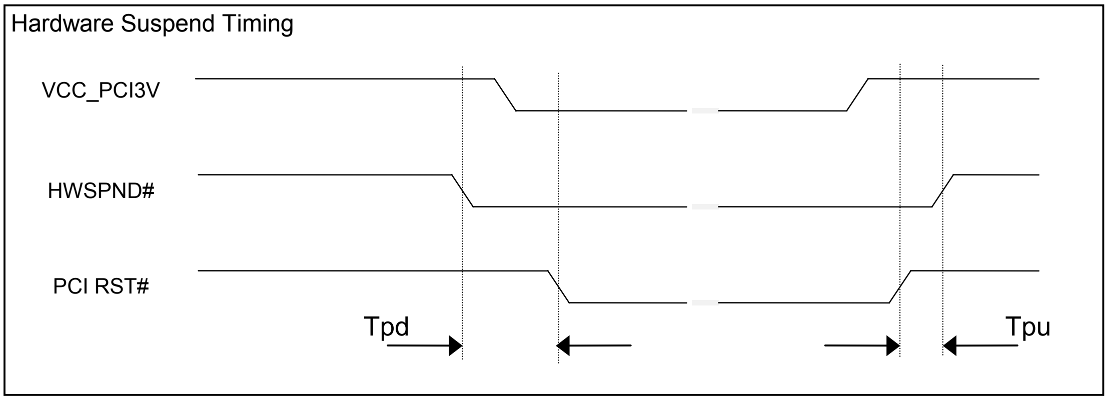
Symbol	Parameter	Min	Max	Unit	Notes
	CAD [31:0], CC/BE#[3:0], CPAR, CFRAME#, CDEVSEL#, CIRDY#, CTRDY#, CSTOP#, CPERR#, CSERR#, CCLKRUN#, CREQ#				
t13a	Setup Time, Signal Valid before CCLK	7		ns	
t13b	Hold Time, Signal Hold Time after CCLK High	0		ns	


CardBus Interface Input Signals Timing
CCLK
0.4Vcc
t13a
t13b
INPUT
0.475Vcc
0.325Vcc

CardBus Input Signals Timing

8.3.5 Hardware Suspend mode

Timing chart for keeping the value of the internal register on the Suspend mode.

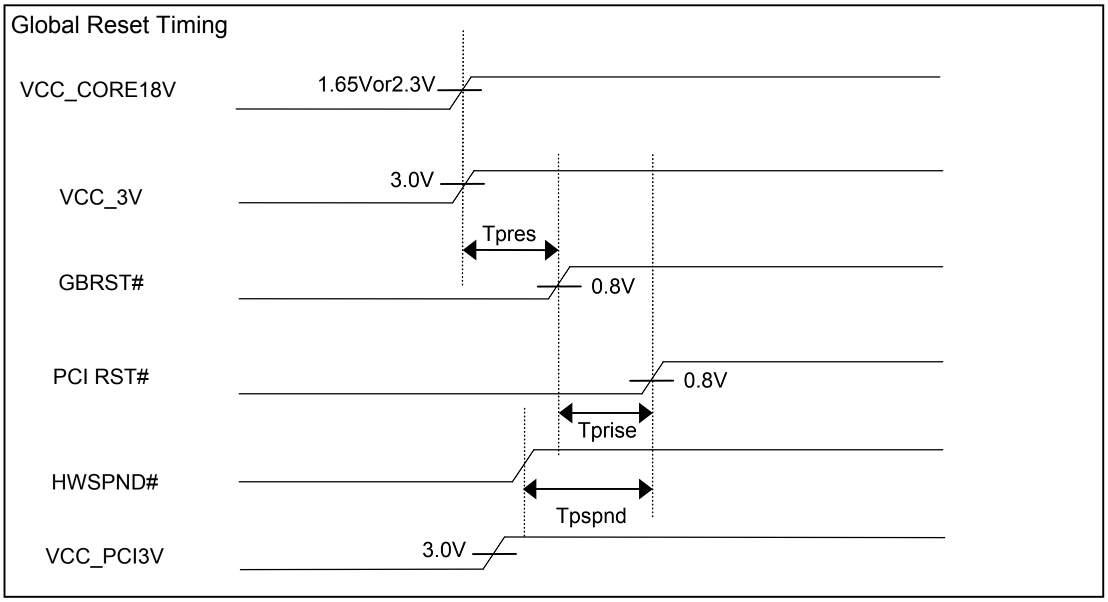

Hardware Suspend Timing
VCC_PCI3V
HWSPND#
PCI RST#
Tpd
Tpu

Symbol	Parameter	Min	Typ	Max	Unit
Tpd	HWSPND# to PCIRST# delay	100*[1]			ns
Tpu	HWSPND# to PCIRST# delay	100*[1]			ns

*[1] : PCICLK=33MHz

8.3.6 Global Reset

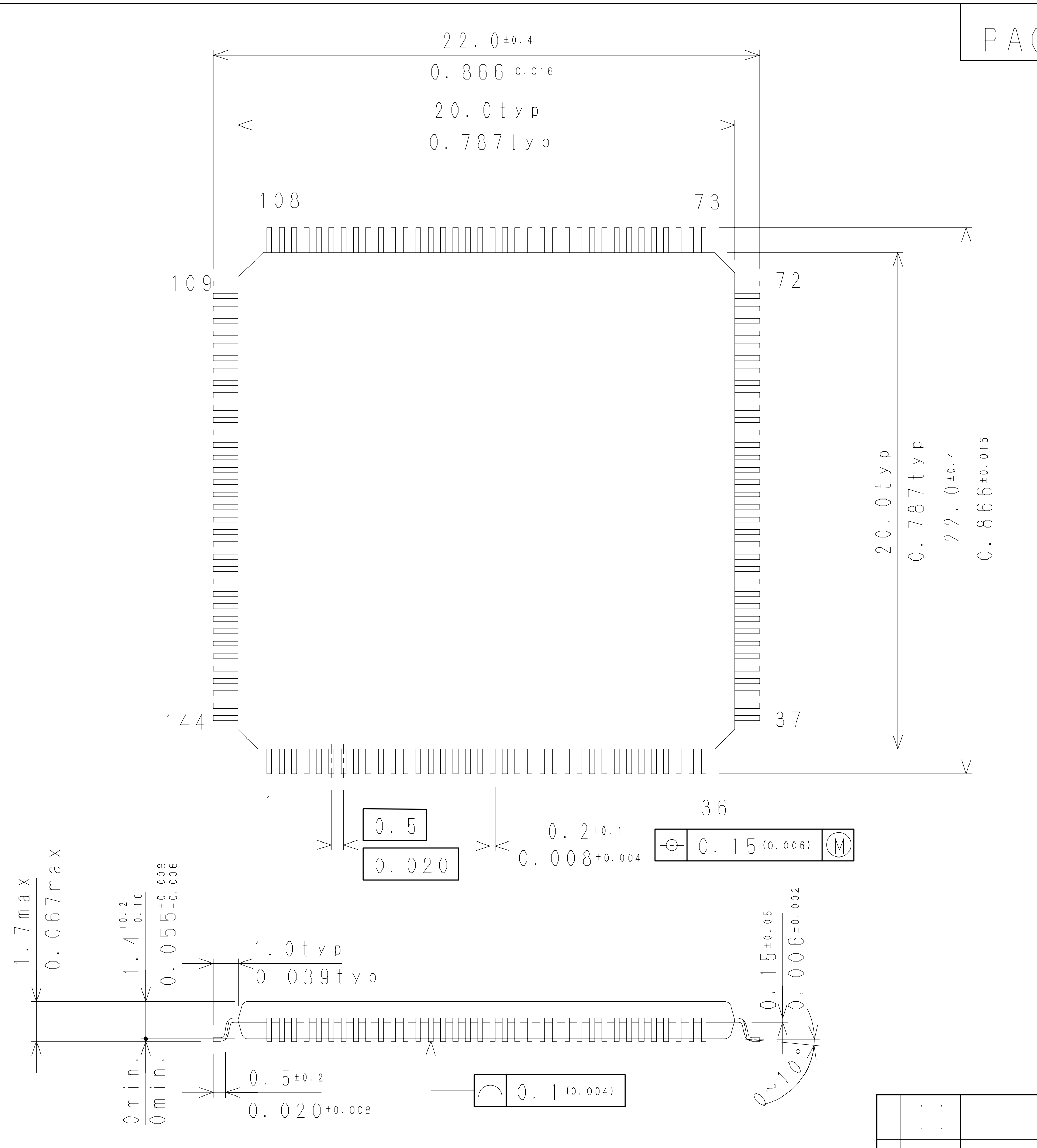
Timing chart for initializing the internal register on the Power's on.


Global Reset Timing
VCC_CORE18V
1.65Vor2.3V
VCC_3V
3.0V
Tpres
GBRST#
0.8V
PCI RST#
0.8V
Tprise
HWSPND#
Tpspnd
VCC_PCI3V
3.0V

Symbol	Parameter	Min	Typ	Max	Unit
Tpres	Power_On to GBRST# delay	1			ms
Tprise	GBRST# to PCIRST# delay	60*[2]			ns
Tpspnd	HWSPND# to PCIRST# delay	100*[2]			ns

*[2] : PCICLK=33MHz

PACKAGE CODE LQFP-144-P2 (2020)


22.0±0.4
0.866±0.016
20.0typ
0.787typ
108
73
109
72
144
37
1
36
20.0typ
0.787typ
22.0±0.4
0.866±0.016
0.5
0.020
0.2±0.1
0.008±0.004
0.15(0.006) M
1.7max
0.067max
1.4+0.2-0.16
0.055+0.008-0.006
1.0typ
0.039typ
0.15±0.05
0.006±0.002
0min.
0min.
0.5±0.2
0.020±0.008
0.1(0.004)
0°~10°

UNIT: MM/INCH

指定以外ノ寸法ニ対スル寸法差 (±)

ヨビ寸法 \ 等級	0級	1級	2級	3級	4級	5級
4以下	0.05	0.1	0.1	0.1	0.2	0.5
4ヲコエ 16マデ	0.05	0.1	0.1	0.2	0.3	0.8
16ヲコエ 63マデ	0.05	0.1	0.2	0.3	0.5	1.2
63ヲコエ 250マデ	0.1	0.2	0.3	0.5	0.8	1.8
250ヲコエ1000マデ		0.3	0.5	0.8	1.2	3.0
1000ヲコエ4000マデ			0.8	1.2	1.8	5.0

指定等級

角度 ±

外観等級

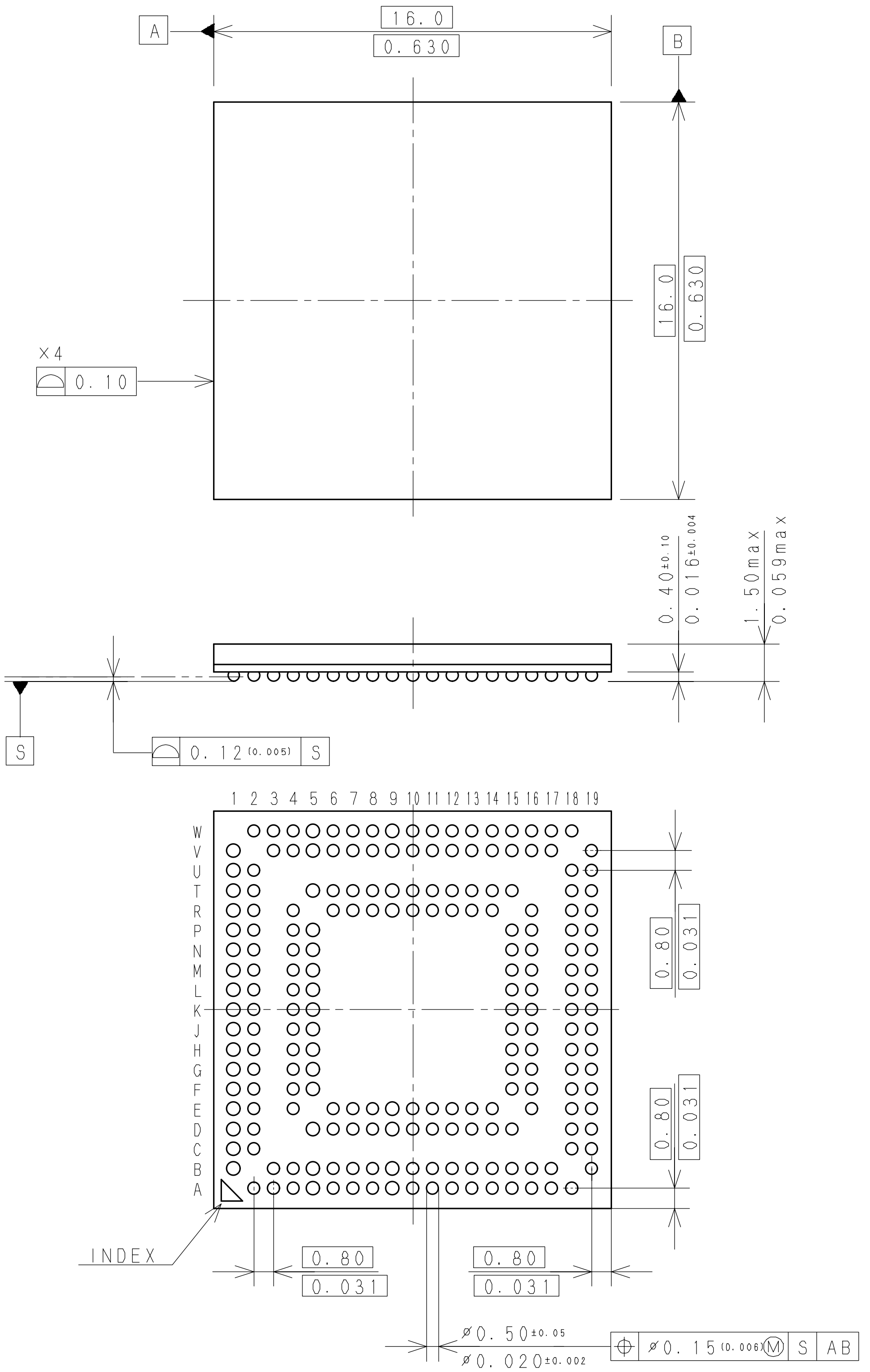
尺度 NTS

年 月 日 変更記事／作成年月日 96・6・26 変更者

品名 LQFP-144PIN(P2) PACKAGE OUTLINE

承認 吉村
検図 後藤
設計
製図 徳山
親部番
部番 DF-144LQFP-002A

PACKAGE CODE	CSP-208-P2 (1616)


A
16.0
0.630
B
×4
0.10
16.0
0.630
0.40±0.10
0.016±0.004
1.50max
0.059max
S
0.12 (0.005) S
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
W
V
U
T
R
P
N
M
L
K
J
H
G
F
E
D
C
B
A
0.80
0.031
0.80
0.031
INDEX
0.80
0.031
0.80
0.031
∅0.50±0.05
∅0.020±0.002
∅0.15 (0.006) M S AB

UNIT: mm / inch

	· ·		
C	01·03·12	TERMINAL POSITION TOLERANCE (0.15→∅0.15)	R. TOKUYAMA
	· ·	ADDITION OF TOLERANCE	R. TOKUYAMA
B	01·03·06	(TERMINAL POSITION & PACKAGE EDGE)	
╱	DATE	CHANGE NOTICE	SIGN

DIMENSIONAL TOLERANCE (±)

DIMENSION X	0	1	2	3	4	5
X ≤ 4	0.05	0.1	0.1	0.1	0.2	0.5
4< X ≤ 16	0.05	0.1	0.1	0.2	0.3	0.8
16< X ≤ 63	0.05	0.1	0.2	0.3	0.5	1.2
63< X ≤ 250	0.1	0.2	0.3	0.5	0.8	1.8
250< X ≤1000		0.3	0.5	0.8	1.2	3.0
1000< X ≤4000			0.8	1.2	1.8	5.0

SPECIFIED GRADE

VISUAL GRADE

ANGLE TOL ±

SCALE NTS

DRAW UP DATE 2000·2·16

PART NAME CSP-208PIN (P2) PACKAGE OUTLINE

APPROVED BY	CHECKED BY	DESIGNED BY	DRAWN BY
T. KAWAKAMI	T. SEIGENJI	M. HIGASHIGUCHI	R. TOKUYAMA

PART NO. DF-208CSP-002 C

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