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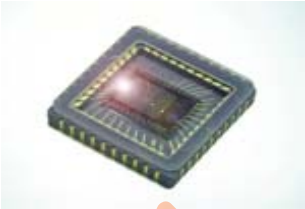
Preliminary Data sheet



PO3130R
1/3.3 Inch SXGA Single Chip CMOS IMAGE SENSOR

Rev 0.34

Last update : 21. Aug . 2006

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Revision History

Version	Date [D/M/Y]	Notes	Writer
0.0	18/07/2005	*(Preliminary)*	Shin Jong Ho
0.1	25/07/2005	Revision number, edit register table	Shin Jong Ho
0.2	10/08/2005	Modified the recommended reg. settings	Sung Je Cheon
0.21	22/09/2005	Modified 1Dh, 45h, 46h register description	BJ Lee
0.22	12/10/2005	Modified Table1	BJ Lee
0.23	17/11/2005	Modified the application note in Flicker setting part	BJ Lee
0.24	21/11/2005	Modified Additional setting according to the resolution in the application note	Sung Je Cheon
0.25	14/02/2006	Modified Application note setting value for CIF output	BJ Lee.
0.26	02/03/2006	Add SNR p4 & Modified application note p78	Sung Je Cheon
0.27	11/05/2006	Modified Table of Contents Modified Figure of Application Note p66, 67, 68 p7, p37, 40, 44, 59, 60, 61, 62, 70, 71, 75, 79 edited Y target Control reg edited Figure 6, 9, 10 edited	YouSu Song
0.28	12/05/2006	p80 changed	SungJe Cheon
0.29	12/05/2006	p83 edited	YouSu Song
0.30	12/06/2006	Modified the DC Characteristics	BJ Lee
0.32	11/08/2006	Modified the Standby Method Modified the PCB Layout Considerations	Sung Je Cheon
0.33	14/08/2006	Modified Operation Temp. in Table 1. Added Operation & Performance Temp. to Electrical Characteristic.	Joo Hee Choi
0.34	21/08/2006	Modified AC Characteristics. in Table5. Modified I2C Bus signal timing in Table 6. Modified Power ON,OFF Sequence in Table 7.	Sang Hyun Kim

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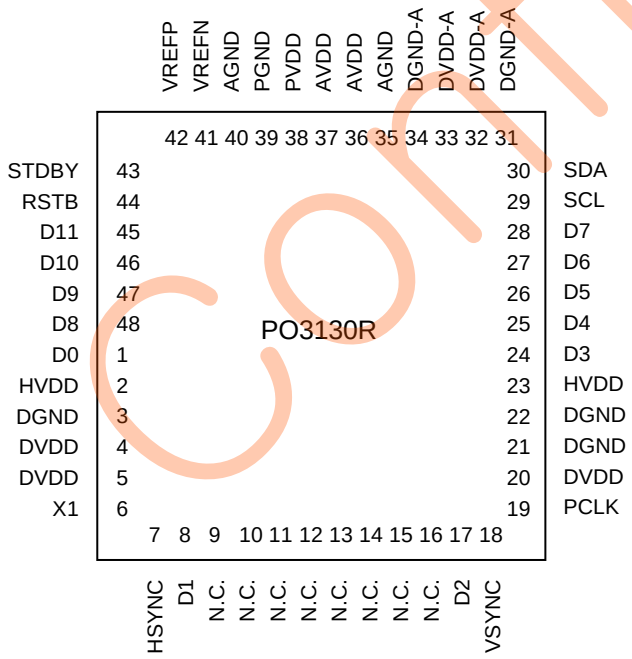
CMOS Image Sensor with 1280 X 1024 Pixel Array and Integrated On-Chip Image Signal Processor

Table of Contents

CMOS Image Sensor with 1280 X 1024 Pixel Array and Integrated On-Chip Image Signal Processor

Features

- 1 / 3.3 inch 1280 X 1024 active pixel array with color filters and micro-lens.
- Power supply 1.8V for core and 1.8 ~ 3.3V for I/O.
- Power down mode through pin or I2C register setting.
- Output formats : 8bit YCbCr, RGB565, 10bit Bayer data, 12bit RGB888, CCIR.656
- Max. 15 (SXGA) frames/sec progressive scan @ 54 MHz master clock.
  Max. 30 (VGA) frames/sec progressive scan @ 27 MHz master clock
- Image processing on chip : lens shading, gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, brightness, contrast, saturation, auto white balance, auto exposure control and back light compensation.
- Still image capture with electrical shutter.
- Frame size, window size and position controllable through a serial interface bus.
- SXGA/VGA/QVGA/QQVGA/CIF/QCIF sub-sampling and scaling.
- Horizontal / Vertical mirroring.
- 50Hz, 60Hz flicker automatic cancellation.
- 2x, 3x, 4x PLL
- Package : 48 pin CLCC.



< Figure. 1> Pin Diagram

Table 1. Typical Parameters

Total Pixel Array	1296 X 1040
Pixel Size	3.3um X 3.3um
Image Area	4.27mm X 3.43mm
Clock Rate (Max.)	54 MHz
Frame rate	Variable up to 15 fps(SXGA) Variable up to 30 fps(VGA)
Dark Signal	11mV/sec
Sensitivity	1.83 V/Lux.sec @7.5fps,IR cut filter
Saturation Level	760 mV
Fill Factor	35%
Supply voltage	1.8 ~ 3.3V I/O,1.8V Core
Power consumption	33 mA @ 7.5fps,2.5V I/O,active
	10 uA @ Standby
Operation Temp.	-30 ~ 70 ℃
Dynamic Range	56 dB
SNR	42 dB
Package	48 pin CLCC

PIN Descriptions

Pin No.	Name	I/O Type	Functions / Descriptions
1	D0	O	Bit 0 of data output.
2	HVDD	P	Digital VDD for I/O : DC 1.8~3.3V. Voltage range for all output signals is 0V ~ HVDD.
3	DGND	P	Digital ground. Core and I/O circuits share the ground pads.
4 ~ 5	DVDD	P	Digital VDD : 1.8V DC, 100nF to DGND
6	X1	I	Master clock : Crystal input pad.
7	HSYNC	O	Horizontal synchronization pulse. HSYNC is high (or low) for the horizontal window of interest. It can be programmed to appear or not outside the vertical window of interest.
8	D1	O	Bit 1 of data output.
9 ~ 16	N.C.	X	No Connection.
17	D2	O	Bit 2 of data output.
18	VSYNC	O	Vertical synchronization pulse : Indicates the start of a new frame.
19	PCLK	O	Pixel clock. Data can be latched by external devices at the rising or falling edge of PCLK. The polarity can be controlled.
20	DVDD	P	Digital VDD : 1.8V DC, 100nF to DGND
21 ~ 22	DGND	P	Digital ground. Core and I/O circuits share the ground pads.
23	HVDD	P	Digital VDD for I/O : DC 1.8~3.3V. Voltage range for all output signals is 0V ~ HVDD.
24	D3	O	Bit 3 of data output.
25	D4	O	Bit 4 of data output.
26	D5	O	Bit 5 of data output.
27	D6	O	Bit 6 of data output.
28	D7	O	Bit 7 of data output.
29	SCL	I	I2C serial clock input.
30	SDA	I/O	I2C serial data bus.

Table 2-1. PIN Descriptions

Pin No.	Name	I/O Type	Functions / Descriptions
31	DGND-A	P	Analog Part Digital ground.
32, 33	DVDD-A	P	Analog Part Digital VDD : 1.8V DC, 100nF to Analog Part DGND-A
34	DGND-A	P	Analog Part Digital ground.
35	AGND	P	Analog ground.
36, 37	AVDD	P	Analog VDD : 1.8V DC, 100nF to AGND.
38	PVDD	P	Pixel array current is supplied from PVDD : 1.8V DC. 100nF to PGND.
39	PGND	P	Ground for pixel array.
40	AGND	P	Analog ground.
41	VREFN	O	ADC reference voltage. 100nF capacitor to AGND.
42	VREFP	O	ADC reference voltage. 100nF capacitor to AGND. ADC assumes V(REFP) – V(REFN) is the minimum input voltage that will be converted to FFh.
43	STDBY	I	Power standby mode. When STDBY='1' there's no current flow in any analog circuit branch, neither any beat of digital clock. D<11:0> and PCLK, HSYNC, VSYNC pins can be programmed to tri-state (Hi-Z). But it is possible to control internal registers through I2C bus interface in STDBY mode. All registers retain their current values.
44	RSTB	I	System reset must remain low for at least 8 master clocks after power is stabilized. When the sensor is reset, all registers are set to their default values.
45	D11	O	Bit 11 of data output. Luminance data Y<7:0> are mapped to output pins D<11:4>. Chrominance data UV<7:0> are also mapped to output pins D<11:4>. 10bit Bayer RGB data are mapped to output pins D<11:2>.
46	D10	O	Bit 10 of data output.
47	D9	O	Bit 9 of data output.
48	D8	O	Bit 8 of data output.

Table 2-2. PIN Description

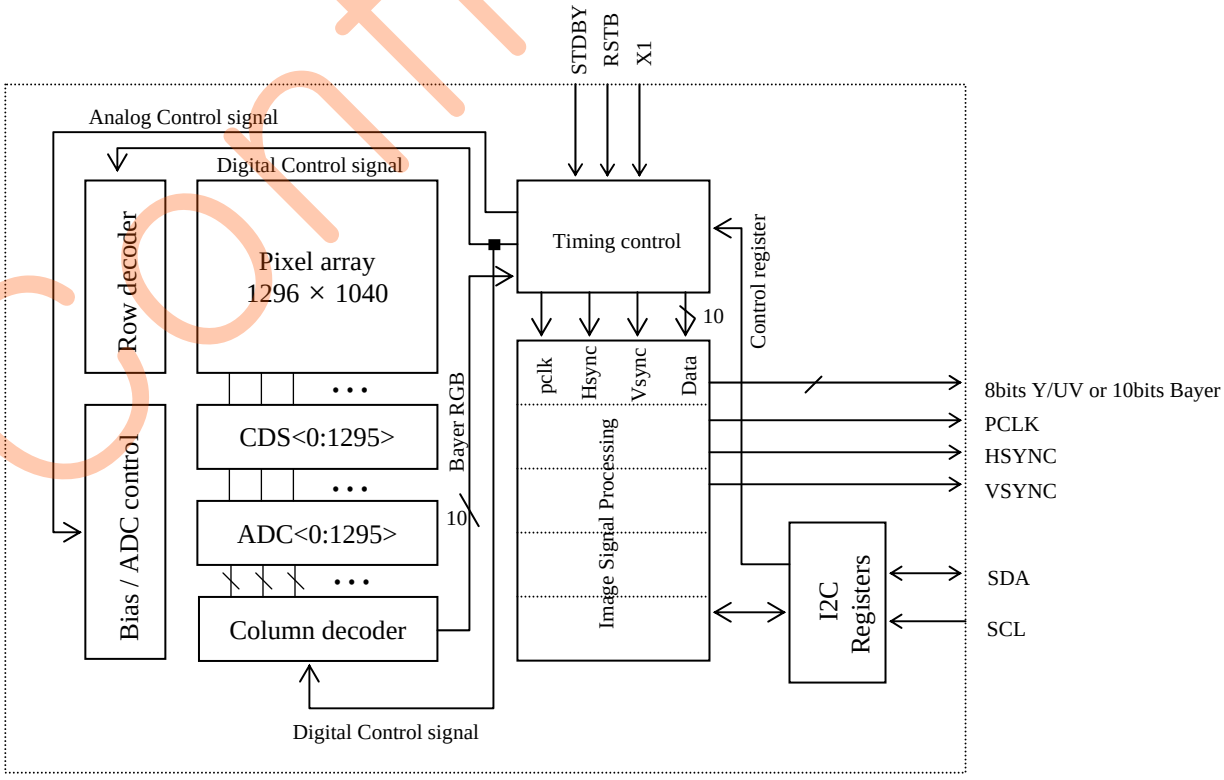
CMOS Image Sensor with 1280 X 1024 Pixel Array and Integrated On-Chip Image Signal Processor

Signal Environment

PO3130R has 3.3V tolerant Input pads. Input signals must be higher than or equal to HVDD but cannot be higher than 3.3V. PO3130R input pad has built in reverse current protection circuit, which makes it possible to apply input voltage even if the HVDD is disconnected or floating. Voltage range for all output signals is 0V ~ HVDD.

Chip Architecture

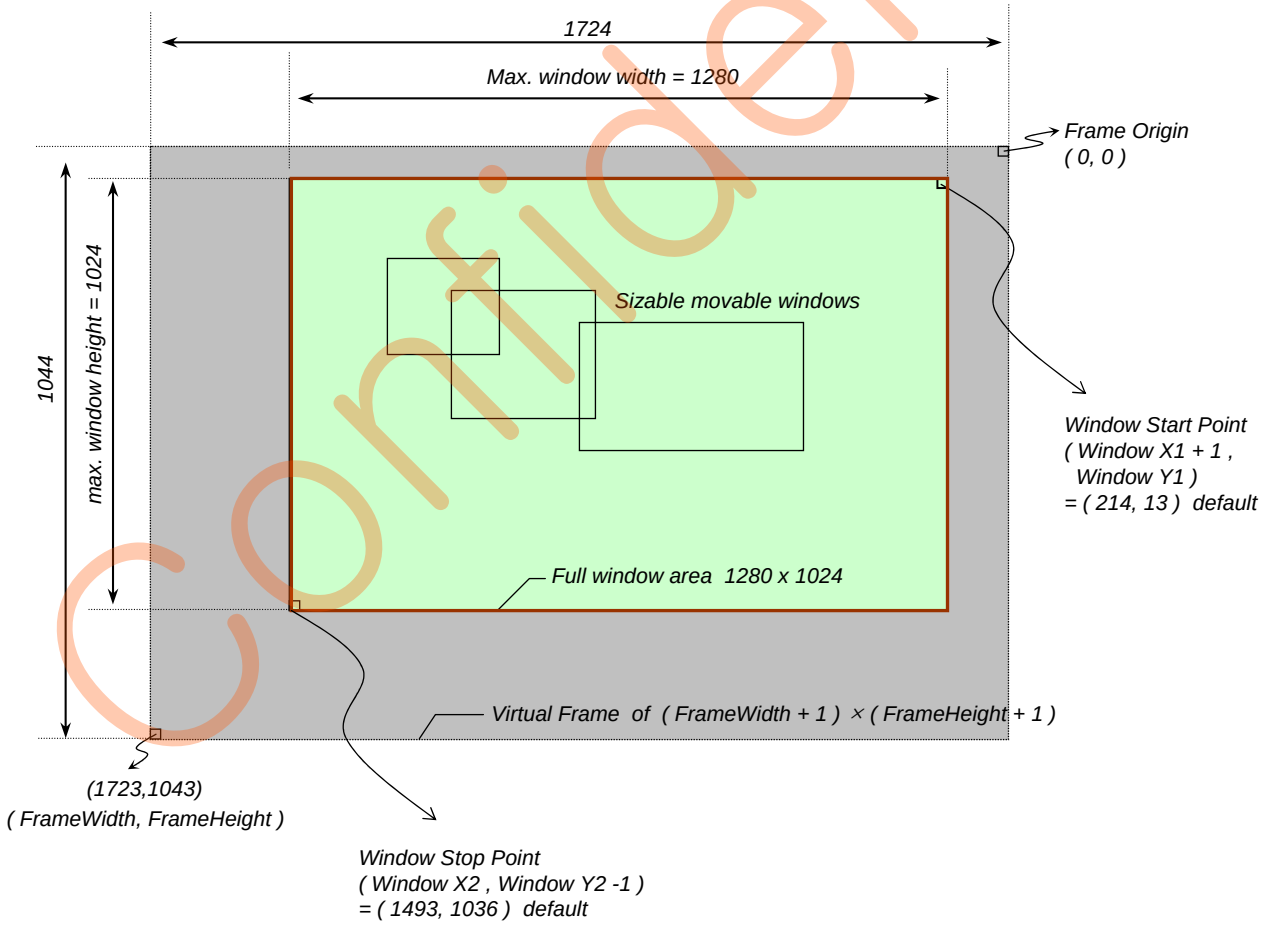
PO3130R has 1296 x 1040 effective pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing blocks to finally produce YCbCr 4:2:2 output data. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through I^2C serial interface.



<Figure. 2> Block Diagram

Frame Structure and Windowing

Origin *(0, 0)* of the frame is at the upper right corner. Size of the frame is determined by two registers : *FrameWidth* and *FrameHeight.* One frame consists of *FrameWidth + 1* columns and *FrameHeight + 1* rows. *FrameWidth* and *FrameHeight* can be programmed to be larger than physical array size. Physical array of 1280 × 1024 pixels is positioned at *(214, 13).* It is possible to define a specific region of the frame as a window. Pixel scanning begins from *(0, 0)* and proceeds row by row downward, and for each line scan direction is from right to the left. HSYNC signal indicates if the output is from a pixel that belongs to the window or not. There are two counters to indicate the present coordinate of frame scanning : Frame row counter and frame column counter. Counter values repeat the cycle of 0 to *FrameHeight* , and 0 to *FrameWidth* respectively. The counter values increase at the pace of pixel clock (PCLK), which does not change as the frame size is altered. The pixel data rate is fixed and is independent of frame size (frame rate.)



< Figure. 3 > Default structure of frame and window. (Top view)

Data Formats

Pixel array is covered by Bayer color filters as can be seen in the figure 4. Since each pixel can have only one type of filter on it, only one color component can be produced by a pixel. PO3130R provides this Bayer pattern RGB data through an 10bit channel. But since it is necessary to know all 3 color components R, G, B to produce a color for a pixel, the other two components must be inferred from other pixel data. For example, G component for a B pixel is calculated as an average of its four nearest G neighbors, and its R component as an average of its four nearest R neighbors. This operation of inferring missing data from existing ones is called the color interpolation. Color interpolation produces an undesirable artifact in image. Sampling nature of color filter can leave an interference pattern around an area with repetitive fine lines. PO3130R adopts a low pass filter to prevent the interference patterns(called Moire pattern) from degrading the image quality too much. After color interpolation, every pixel has all three color components. These three color components R, G, B can be routed to 12 bit output pins in such a way that 8bit R data and upper 4bits of G data are passed first and then, lower 4 bits of G data and 8bit B data are passed to output pins. It takes two PCLK's to pass one pixel RGB data to output bus.

G1	R	G1	R
B	G2	B	G2
G1	R	G1	R
B	G2	B	G2

< Figure. 4 > Bayer filter pattern

It is possible to extract monochrome luminance data from RGB color components and the conversion equation is : Y = 0.299R + 0.587G + 0.114B where R,G and B are gamma corrected color components. And the color information is separated from luminance information according to following equations.

$$U = 0.492 (B – Y)$$

$$V = 0.877 (R – Y)$$

Since human eyes are less sensitive to color variation than to luminance, color components can be sub-sampled to reduce the amount of data to be transmitted, but preserving almost the same image quality.

U1	Y1	V1	Y2	U3	Y3	V3	Y4	…

< Figure. 5> 4:2:2 YUV data sequence.

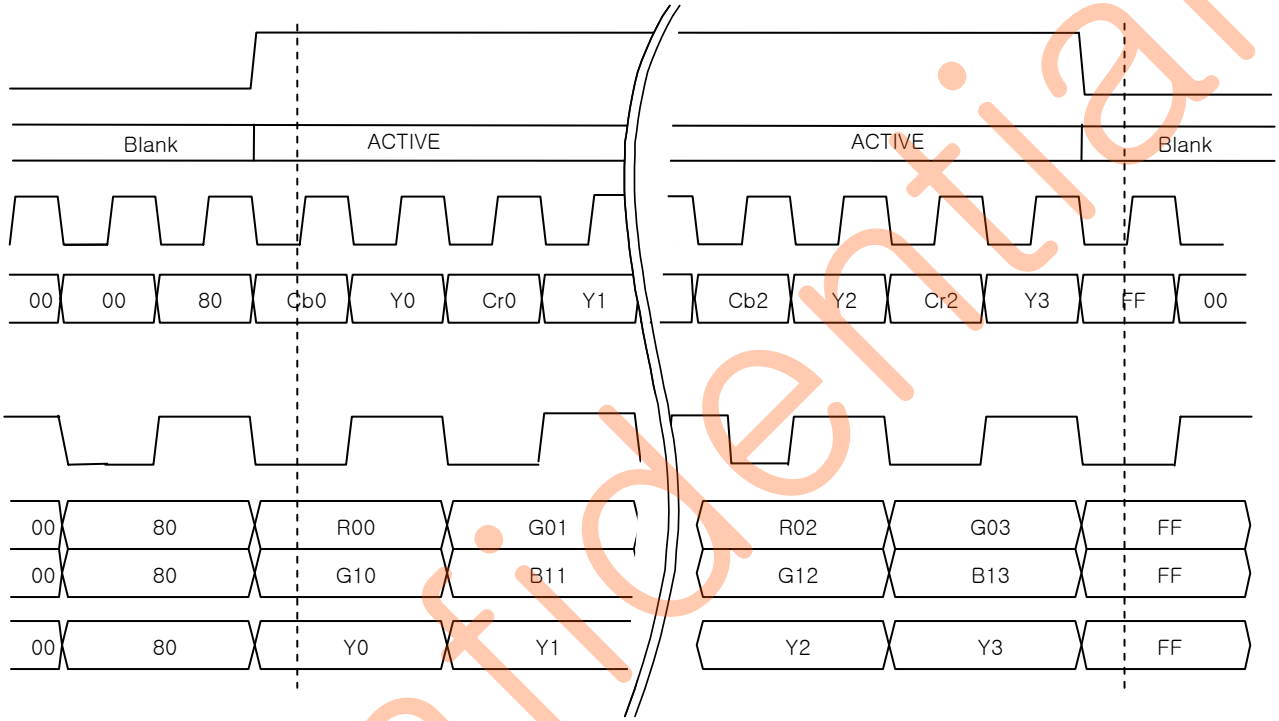
PO3130R supports 4:2:2 YUV data format where U and V components are horizontally sub-sampled such that U and V for every other pixel are omitted. PO3130R also supports ITU-R BT.601 YC_BC_R format which is a scaled, offset version of YUV. Y is the same in both formats but the C_BC_R is formed as follows.

$$C_B = 0.564 (B – Y) + 128$$

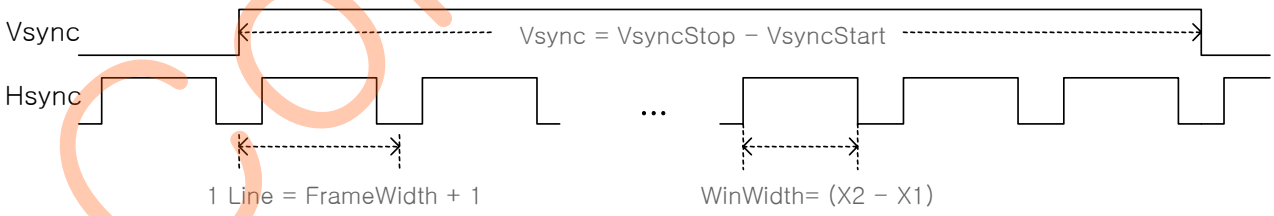
$$C_R = 0.713 (R – Y) + 128$$

Data and Synchronization Timing

In <Fig.6>, HSYNC / VSYNC / PCLK polarity can have any combinations possible. Data can be latched at the rising or falling edge of PCLK. HSYNC and VSYNC can be set to be active high or active low.



< Figure. 6 > Timing diagram for HSYNC, PCLK and data

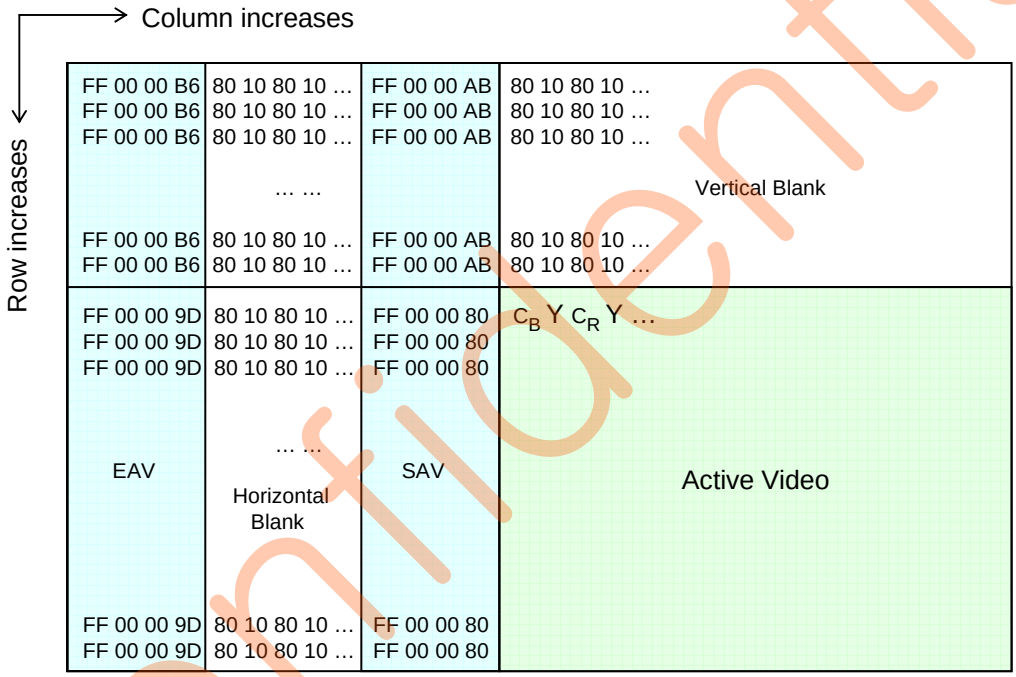


< Figure. 7> Timing diagram for VSYNC and HSYNC

In <Fig.7>, The width of VSYNC can be controlled by VsyncStart/VsyncStop registers : Vsync Width = (VsyncStop - VsyncStart). The width of Hsync can be controlled by windowX1/X2 registers: Hsync Width = WindowX2 - WindowX1

See register Description : # A2h ~ # A7h

In <Fig. 8>, EAV(End of Active Video) and SAV(Start of Active Video) signals are inserted for synchronization purposes. EAV is a 4 byte sequence of “FF 00 00 9D” for active lines, and “FF 00 00 B6” for blank lines. SAV is a 4 byte sequence of “FF 00 00 80” for active lines, and “FF 00 00 AB” for blank lines. HSYNC signal is asserted right after the SAV sequence and de-asserted right before the EAV sequence. Horizontal and vertical blank area is repeatedly filled with “80 10”.



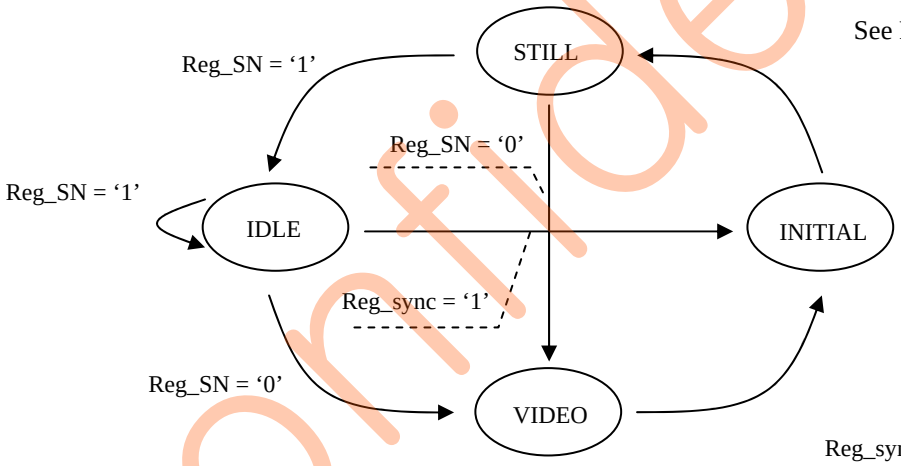
< Figure. 8 > Frame data sequence including EAV and SAV.

Video Mode(Preview Mode) and Still Image Capture Mode

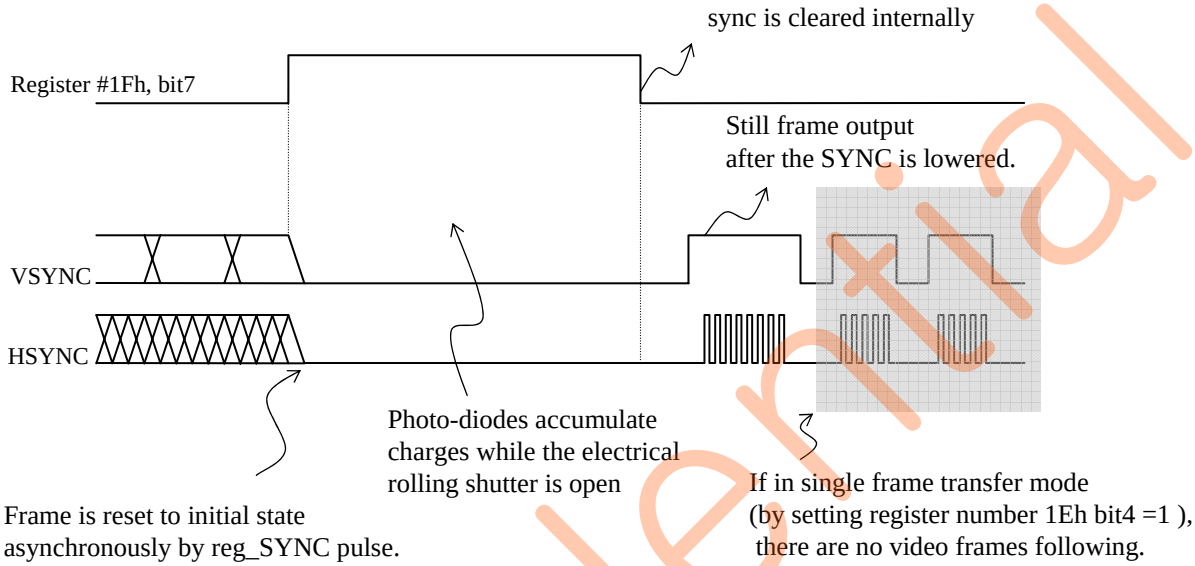
PO3130R normally operates in video mode. If you want to capture still image, User must do as follows.

step1 : set register #20h (set appropriate register value : image resolution)
step2 : set register #1Fh bit7 to '1'.

When bit7 of register 31d (1Fh) is set to '1', Sensor is under still state using electrical rolling shutter. After Still state, video mode may follow immediately or the sensor may be in idle state until an appropriate bit(reg_SN) is reset in the I²C register file. While the sensor is in idle state, there's no HSYNC or VSYNC pulse. Image resolution switch between video and still mode (for example, video in VGA resolution and still image in SXGA resolution) can be done manually or automatically.



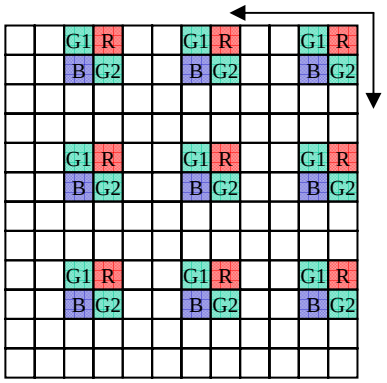
< Figure. 9 > Sensor state transition diagram



< Figure. 10> Still image capture with electrical shutter

Sub-sampling

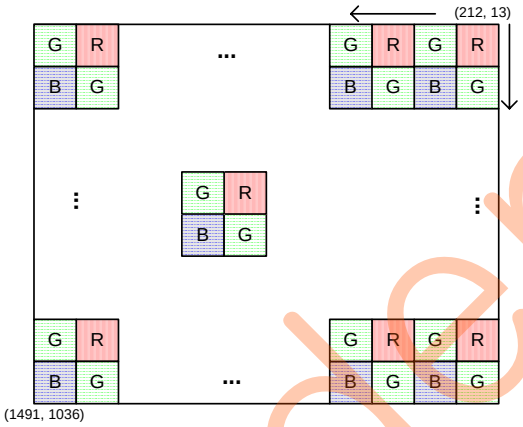
PO3130R supports one modes of sub-sampling : 1/4 sub-sampling . Figure 11 shows the way PO3130R selects sub-sample data from whole picture array. Since unselected rows and columns are omitted from counting, it takes only ¼ pixel clocks compared to the full-sampling case so that the frame rate is incremented by 4 times given the clock rate is identical for all modes. The clock rate can be reduced by a factor of 4 leaving frame size identical. *FrameWidth* is incremented by 4 times and the clock rate remains the same. *FrameHeight* is incremented by a factor of 2 and the clock frequency is decremented to half it used to be. PO3130R provides 30 fps under VGA mode using 27 MHz master clock while 7.5 fps under SXGA mode. Window position and size are all with respect to the full-sampling mode.



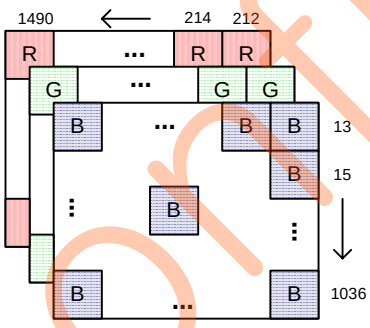
< Figure. 11 > 1/4 sub-sampling

Scaling

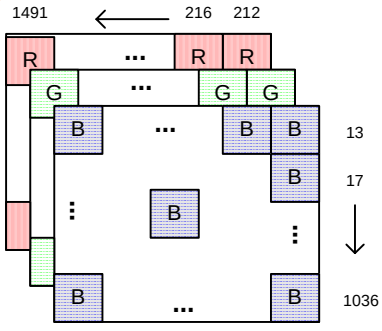
PO3130R supports four modes of scaling : 1/4 scaling, 1/16 scaling, CIF and QCIF. There are two ways of 1/4 sub-sampling that is 1/4 sensor sub-sampling and 1/4 scaling. And 1/16 sub-sampling has two ways also, which is (1/4 sensor sub-sampling + 1/4 scaling) and 1/16 scaling. It is possible CIF and QCIF scaling modes only in 1/4 sensor sub-sampling modes. It is dependent for frame rate on sensor sub-sampling modes. Figure 12 shows the scaling four modes. (Ref. reg20h)



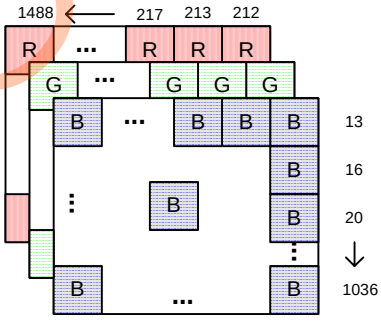
a. Normal Bayer Pattern



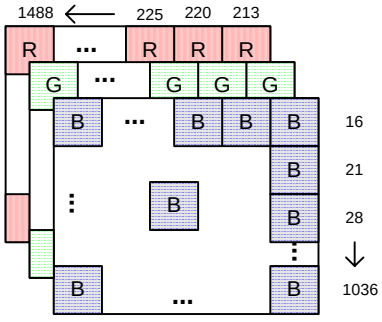
b. 1/4 scaling



c. 1/16 scaling



d. CIF scaling



e. QCIF scaling

< Figure. 12 >1/4 , 1/16, CIF, QCIF Scaling

I²C Description

The registers of PO3130R are written and read through the I²C interface. The PO3130R has I²C slave. The PO3130R is controlled by the I²C clock (SCL), which is driven by the I²C master. Data is transferred into and out of the PO3130R through the I²C data (SDA) line. The SCL and SDA lines are pulled up to VDD by a 2kΩ off-chip resistor. Either the slave or master device can pull the lines down. The I²C protocol determines which device is allowed to pull the two lines down at any given time.

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of an I²C device consists of 7 bits of address and 1 bit of direction. A 0 in the LSB of the address indicates write mode, and a 1 indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The I²C clock pulse is provided by the master. The data must be stable during the HIGH period of the I²C clock : it can only change when the I²C clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a 0 indicates a write and a 1 indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

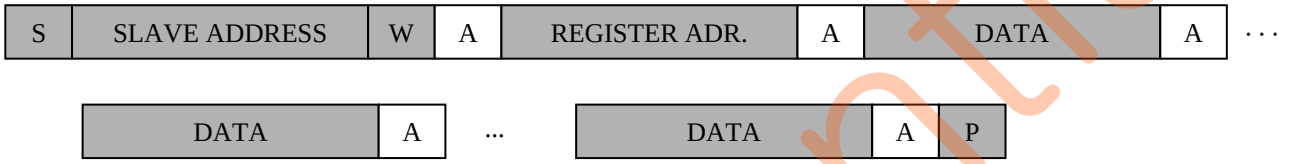
If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The PO3130R uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

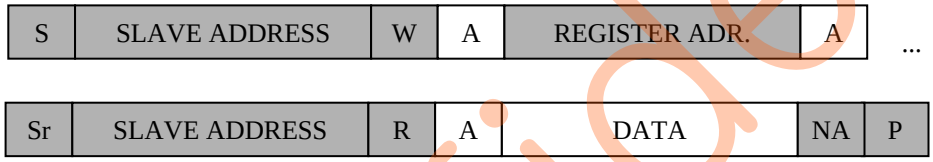
I²C Functional Description

Single Write Mode operation

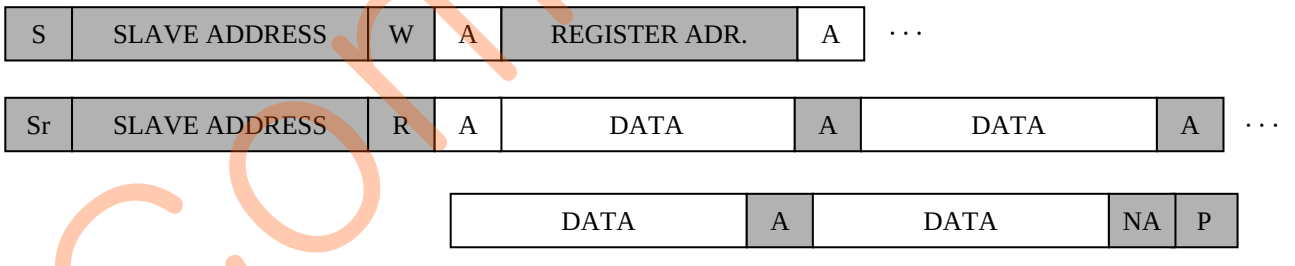
Multiple Write Mode (Register address is increased automatically)[1] operation



Single Read Mode operation



Multiple Read Mode (Register address is increased automatically)[1] operation



S: Start condition. Sr : Repeated Start (Start without preceding stop.)
SLAVE ADDRESS: write address = ECh = 11101100b
read address = EDh = 11101101b
R/W: Read/Write selection. High = read / LOW = write.
A: Acknowledge bit. NA : No Acknowledge.
DATA: 8-bit data
P: Stop condition

Note 1: Continuous writing or reading without any interrupt increases the register address automatically. If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.

Register Table

Address	Name	R/W	Default Value	Description
0 (00h)	DeviceID_H	R	00110001 (31h)	PO3130D Device ID
1 (01h)	DeviceID_L	R	00110000 (30h)	
2 (02h)	RevNumber	R	00000111 (07h)	Device Revision Number
4 (04h)	FrameWidth_H	RW	xx000110 (06h)	Frame Width = 1723d (06BBh)
5 (05h)	FrameWidth_L	RW	10111011 (BBh)	
6 (06h)	FrameHeight_H	RW	xx000100 (04h)	Frame Height = 1043d (0413h)
7 (07h)	FrameHeight_L	RW	00010011 (13h)	
8 (08h)	WindowX1_H	RW	00000000 (00h)	Window X1 = 213d (00D5h)
9 (09h)	WindowX1_L	RW	11010101 (D5h)	
10 (0Ah)	WindowY1_H	RW	00000000 (00h)	Window Y1 = 13d (000Dh)
11 (0Bh)	WindowY1_L	RW	00001101 (0Dh)	
12 (0Ch)	WindowX2_H	RW	00000101 (05h)	Window X2 = 1493d (05D5h)
13 (0Dh)	WindowX2_L	RW	11010101 (D5h)	
14 (0Eh)	WindowY2_H	RW	00000100 (04h)	Window Y2 = 1037d (040Dh)
15 (0Fh)	WindowY2_L	RW	00001101 (0Dh)	
18 (12h)	AmpBias	RW	xxxx0010 (02h)	Global Current Bias
19 (13h)	PixelBias	RW	xxxx0010 (02h)	Pixel Array Current Bias
21 (15h)	GlobalGain	RW	00000000 (00h)	Gain Factor that is Common to R, G, B
22 (16h)	RedGain	RW	01000000 (40h)	R Pixel Gain Factor
23 (17h)	Green1Gain	RW	01000000 (40h)	G1 Pixel Gain Factor
24 (18h)	BlueGain	RW	01000000 (40h)	B Pixel Gain Factor
25 (19h)	Green2Gain	RW	01000000 (40h)	G2 Pixel Gain Factor
26 (1Ah)	IntTime_H	RW	xx000000 (00h)	Pixel Integration Time
27 (1Bh)	IntTime_M	RW	10000000 (80h)	
28 (1Ch)	IntTime_L	RW	000000xx (00h)	
29 (1Dh)	Tgcontrol1	RW	00000101 (05h)	Timing Generate Control Registers
30 (1Eh)	Tgcontrol2	RW	00001010 (0Ah)	
31 (1Fh)	Tgcontrol3	RW	00011011 (1Bh)	
32 (20h)	Tgcontrol4	RW	01000100 (44h)	
56 (38h)	ADCOffset	RW	00000000 (00h)	ADC offset
68 (44h)	FdControl	RW	00000000 (00h)	Flicker Control Register
69 (45h)	regclk167_H	RW	xxxxxx01 (01h)	number of Master clock for flicker detection.
70 (46h)	regclk167_L	RW	01011111 (5Fh)	
71 (47h)	Period50H	RW	00000001 (01h)	Flicker Period (50Hz)
72 (48h)	Period50L	RW	00101100 (2Ch)	
73 (49h)	Period60H	RW	00000000 (00h)	Flicker Period (60Hz)
74 (4Ah)	Period60L	RW	11110100 (F4h)	
75 (4Bh)	IspControl1	RW	11011101 (DDh)	ISP Control Registers
76 (4Ch)	IspControl2	RW	00000000 (00h)	
77 (4Dh)	IspControl3	RW	00001010 (0Ah)	
78 (4Eh)	IspControl4	RW	01110000 (70h)	
86 (56h)	LensRGain	RW	xxxx0000 (00h)	Lens Shading Red Gain
87 (57h)	LensGGain	RW	xxxx0000 (00h)	Lens Shading Green Gain
88 (58h)	LensBGain	RW	xxxx0000 (00h)	Lens Shading Blue Gain
89 (59h)	Edge Control	RW	10101100 (ACh)	Edge Enhancement Gain
90 (5Ah)	Edge Th	RW	00000010 (02h)	Edge Enhancement Threshold
115 (73h)	GmCoeff0	RW	00000000 (00h)	Common Gamma Coefficients
116 (74h)	GmCoeff1	RW	00011010 (1Ah)	
117 (75h)	GmCoeff2	RW	00101010 (2Ah)	
118 (76h)	GmCoeff3	RW	00110111 (37h)	
119 (77h)	GmCoeff4	RW	01000010 (42h)	
120 (78h)	GmCoeff5	RW	01010110 (56h)	
121 (79h)	GmCoeff6	RW	01101000 (68h)	

Address	Name	R/W	Default Value	Description
122 (7Ah)	GmCoeff7	RW	10000111 (87h)	Common Gamma Coefficients
123 (7Bh)	GmCoeff8	RW	10100011 (A3h)	
124 (7Ch)	GmCoeff9	RW	10111100 (BCh)	
125 (7Dh)	GmCoeff10	RW	11010100 (D4h)	
126 (7Eh)	GmCoeff11	RW	11101010 (EAh)	
139 (8Bh)	ColorMatrix11	RW	00111000 (38h)	Color Correction Coefficients
140 (8Ch)	ColorMatrix12	RW	10100101 (A5h)	
141 (8Dh)	ColorMatrix13	RW	00001101 (0Dh)	
142 (8Eh)	ColorMatrix21	RW	10010011 (93h)	
143 (8Fh)	ColorMatrix22	RW	00101101 (2Dh)	
144 (90h)	ColorMatrix23	RW	00000110 (06h)	
145 (91h)	ColorMatrix31	RW	10000011 (83h)	
146 (92h)	ColorMatrix32	RW	10101010 (AAh)	
147 (93h)	ColorMatrix33	RW	01001101 (4Dh)	
148 (94h)	CG11C	RW	00100101 (25h)	Cb Color Gain
149 (95h)	CG22C	RW	00100101 (25h)	Cr Color Gain
152 (98h)	Bright	RW	00000000 (00h)	Y Brightness
153 (99h)	Contrast	RW	10010110 (96h)	Y Contrast
156 (9Ch)	CbTone	RW	10000000 (80h)	Cb sepia Data
157 (9Dh)	CrTone	RW	10000000 (80h)	Cr sepia Data
162 (A2h)	VsyncStart_H	RW	00000000 (00h)	Out Vsync Row Start = 13d (000Dh)
163 (A3h)	VsyncStart_L	RW	00001101 (0Dh)	
164 (A4h)	VsyncStop_H	RW	00000100 (04h)	Out Vsync Row Stop = 1037d (0040Dh)
165 (A5h)	VsyncStop_L	RW	00001101 (0Dh)	
166 (A6h)	VsyncColumn_H	RW	00000000 (00h)	Out Vsync Column Start = 110d (006Eh)
167 (A7h)	VsyncColumn_L	RW	01101110 (6Eh)	
170 (AAh)	WW control	RW	10011111 (9Fh)	Weight Window Control register
171 (ABh)	AE_lock	RW	00100010 (22h)	AE / AWB tolerance
172 (ACh)	AE_speed	RW	10001100 (8Ch)	AE speed
173 (ADh)	Exposure_H	RW	00000000 (00h)	Exposure
174 (AEh)	Exposure_M	RW	10000000 (80h)	
175 (AFh)	Exposure_L	RW	00000000 (00h)	
176 (B0h)	TargetExp	RW	01110000 (70h)	Y Bright Target
182 (B6h)	MaxFrmHeight_H	RW	00001000 (08h)	Maximum Frame Height
183 (B7h)	MaxFrmHeight_L	RW	00100110 (26h)	
184 (B8h)	MaxExp_H	RW	00010000 (10h)	Maximum Exposure Time
185 (B9h)	MaxExp_M	RW	01001100 (4Ch)	
186 (BAh)	MinExp_M	RW	00000000 (00h)	Minimum Exposure Time
187 (BBh)	MinExp_L	RW	00001100 (0Ch)	
190 (BEh)	RMinAwb	RW	00010000 (10h)	Minimum AWB R Gain
191 (BFh)	RMaxAwb	RW	11100000 (E0h)	Maximum AWB R Gain
192 (C0h)	BMinAwb	RW	00010000 (10h)	Minimum AWB B Gain
193 (C1h)	BMaxAwb	RW	11100000 (E0h)	Maximum AWB B Gain
194 (C2h)	Awb_rgratio	RW	10000000 (80h)	AWB RG ratio
195 (C3h)	Awb_bgratio	RW	10000000 (80h)	AWB BG ratio
196 (C4h)	weightx1_H	RW	00000010 (02h)	Weight Window : X1 = 615d (0267h)
197 (C5h)	weightx1_L	RW	01100111 (67h)	
198 (C6h)	weightx2_H	RW	00000100 (04h)	Weight Window : X2 = 1061d (0425h)
199 (C7h)	weightx2_L	RW	00100101 (25h)	
200 (C8h)	weighty1_H	RW	00000001 (01h)	Weight Window : Y1 = 349d (015Dh)
201 (C9h)	weighty1_L	RW	01011101 (5Dh)	
202 (CAh)	weighty2_H	RW	00000010 (02h)	Weight Window : Y2 = 691d (02B3h)
203 (CBh)	weighty2_L	RW	10110011 (B3h)	
209 (D1h)	Auto Control	RW	00111100 (3Ch)	AE / AWB enable
213 (D5h)	PLL Control	RW	00110000 (30h)	PLL Control
214 (D6h)	Gamma Control	RW	00101001 (29h)	Gamma Curve Selection

Register Descriptions

Register names are written in *slanted* characters. To differentiate between decimal, binary, and hexa numbers, (d, b, and h) are appended. The sensor should be reset by RSTB pin set low, after power is up, for at least 8 master clock periods. This will initialize all of the registers to their default values.

(0-2) DeviceID, RevNumber

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
00h	0	0	1	1	0	0	0	1	R
01h	0	0	1	1	0	0	0	0	
02h	x	x	x	x	0	1	1	1	

Default : 00h = 31h, 01h = 30h, 02h = 07h

Description :

Indicate PO3130R device ID, reversion number.

(4-5) FrameWidth

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
04h	x	x	0	0	0	1	1	0	RW
05h	1	0	1	1	1	0	1	1	

Default : 04h = 06h, 05h = BBh Frame Width = 1723d

Description :

FrameWidth is the number of columns to be counted during one line time. Column counter value is incremented 1 by 1 until it reaches *FrameWidth*, then it is reset to 0. It can be larger than physical frame width but cannot be smaller.

FrameHeight and *FrameWidth* determines the frame rate. Frame rate is given as follows.

Frame Rate = freq(MCLK) / *((FrameHeight* +1*)* x *(FrameWidth*+1 *) x 2)*

For example, If master clock (MCLK) = 27 MHz, *FrameHeight* = 1723d and *FrameWidth* = 1043d. then, the frame rate is 7.5 fps for SXGA Full Sampling Mode.

If you double the *FrameWidth*, you cut the frame rate by half. *FrameWidth* value must be set with respect to the full sampling mode. Changing to 1/4 or 1/16 sub-sampling mode does not require any change in *FrameWidth*.

(6-7) FrameHeight

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
06h	x	x	0	0	0	1	0	0	RW
07h	0	0	0	1	0	0	1	1	

Default : 06h = 04h, 07h = 13h Frame Height = 1043d

Description :

FrameHeight is the number of rows to be counted during one frame time. Row counter value is incremented 1 by 1 until it reaches *FrameHeight*, then it is reset to 0. It can be larger than physical frame height but cannot be smaller.

FrameHeight and *FrameWidth* determines the frame rate. Frame rate is given as follows

Frame Rate = freq(MCLK) / *((FrameHeight* +1*) x (FrameWidth*+1 *) x 2)*

For example, If master clock (MCLK) = 27 MHz, *FrameHeight* = 1723d and *FrameWidth* = 1043d. then, the frame rate is 7.5 fps for SXGA Full Sampling Mode.

If you double the *FrameHeight*, you cut the frame rate by half, and the vertical blank time is increased, but the PCLK rate does not change.

(8-9) WindowX1

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
08h	0	0	0	0	0	0	0	0	RW
09h	1	1	0	1	0	1	0	1	

Default : 08h = 00h, 09h = D5h WindowX1 = 213d

Description :

Window can be defined by 4 parameters : *WindowX1*, *WindowY1*, *WindowX2*, and *WindowY2*. Serial image data stream out pixel by pixel. Window specifies the area of pixels that we are interested in. HSYNC signal indicates if the image data output is from a pixel that lies within the window area or not.

Output data stream does not stop for pixels lying outside the window : just the HSYNC signal is de-asserted. The actual window position in the frame is given as

upper right corner = (*Window X1 + 1*, *Window Y1*)

lower left corner = (*Window X2*, *Window Y2 - 1*)

All the coordinates are with respect to the maximum window origin (0, 0) of Figure 3. Window position and size is with respect to the full sampling mode. It is not necessary to change the window parameters when sampling mode is switched between one and another.

(10-11) WindowY1

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0Ah	0	0	0	0	0	0	0	0	RW
0Bh	0	0	0	0	1	1	0	1	

Default : 0Ah = 00h, 0Bh = 0Dh WindowY1 = 13d

Description : refer to *Window X1*

(12-13) WindowX2

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0Ch	0	0	0	0	0	1	0	1	RW
0Dh	1	1	0	1	0	1	0	1	

Default : 0Ch = 05h, 0Dh = D5h WindowX2 = 1493d

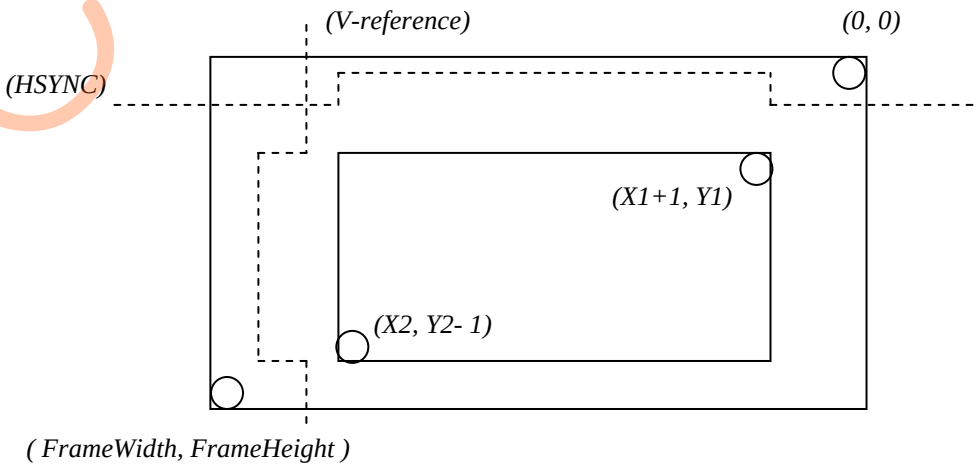
Description : refer to *Window X1*

(14-15) WindowY2

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0Eh	0	0	0	0	0	1	0	0	RW
0Fh	0	0	0	0	1	1	0	1	

Default : 0Eh = 04h, 0Fh = 0Dh WindowY2 = 1037d

Description : refer to *Window X1*



(18) Amp Bias

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
12h	x	x	x	x	0	0	1	0	RW

Default : 12h = 02h

Description :

All analog circuits such as opamp or reference voltage generators are biased using current mirrors. Current flowing in every branch of analog circuits is an integral multiple of 1uA.

Ibranch = (*Global I Bias*) * 1uA

If an opamp has 4 branches and *Global I Bias* is set to 2, then the amplifier consumes total current of 8uA . As the current increases, frequency response of OPAmp improves and better images can be obtained, but the power consumption also increases.

(19) Pixel Bias

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
13h	x	x	x	x	0	0	1	0	RW

Default : 13h = 02h

Description :

Pixel array has a source follower circuit for each column to buffer the photo-diode signal voltage. The source follower bias current is determined as an integral multiple of 1uA.

Ipixel = *PixelBias* * 1uA

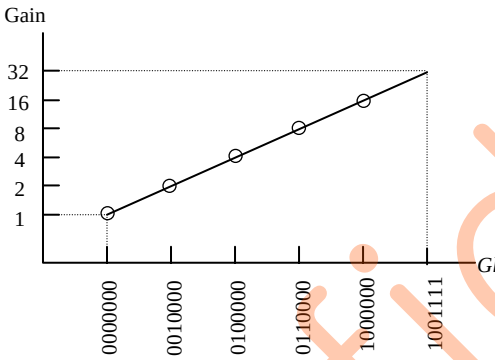
(21) Global Gain

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
15h	0	0	0	0	0	0	0	0	RW

Default : 15h = 00h

Description :

GlobalGain has effect on all of R, G, and B pixel outputs. Raw R, G, B data are amplified by a common factor of *GlobalGain*. The relation between *GlobalGain* and amplification factor is shown in the picture below.



Maximum value of *GlobalGain* is 1001111. Gain factors for *GlobalGain* larger than or equal to 1010000 are not defined.

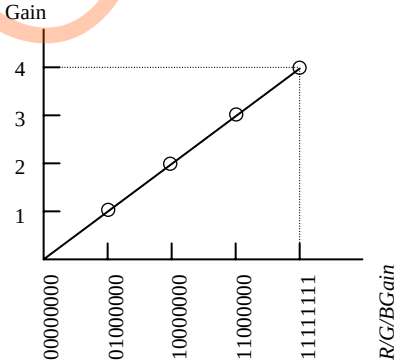
(22) Red Gain

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
16h	0	1	0	0	0	0	0	0	RW

Default : 16h = 40h

Description :

RGain is the multiplication factor for red pixel output. Total gain factor for red pixels is (gain from *GlobalGain*) * (gain from *Rgain*).



R / G / B gain can be used for white balance control. Bit7 of *R/G/BGain* is weighted by 2, bit6 by1 and the other consecutive bits are weighted by 1/2, 1/4, 1/8, … respectively. That is, *R/G/Bgain* is a binary number with decimal point between bit6 and bit5.

(23) Green 1 Gain

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
17h	0	1	0	0	0	0	0	0	RW

Default : 17h = 40h

Description :

G1 pixels are those green pixels whose nearest neighbors are red pixels.

Refer to *Red Gain(16h)* register description.

(24) Blue Gain

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
18h	0	1	0	0	0	0	0	0	RW

Default : 18h = 40h

Description : refer to *Red Gain(16h)* register description.

(25) Green 2 Gain

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
19h	0	1	0	0	0	0	0	0	RW

Default : 19h = 40h

Description :

G2 pixels are those green pixels whose nearest neighbors are blue pixels.

Refer to *Red Gain(16h)* register description.

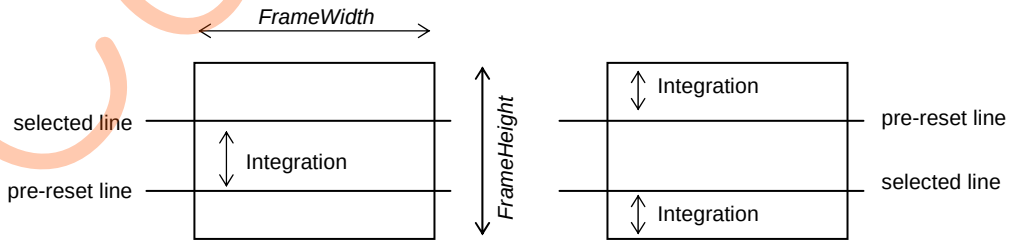
(26-28) Integration Time

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
1Ah	x	x	0	0	0	0	0	0	
1Bh	1	0	0	0	0	0	0	0	RW
1Ch	0	0	0	0	0	0	x	x	

Default : 1Ah = 00h, 1Bh = 80h, 1Ch = 00h, Integration Time = 8192d

Description :

There are 3 bytes of registers to control the photo-charge accumulation interval for each pixel. 1Ah and 1Bh registers indicate how many line times the integration will continue until they are all reset. 1Ch register further sub-divides one line time into 64 smaller intervals. Total integration time is the sum of the integral multiple and fractional parts of one line time. As the row counter value is incremented from 0 to *FrameHeight*, each line relevant to the row count is selected and all pixel data of that line is read out all at once. The read- out operation involves pixel reset pulses, so all pixels that are selected and read out are reset to initial states. To control exposure time, there runs another counter to select and reset a line other than the one that is selected to be read out. The space between the two lines is equal to the number of integration lines. There are two possible situations concerning the position of selected line and reset line. The 1st case is where the pre-reset counter runs ahead of read-out counter. And the other case Is just the reverse of the 1st one. The number of integration lines is different for the two cases as is shown in the left figures. Since the basic unit of integration time for PO3130R is 1/ 64 line time, it is easy to implement Auto Exposure algorithms without worrying about strong light environment where the image may change abruptly in brightness or it may even blink.



Case 1. Reset line preceding select line Case 2. Select line preceding reset line

(29) Timing Generator Control Register 1

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
1Dh	Drop	CK2	CK1	CK0	x	*RSV*	*RSV*	*RSV*	RW
	0	0	0	0	x	1	0	1	

Default : 1Dh = 05h

Description :

Bit name	value	Description
Drop	0	Frame Drop Disable.
	1	Frame Drop Enable.
CK(2:0)	000	Internal clock = (external master clock) x 1 / 2 (*default*)
	001	Internal clock = (external master clock) x 1 / 3
	010	Internal clock = (external master clock) x 1 / 4
	011	Internal clock = (external master clock) x 1 / 8
	100	Internal clock = (external master clock) x 1 / 16
	101	Internal clock = (external master clock) x 1 / 32
	110	Internal clock = (external master clock) x 1 / 64
	111	Internal clock = (external master clock) x 1 / 128

(30) Timing Generator Control Register 2

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
1Eh	HM	VM	*RSV*	SN	*RSV*	*RSV*	*RSV*	*RSV*	RW
	0	0	0	0	1	0	1	0	

Default : 1Eh = 0Ah

Description :

Bit name	value	Description
HM	0	Horizontal Mirror Disable. *(default)*
	1	Horizontal Mirror Enable.
VM	0	Vertical Mirror Disable*(default)*
	1	Vertical Mirror Enable.
SN	0	single still image output disable (*default*)
	1	single still image output enable

(31) Timing Generator Control Register 3

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
1Fh	sync	stdby	*RSV*	*RSV*	*RSV*	*RSV*	*RSV*	*RSV*	RW
	0	0	0	1	1	0	1	1	

Default : 1Fh = 1Bh

Description :

Bit name	value	Description
sync	0	Sync input register
stdby	0	Stdby input register

(32) Timing Generator Control Register 4

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
20h	SM7	SM6	SM5	SM4	SM3	SM2	SM1	SM0	RW
	0	1	0	0	0	1	0	0	

Default : 20h = 44h

Description :

MSB 4 bits control sub sampling mode under Video State, while LSB 4bits under Still State.
Bit(7) and Bit(3) are used for Sensor Sub Sampling Enable S/W under Video/Still state each other.

Under Video State or Still State

- Sensor Full sampling mode. (frame rate constant)
sm(7 : 4) or sm(3 : 0) : “01XX" => SXGA
sm(7 : 4) or sm(3 : 0) : “0001" => VGA (QSXGA)
sm(7 : 4) or sm(3 : 0) : “0011" => QVGA (QQSXGA)

- Sensor Q sub sampling mode. (frame rate increase)
sm(7 : 4) or sm(3 : 0) : "11XX" => VGA(QSXGA)
sm(7 : 4) or sm(3 : 0) : "1000" => CIF
sm(7 : 4) or sm(3 : 0) : "1001" => QVGA(QQSXGA)
sm(7 : 4) or sm(3 : 0) : "1010" => QCIF
sm(7 : 4) or sm(3 : 0) : "1011" => QQVGA (QQQSXGA)

(56) ADC offset

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
38h	0	0	0	0	0	0	0	0	RW

Default : 38h = 00h

Description :

ADC offset value.

(68) Flicker Control Register

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
44h	AF	F5	F6	FDM	FK1	FK0	FL1	FL0	RW
	0	0	0	0	0	0	0	0	

Default : 44h = 00h

Description :

Bit name	value	Description
AF	0 1	Manual Flicker Detection Enable Mode. Auto Flicker Detection Enable Mode
F5	0 1	50Hz Flicker Detection Mode Disable 50Hz Flicker Detection Mode Enable
F6	0 1	60Hz Flicker Detection Mode Disable 60Hz Flicker Detection Mode Enable
FDM	0 1	Flicker Duration long lasting Mode Flicker Duration only while the flicker exists.
FK (1:0)	00 01 10 11	Flicker Count Increase/Decrease step ‘0’. Flicker Count Increase/Decrease step ‘1’. Flicker Count Increase/Decrease step ‘2’. Flicker Count Increase/Decrease step ‘3’.
FL(1:0)	00 01 10 11	Flicker Tolerance ‘0’ Flicker Tolerance ‘1’ Flicker Tolerance ‘2’ Flicker Tolerance ‘3’

(69-70) Regclk167

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
45h	x	x	x	x	x	x	0	1	RW
46h	0	1	0	1	1	1	1	1	RW

Default : 45h=01h, 46h = 5Fh

Description :

# of Master clock for flicker detection standard time or 1.667 ms time ratio

Regclk167 = 1.667ms / (master clock period x 256)

(71-74) Flicker Free Mode Period

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
47h	0	0	0	0	0	0	0	1	RW
48h	0	0	1	0	1	1	0	0	
49h	0	0	0	0	0	0	0	0	
4Ah	1	1	1	1	0	1	0	0	

Default : 47h = 01h, 48h = 2Ch, 49h = 00h, 4Ah = F4h

Description :

Address	Name	Function
47h	period50 (H)	Flicker Period Control register for 50Hz light source
48h	period50 (L)	
49h	period60 (H)	Flicker Period Control register for 60Hz light source
4Ah	period60 (L)	

Refer to the application note for the calculation method of flicker free period.

(75) Image Signal Processor control 1 : ISP Control 1

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
4Bh	*RSV*	*RSV*	*RSV*	*RSV*	CCE	*RSV*	*RSV*	*RSV*	RW
	1	1	0	1	1	1	0	1	

Default : 4Bh = DDh

Description :

Bit name	value	Description
CCE	0	Color Correction Disable.
	1	Color Correction Enable. *(default)*

(76) Image Signal Processor control 2 : ISP Control 2

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
4Ch	CEN	OCF2	OCF1	OCF0	ODF3	ODF2	ODF1	ODF0	RW
	0	0	0	0	0	0	0	0	

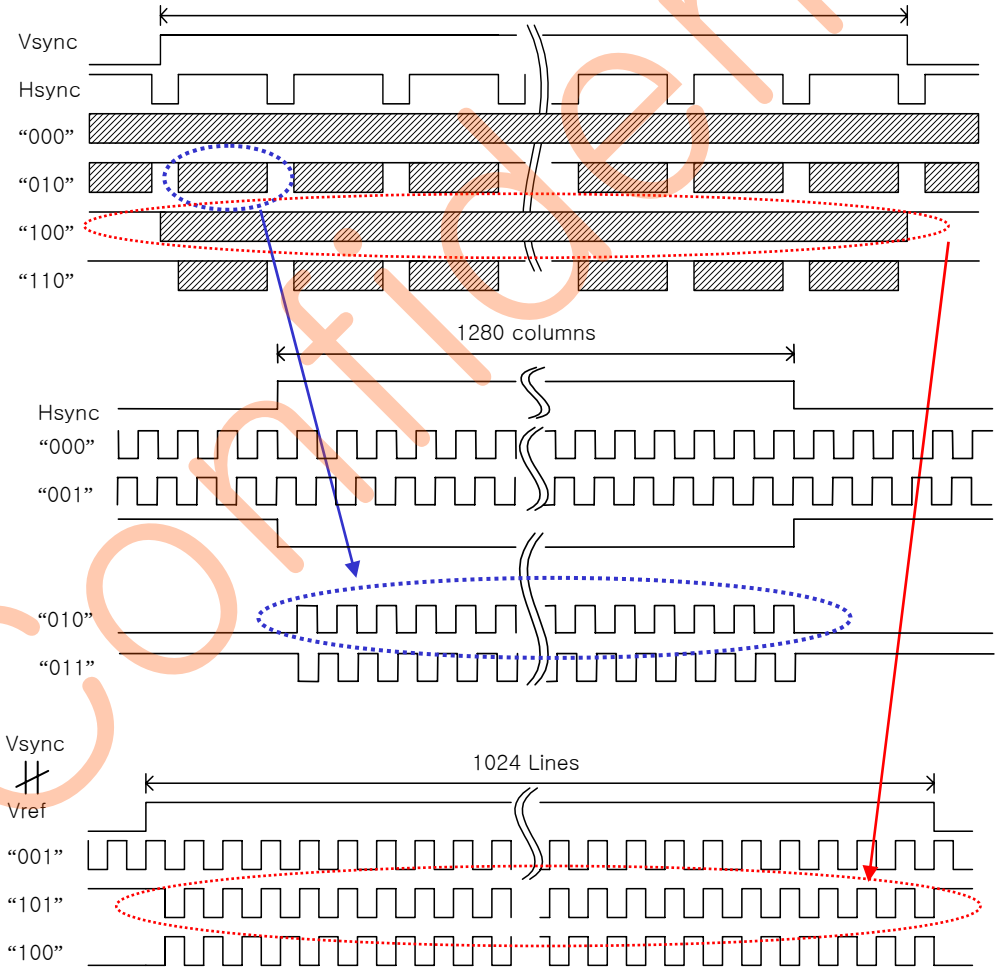
Default : 4Ch = 00h

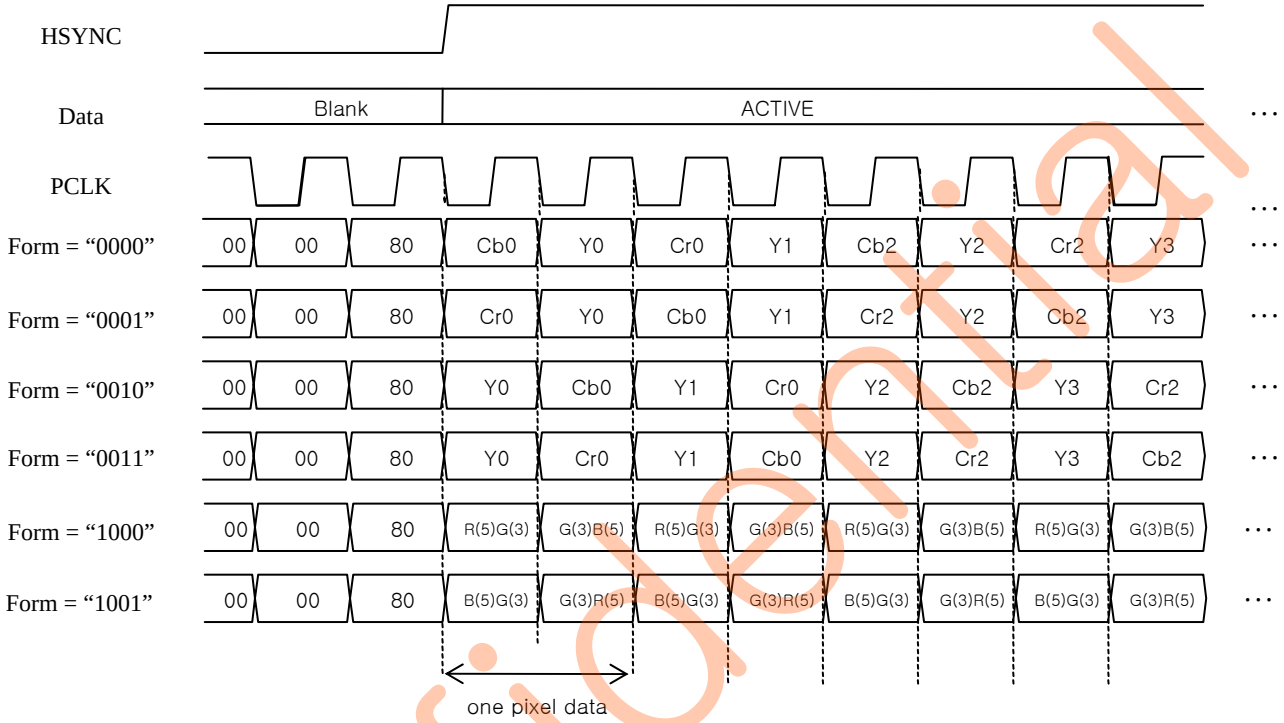
Description :

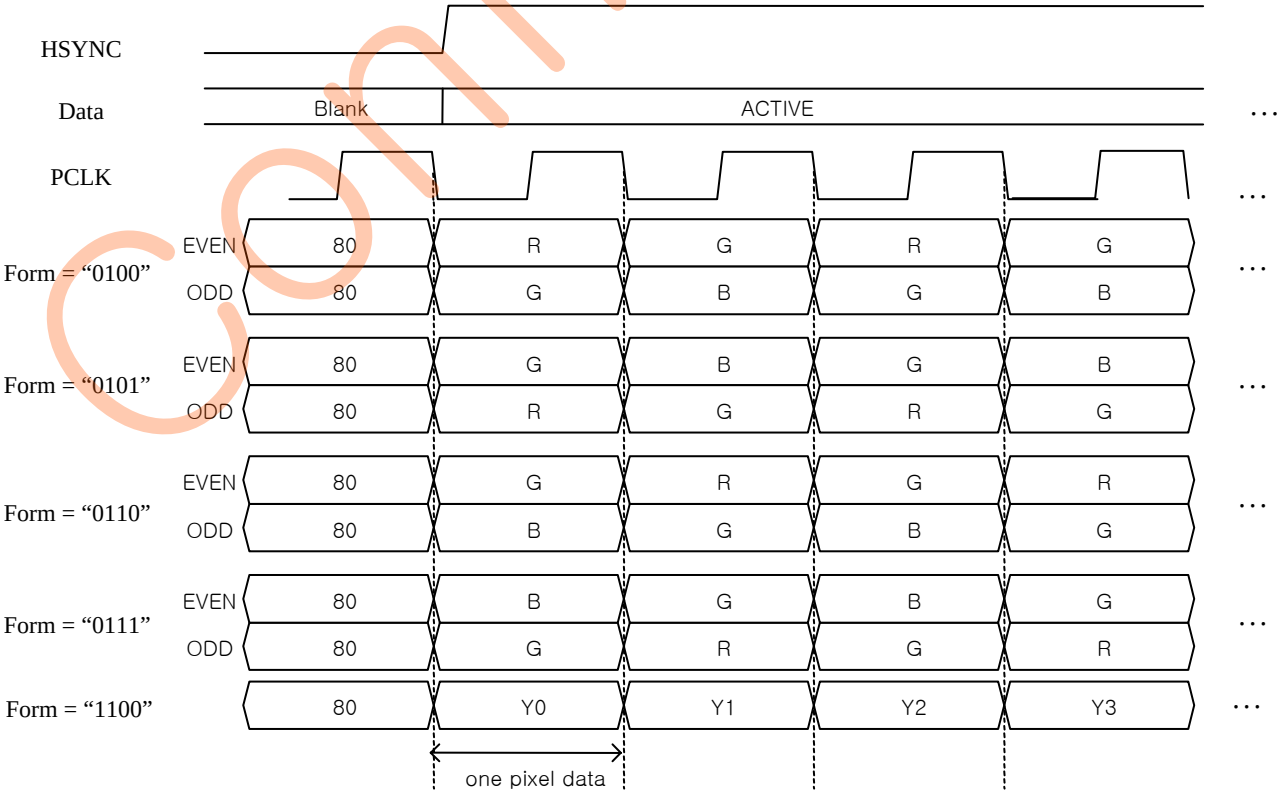
Bit name	value	Description
CEN	0	Normal condition. *(default)*
	1	Out Clock set to ground.
OCF[6:4]		Out Clock format Control
	000	Normal. *(default)*
	001	Invert.
	010	& H-ref
	011	invert & H-ref
	100	& V-ref
	101	invert & V-ref
	110	& H-ref & Vref
	111	invert & H-ref & V-ref
ODF[3:0]		Out Data Format
	0000	CB Y CR Y … *(default)*
	0001	CR Y CB Y …
	0010	Y CB Y CR …
	0011	Y CR Y CB…
	0100	RGRG…GBGB …
	0101	GBGB…RGRG …
	0110	GRGR…BGBG …
	0111	BGBG…GRGR …
	1000	R5G3, G3B5
	1001	B5G3, G3R5
	1010	R8G4,G4B8
	1011	B8G4,G4B8
	1100	YYYY...

- OCF[6:4] : Out Clock Format

PCLK		Description
Normal type	Complementary type	
000 (default)	001	Normal Clock
010	011	Valid in Hsync high.
100	101	Valid in Active Window.
110	111	Valid in Active Window and Hsync high.







(77) Image Signal Processor control 3 : ISP Control 3

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
4Dh	SCE	*RSV*	Vpol	Hpol	HD	*RSV*	*RSV*	*RSV*	RW
	0	0	0	0	1	0	1	0	

Default : 4Dh = 0Ah

Description :

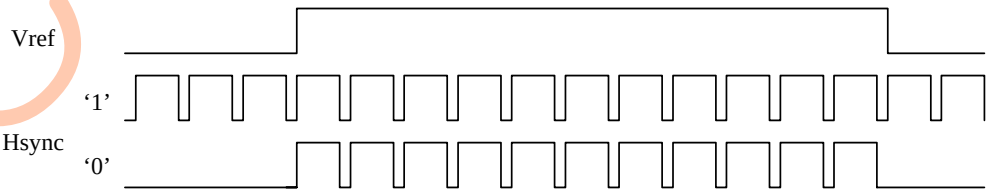
Bit name	value	Description
SCE	0 1	Sepia Color Disable. *(default)* Sepia Color Enable.
Vpol	0 1	VSYNC. *(default)* Invert VSYNC
Hpol	0 1	HSYNC. *(default)* Invert HSYNC
HD	0 1	Only Active region HSYNC All region HSYNC *(default)*

(1) SCE : sepia color : Cb = Reg. Cb Tone (9Ch), Cr = Reg. Cr Tone(9Dh) -> before Color Gain effect

(2) Vpol : VSYNC polarity.

(3) Hpol : HSYNC polarity.

(4) HD



(78) Image Signal Processor control 4 : ISP Control 4

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
4Eh	Hiz	SHiz	FY	FC	aTP	RGE	GGE	BGE	RW
	0	1	1	1	0	0	0	0	

Default : 4Eh = 70h

Description :

Bit name	value	Description
Hiz	0 1	Normal condition *(default)* Out PAD set to Hi-z condition.
SHiz	0 1	Don't care STDBY in Hi-z condition Out Pad set to Hi-z condition @ STDBY '1'
FY	0 1	Y Data range are 16 to 235 Y Data range are 1 to 254 *(default)*
FC	0 1	CbCr Data range are 16 to 240 CbCr Data range are 1 to 254 *(default)*
aTP	0 1	Activated Test pattern disable. *(default)* Activated Test pattern enable.
RGE	0 1	Red Gamma operation Enable. *(default)* Red Gamma operation Disable.
GGE	0 1	Green Gamma operation Enable. *(default)* Green Gamma operation Disable.
BGE	0 1	Blue Gamma operation Enable. *(default)* Blue Gamma operation Disable.

StdbyHiz (SHiz)	Hiz	Stdby	Out PAD condition
1	-	0 1	Normal Hi-Z
-	1	-	Hi-Z
0	1 0	-	Hi-Z Normal

(86-88) Lens Shading Gain (RGB)

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
56h	x	x	x	x	0	0	0	0	
57h	x	x	x	x	0	0	0	0	RW
58h	x	x	x	x	0	0	0	0	

Default : 56h = 00h, 57h = 00h, 58h = 00h

Description :

Address	Name	Description
56h	LensRgain	Lens Gain for Red Pixel
57h	LensGgain	Lens Gain for Green Pixel
58h	LensBgain	Lens Gain for Blue Pixel

(89) Edge Gain

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
59h	*RSV*	*RSV*	*RSV*	0	1	1	0	0	RW

Default : 59h = ACh

Description :

Edge enhancement gain

	Description
EdgeControl[4:0]	Edge enhancement gain

(90) Edge Threshold

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
5Ah	0	0	0	0	0	0	1	0	RW

Default : 5Ah = 02h

Description :

Edge Enhancement threshold.

(115-126) Gamma Correction Coefficients

Address	Name	Value
73h	GC0	0 0 0 0 0 0 0 0 (00h)
74h	GC1	0 0 0 1 1 0 1 0 (1Ah)
75h	GC2	0 0 1 0 1 0 1 0 (2Ah)
76h	GC3	0 0 1 1 0 1 1 1 (37h)
77h	GC4	0 1 0 0 0 0 1 0 (42h)
78h	GC5	0 1 0 1 0 1 1 0 (56h)
79h	GC6	0 1 1 0 1 0 0 0 (68h)
7Ah	GC7	1 0 0 0 0 1 1 1 (87h)
7Bh	GC8	1 0 1 0 0 0 1 1 (A3h)
7Ch	GC9	1 0 1 1 1 1 0 0 (BCh)
7Dh	GC10	1 1 0 1 0 1 0 0 (D4h)
7Eh	GC11	1 1 1 0 1 0 1 0 (EAh)

Default : 00h, 1Ah, 2Ah, 37h, 42h, 56h, 68h, 87h, A3, BCh, D4h, EAh

Description :

Related Register : Gamma Control (0xD6) bit7 | bit6 = Gamma Coefficient Selector

"00" : Address 0x73 ~ 0x7E is Red Data Gamma Coefficient

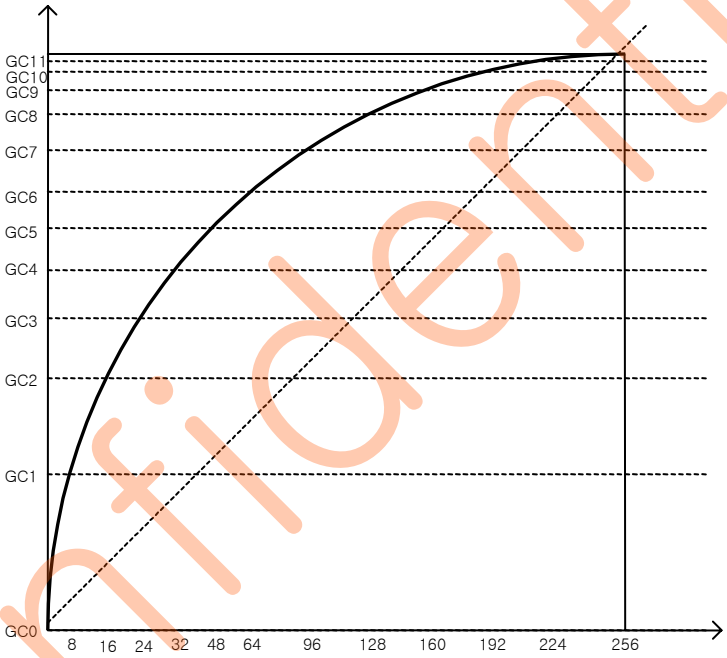
"01" : Green Data Gamma Coefficient

else : Blue Data Gamma Coefficient

Description :

Gamma Correction is applied to RGB signal which ranges from 0 to 255 to compensate non-linear characteristics of display brightness vs input brightness.

Common Gamma Coefficient(GC)



(139-147) Color Correction Coefficient

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
8Bh	0	0	1	1	1	0	0	0	RW
8Ch	1	0	1	0	0	1	0	1	
8Dh	0	0	0	0	1	1	0	1	
8Eh	1	0	0	1	0	0	1	1	
8Fh	0	0	1	0	1	1	0	1	
90h	0	0	0	0	0	1	1	0	
91h	1	0	0	0	0	0	1	1	
92h	1	0	1	0	1	0	1	0	
93h	0	1	0	0	1	1	0	1	

Default : 38h, A5h, 0Dh, 93h, 2Dh, 06h, 83h, AAh, 4Dh

Description :

Address	Name	Function
8Bh	*CCMC0*	Color Correction Matrix Coefficient, ***m00***
8Ch	*CCMC1*	Color Correction Matrix Coefficient, ***m01***
8Dh	*CCMC2*	Color Correction Matrix Coefficient, ***m02***
8Eh	*CCMC3*	Color Correction Matrix Coefficient, ***m10***
8Fh	*CCMC4*	Color Correction Matrix Coefficient, ***m11***
90h	*CCMC5*	Color Correction Matrix Coefficient, ***m12***
91h	*CCMC6*	Color Correction Matrix Coefficient, ***m20***
92h	*CCMC7*	Color Correction Matrix Coefficient, ***m21***
93h	*CCMC8*	Color Correction Matrix Coefficient, ***m22***

- Color Coefficient : sign[7] | integer [6:5] | fractional [4:0]

CC Coefficient

$$\begin{pmatrix} 1.739627 & -1.14441 & 0.404786 \\ -0.60387 & 1.413677 & 0.190193 \\ -0.10247 & -1.30942 & 2.411888 \end{pmatrix} \times 32 = \begin{pmatrix} 55.66805 & -36.6212 & 12.95316 \\ -19.3239 & 45.23768 & 6.08619 \\ -3.27892 & -41.9015 & 77.18042 \end{pmatrix} = \begin{pmatrix} 38 & A5 & 0D \\ 93 & 2D & 06 \\ 83 & AA & 4D \end{pmatrix}$$

(148-149) Color Gain

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
94h	0	0	1	0	0	1	0	1	RW
95h	0	0	1	0	0	1	0	1	

Default : 94h = 25h, 95h = 25h

Description :

Color Gain = Sign[7] | Integer[6:5] | fractional[4:0]

Address	Name	Value
94h	CG11C	0 0 1 0 0 1 0 1 (25h)
95h	CG22C	0 0 1 0 0 1 0 1 (25h)

$Cb' = Cb * CG11C$

$Cr' = Cr * CG22C$

(152-153) Brightness & Contrast

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
98h	0	0	0	0	0	0	0	0	RW
99h	1	0	0	1	0	1	1	0	

Default : 98h = 00h, 99h = 96h

Description :

Y' = Y x (Y_cont/128) + Y_bright

* Brightness(98h) : (bit7) | (bit6 ~ bit0) = sign digit | magnitude

Address	Name	Value
98h	Brightness	0 0 0 0 0 0 0 0 (00h)
99h	Contrast	1 0 0 1 0 1 1 0 (96h)

(156-157) Cb Tone / Cr Tone

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
9Ch	1	0	0	0	0	0	0	0	RW
9Dh	1	0	0	0	0	0	0	0	

Default : 9Ch = 80h, 9Dh = 80h

Description :

Cb /Cr Color tone @ sepia color condition.(reg 4Dh[7])

Address	Name	Value
9Ch	Cb tone	1 0 0 0 0 0 0 0 (80h)
9Dh	Cr tone	1 0 0 0 0 0 0 0 (80h)

(158-161) CCIR656 Sync Index Value

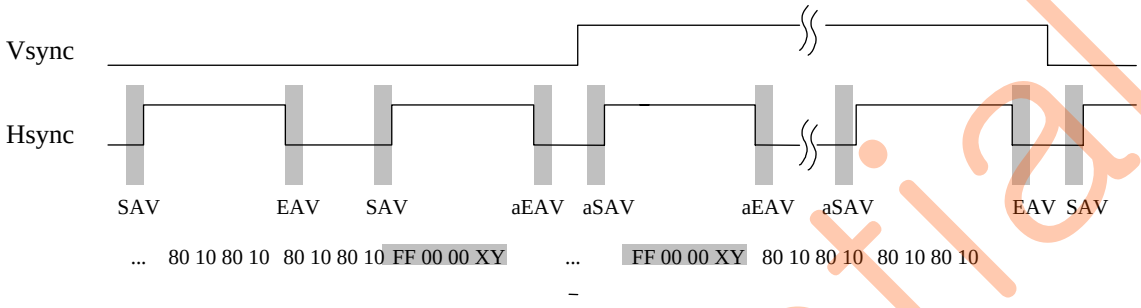
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
9Eh	1	0	1	1	0	1	1	0	RW
9Fh	1	0	0	1	1	1	0	1	
A0h	1	0	1	0	1	0	1	0	
A1h	1	0	0	0	0	0	0	0	

Default : B6h, 9Dh, ABh, 80h

Description :

EAV and SAV signals are inserted for synchronization purposes.

Address	Name	Description
9Eh	*BlankEAV*	Blank Range End of Video
9Fh	*ActiveEAV*	Active Range End of Video
A0h	*BlankSAV*	Blank Range Start of Video
A1h	*ActiveSAV*	Active Range Start of Video



EAV : blank EAV, SAV : blank SAV
aEAV : Active EAV, aSAV : Active SAV

(162-167) Pad Vsync Start / Stop

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
A2h	0	0	0	0	0	0	0	0	RW
A3h	0	0	0	0	1	1	0	1	
A4h	0	0	0	0	0	1	0	0	
A5h	0	0	0	0	1	1	0	1	
A6h	0	0	0	0	0	0	0	0	
A7h	0	1	1	0	1	1	1	0	

Default : 00h, 0Dh, 04h, 0Dh, 00h, 6Eh

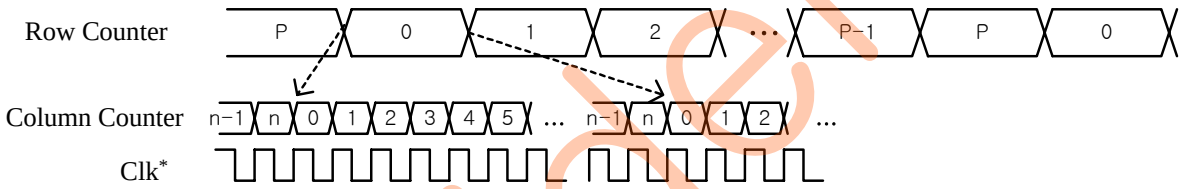
Description :

VSYNC positions.

There are two counters to indicate the present coordinate of frame scanning :

Frame row counter and frame column counter. Counter values repeat the cycle of 0 to *Frame Height* , and 0 to *Frame Width* respectively.

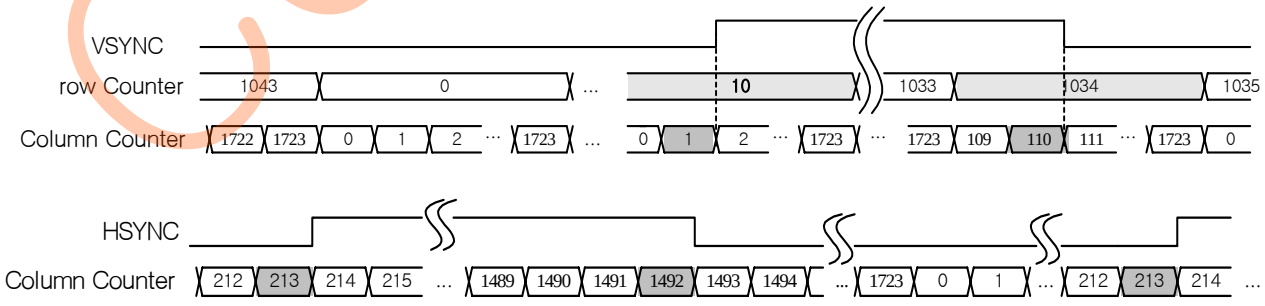
Address	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
A2h	*VsyncStart (H)*	0	0	0	0	0	0	0	0	(00h)
A3h	*VsyncStart (L)*	0	0	0	0	1	1	0	1	(0Dh)
A4h	*VsyncStop (H)*	0	0	0	0	0	1	0	0	(04h)
A5h	*VsyncStop (L)*	0	0	0	0	1	1	0	1	(0Dh)
A6h	*VsyncColumn (H)*	0	0	0	0	0	0	0	0	(00h)
A7h	*VsyncColumn (L)*	0	1	1	0	1	1	1	0	(6Eh)



P = reg. Frame Height
n = reg. Frame Width
CLK* : Clock for Bayer Data

VSYNC rising : when (Row_counter = Reg. VsyncStart) & (Column_counter = Reg. VsyncColumn)
falling : when (Row_counter = Reg. VsyncStop) & (Column_counter = Reg. VsyncColumn)

(For example) VsyncStart = 10d, VsyncStop = 1034d, VsyncColumn = 110d.
Frame Width(reg.04h, 05h) = 1723d, Frame Height(reg.06h, 07h) = 1043d,
Window X1(reg. 08h, 09h) = 213d, Window X2(reg.0Ch, 0Dh) = 1492d.
Then VSYNC & HSYNC is



(170) Weight Window (WW) Control

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
AAh	CW3	CW2	CW1	CW0	*RSV*	*RSV*	*RSV*	*RSV*	RW
	1	0	0	1	1	1	1	1	

Default : AAh = 9Fh

Description :

Bit name	value	Description
CW[3:0]	1001	Weight (Back Light compensation)

(171) AWB / AE Tolerance

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
ABh	0	0	1	0	0	0	1	0	RW

Default : ABh = 22h

Description :

[7 : 4] Set margin of AWB functions

[3 : 0] Set margin of AE functions

(172) AE speed

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
ACh	1	0	0	1	1	1	0	0	RW

Default : ACh = 9Ch

Description :

AE speed[3:0] : "*Ae Speed Gain factor B*" AE speed applied when exposure time is decreasing.

AE speed[7:4] : "*Ae Speed Gain factor D*" AE speed applied when exposure time is increasing.

(173-175) Exposure

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
ADh	0	0	0	0	0	0	0	0	
AEh	1	0	0	0	0	0	0	0	RW
AFh	0	0	0	0	0	0	0	0	

Default : ADh = 00h, AEh = 80h, AFh = 00h

Exposure[23:0] : "*Exposure*" register means abstract exposure level of sensor. Larger the value of *Exposure*, effectively longer exposure time. LSB of *Exposure* corresponds to 1/64 line exposure time. User can write *Exposure* register only when AE function is disabled.

(176) Reference Exposure

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
B0h	0	1	1	1	0	0	0	0	RW

Default : B0h = 70h

Description :

Address	Name	Function
B0h	*TargetExp*	Target exposure level in auto-exposure mode

TargetExp determines target average brightness (Y target) for AE function. AE function controls Exposure register until captured image has brightness of target average brightness. The relationship between *TargetExp* and target average brightness is

target average brightness = TargetExp

(182-183) Maximum Frame Height

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
B6h	0	0	0	0	1	0	0	0	RW
B7h	0	0	1	0	0	1	1	0	

Default : B6h = 08h, B7h = 26h

Description :

Address	Name	Function
B6h	*MaxFrmHeight (H)*	Maximum Frame Height
B7h	*MaxFrmHeight (L)*	

During auto exposure mode, minimum frame rate is set by *MaxExpTime* register. If user set the *MaxExpTime* register larger value than *FrmHeight* register value so that *ExpTime* register have larger value than default(0413h), frame rate is automatically varied.

(184-185) Maximum Exposure

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
B8h	0	0	0	1	0	0	0	0	RW
B9h	0	1	0	0	1	1	0	0	

Default : B8h = 10h, B9h = 4Ch

Description :

Address	Name	Function
B8h	*MaxExp (H)*	Maximum Exposure
B9h	*MaxExp (M)*	

During auto exposure mode, maximum global gain is set by *MaxExp* register. If user set the *MaxExp* register larger value than *MaxFrmHeight* register value, global gain is automatically varied.

(186-187) Minimum Exposure Time

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
BAh	0	0	0	0	0	0	0	0	RW
BBh	0	0	0	0	1	1	0	0	

Default : BAh = 00h, BBh = 03h

Description :

Address	Name	Function
BAh	*MinExpTime (H)*	Minimum Exposure Time
BBh	*MinExpTime (L)*	

Under auto exposure mode, minimum exposure time is set by *MinExpTime* register. LSB of *MinExpTime* corresponds to time for reading 1/64 line in each frame.

(190-193) Minimum / Maximum AWB Gain

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
BEh	0	0	0	1	0	0	0	0	RW
BFh	1	1	1	0	0	0	0	0	
C0h	0	0	0	1	0	0	0	0	
C1h	1	1	1	0	0	0	0	0	

Default : BEh = 10h, BFh = E0h, C0h = 10h, C1h = E0h

Description :

During auto white balance, *RedGain* and *BlueGain* register value varies between *MinAWB* and *MaxAWB*

Address	Name	Function
BEh	*Red Min Gain AWB*	0 0 0 1 0 0 0 0
BFh	*Red Max Gain AWB*	1 1 1 0 0 0 0 0
C0h	*Blue Min Gain AWB*	0 0 0 1 0 0 0 0
C1h	*Blue Max Gain AWB*	1 1 1 0 0 0 0 0

(194-195) AWB RG / BG ratio

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
C2h	1	0	0	0	0	0	0	0	RW
C3h	1	0	0	0	0	0	0	0	

Default : C2h = 80h, C3h = 80h

Description :

Address	Name	Function
C2h	*AWB RG ratio*	AWB Color Ratio
C3h	*AWB BG ratio*	

Red Gm = Gm x AWB RGratio

Blue Gm = Gm x AWB BGratio

(AWB RG / BG ratio x1 = 80h)

(196-203) Weighting Window

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
C4h	0	0	0	0	0	0	1	0	RW
C5h	0	1	1	0	0	1	1	1	
C6h	0	0	0	0	0	1	0	0	
C7h	0	0	1	0	0	1	0	1	
C8h	0	0	0	0	0	0	0	1	
C9h	0	1	0	1	1	1	0	1	
CAh	0	0	0	0	0	0	1	0	
CBh	1	0	1	1	0	0	1	1	

Default : 02h, 67h, 04h, 25h, 01h, 5Dh, 02h, B3h

Description : Refer to the description of WW bit of WW *Control* [AAh].

WeightX1 = 0x0267h, *WeightX2*= 0x0425h, *WeightY1* = 0x015Dh, *WeightY2* = 0x02B3h

WeighteX1 > 615d, *WeightedX2* < 1061d

WeighteY1 > 349d, *WeightedY2* < 691d

Address	Name	Function
C4h	*WeightX1 (H)*	X1 coordination of weight window of auto-exposure process
C5h	*WeightX1 (L)*	
C6h	*WeightX2 (H)*	X2 coordination of weight window of auto-exposure process
C7h	*WeightX2 (L)*	
C8h	*WeightY1 (H)*	Y1 coordination of weight window of auto-exposure process
C9h	*WeightY1 (L)*	
CAh	*WeightY2 (H)*	Y2 coordination of weight window of auto-exposure process
CBh	*WeightY2 (L)*	

(209) Auto Control

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
D1h	x	x	AWBen	AEen	*RSV*	*RSV*	*RSV*	*RSV*	RW
	x	x	1	1	1	1	0	0	

Default : D1h = 3Ch

Description :

Mnemonic	Description
AWBen	AWB enable
AEen	AE enable

(213) PLL Control

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
D5h	PLLs1	PLLs0	*RSV*	*RSV*	SC1	SC0	*RSV*	*RSV*	RW
	0	0	0	0	1	1	0	0	

Default : D5h = 30h

Description :

Bit name	value	Description
PLLs[1:0]		PLL Selector
	00	PLL stdby
	01	x2
	10	x3
	11	x4
SC[1:0]		Selector Blank Data
	00	CCIR656 Data
	01	FFF
	10	000
	11	A50

(214) GammaSelect

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
D6h	GCS1	GCS0	*RSV*	*RSV*	*RSV*	*RSV*	*RSV*	*RSV*	RW
	0	0	1	0	1	0	0	1	

Default : D6h = 29h

Description :

Bit name	value	Description
GCS[1:0]		Gamma Coefficient(GC) select (0x73 ~ 0x7E)
	00	Red GC
	01	Green GC
	Else	Blue GC

Electrical Characteristics

Absolute Maximum Ratings *

HVDD Supply Voltage ---------- −0.3V to 4.5V
AVDD,DVDD Supply Voltage ---------- −0.3V to 2.5V
DC Voltage at any input pin ---------- −0.3V to HVDD+0.3V
DC Voltage at any output pin ---------- −0.3V to HVDD+0.3V
Operation Temperature ---------- −30 °C to + 70 °C
Performance Temperature ---------- −30 °C to + 50 °C
Storage Temperature ---------- −40°C to + 125°C

Table 4. DC Characteristics

Symbol	Descriptions	Min	Typ	Max	Unit
V_{DD}	Digital, Analog, Pixel VDD voltage relative to GND(DGND, AGND, PGND) level.	1.62	1.8	1.98	V
HV_{DD}	High VDD(HVDD) voltage relative to GND(DGND) level.	1.62	1.8 2.5 3.3	3.6	V
I_{DDD}	Supply current at 7.5 fps. Currents are programmable through I2C serial interface. (V_{DD} : 1.8V, HV_{DD} : 1.8V ~ 3.3V, MCLK : 27MHz)		33	45	mA
	Supply current at 7.5 fps. Currents are programmable through I2C serial interface. (V_{DD} : 1.98V, HV_{DD} : 3.6V, MCLK : 27MHz)		40	55	
I_{DDS}	Standby supply current		10	20	uA
V_{IL1}	Input voltage LOW level			0.2*HVDD	V
V_{IH1}	Input voltage HIGH level	0.8*HVDD			V
V_{IL2}	Input voltage LOW level for SCL, SDA.			0.2*HVDD	V
V_{IH2}	Input voltage HIGH level for SCL, SDA.	0.8*HVDD			V
C_{IN}	Input pin capacitance			10	pF
V_{OL1}	Output Voltage LOW			0.1*HVDD	V
V_{OH1}	Output Voltage HIGH	0.9*HVDD			V
V_{OL2}	Output Voltage LOW level for SCL, SDA.			0.2	V
V_{OH2}	Output Voltage HIGH level for SDA.	HVDD-0.2			V
I_{IN}	Input leakage current		0.005	1	uA
Iot	Output leakage current		0.005	1	uA

* CAUTION !! : Excessive stresses may cause permanent damage to the device.

Table 5. AC Characteristics (Cout = 16pF, HVDD = 2.5V, MCLK = 27MHz, Output Format = YUV422)

Symbol	Descriptions	Min	Typ	Max	Unit
f_{MCLK}	Master clock Frequency	-	27	54	MHz
duty	Master clock duty cycle	45	50	55	%
t1	Master clock rise/fall time	0.5	5	10	ns
t2	PCLK rise/fall time	1.5	5	10	ns
t3	PCLK rising edge to HSYNC	14	19	24	ns
t4	PCLK rising edge to digital output	18	23	28	ns
t5	MCLK rising edge to PCLK rising edge	12	17	22	ns

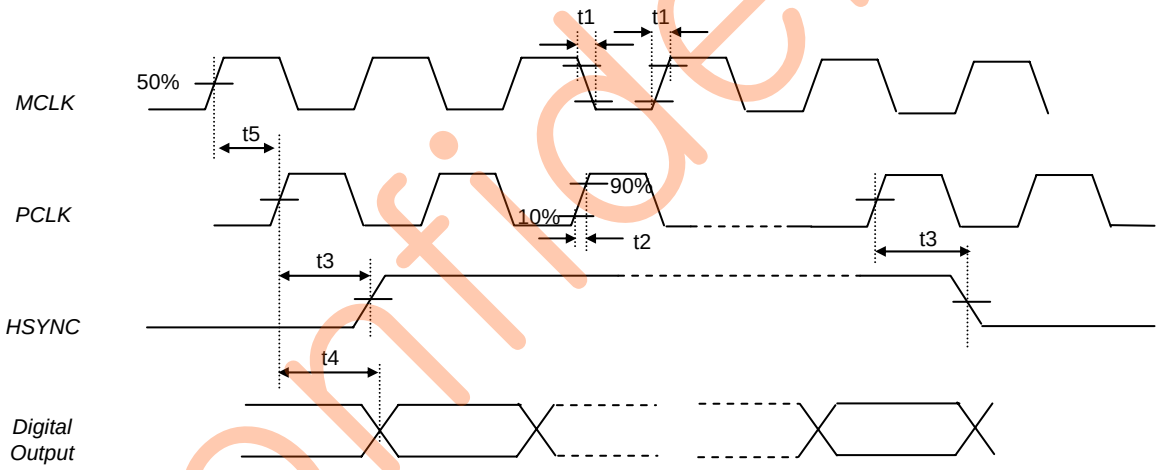
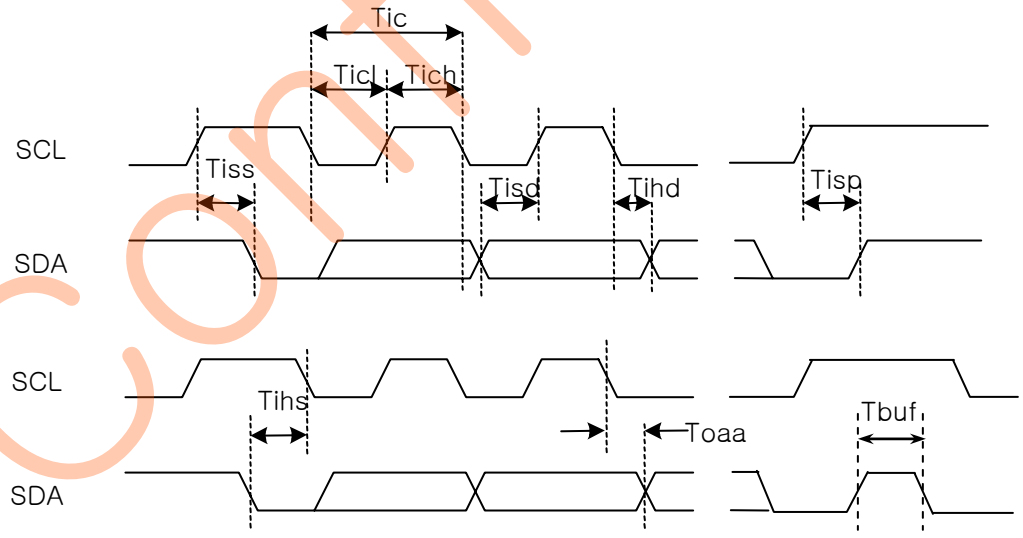


Fig. 14 Timing diagram of Clock, DATA, and HSYNC

Table 6. I2C bus signal timing

Symbol	Descriptions	Min	Max	Unit
Tic	I2C Clock frequency		400	kHz
Ticl	I2C Clock Low period	1.3		us
Tich	I2C Clock High period	600		ns
Tiss	setup time for start condition	600		ns
This	hold time for start condition	600		ns
Tisd	setup time for input data	300		ns
Tihd	hold time for input data	50		ns
Tisp	setup time of stop condition	600		ns
Tbuf	Bus free time between a stop and start condition	1.3		us
Toaa	Output delay time		70	ns
Tr	Input rising time		300	ns
Tf	Input falling time		300	ns



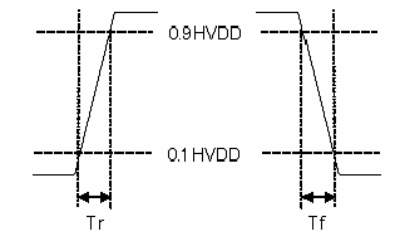
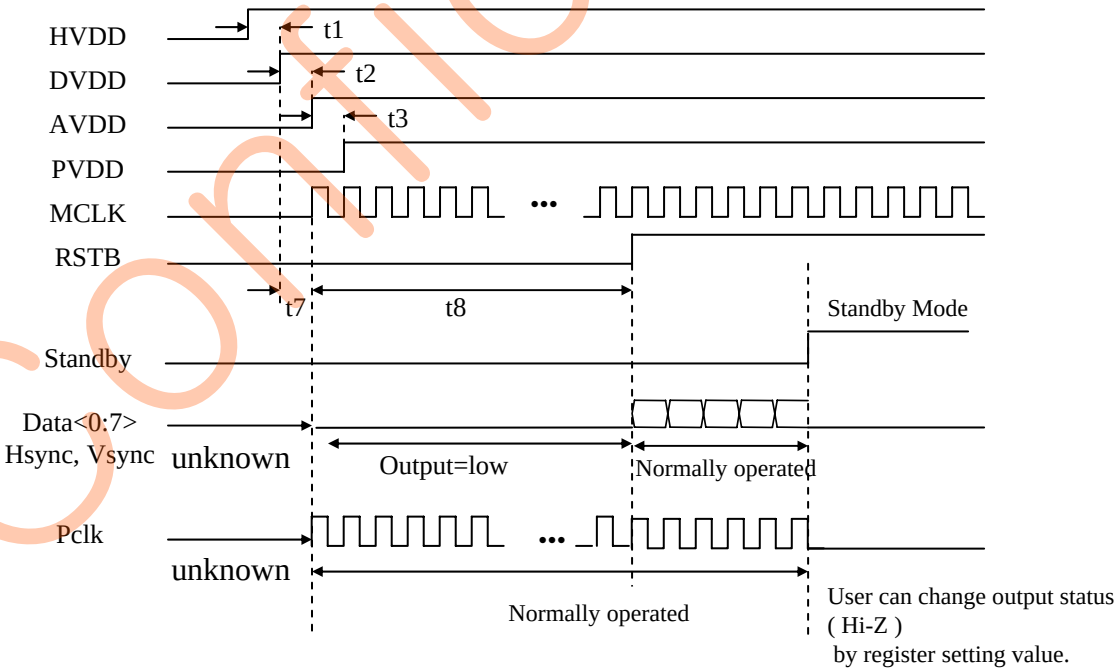


Table 7. Power ON,OFF Sequence

Symbol	Descriptions	Min	Typ	Max	Unit
t1	From HVDD rising to DVDD rising	0	-	100	ns
t2	From DVDD rising to AVDD rising	0	-	100	ns
t3	From AVDD rising to PVDD rising	0	-	100	ns
t4	From PVDD falling to AVDD falling	0	-	100	ns
t5	From AVDD falling to DVDD falling	0	-	100	ns
t6	From DVDD falling to HVDD falling	0	-	100	ns
t7	From DVDD rising to initial mclk rising	0	-	100	ns
t8	Minimum reset time	8 × (*)Tmclk	-	-	-

((*)Tmclk = 1/fmclk, period time of mclk)

Power-On Sequence



Power-Off Sequence

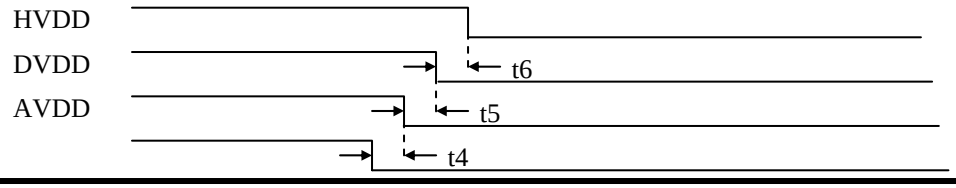


Table 8. Electro- Optical Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Unit
Sens	Sensitivity	1)		1.83		V/Lux.sec
Vsat	Saturation Level	2)		760		mV
Vdrk	Dark Signal	3)		11		mV/sec
PSNU	PIXEL Signal NON-Uniformity	4)		6		%
DR	Dynamic range	5)		56		dB

Notes :

1) Measured sensitivity of Green pixel at 2.3lux illumination for 132ms integration time
2) For λ=550 wavelength
3) Measured at the zero illumination for 132ms at the 40 degree
4) For 16X16 pixel region under illumination with output signal equal to 50% of saturation signal.

$$\frac{\text{Max value of Block} - \text{Min value of Block}}{\text{Average value of all blocks}} \times 100$$

5) For frame rate = 7.5fps, 40 degree
20*Log [Saturation Signal /Dark signal] [dB]

CMOS Image Sensor with 1280 X 1024 Pixel Array and Integrated On-Chip Image Signal Processor

CSP(Chip Scale Package) Specification

Table 9. Package Dimensions

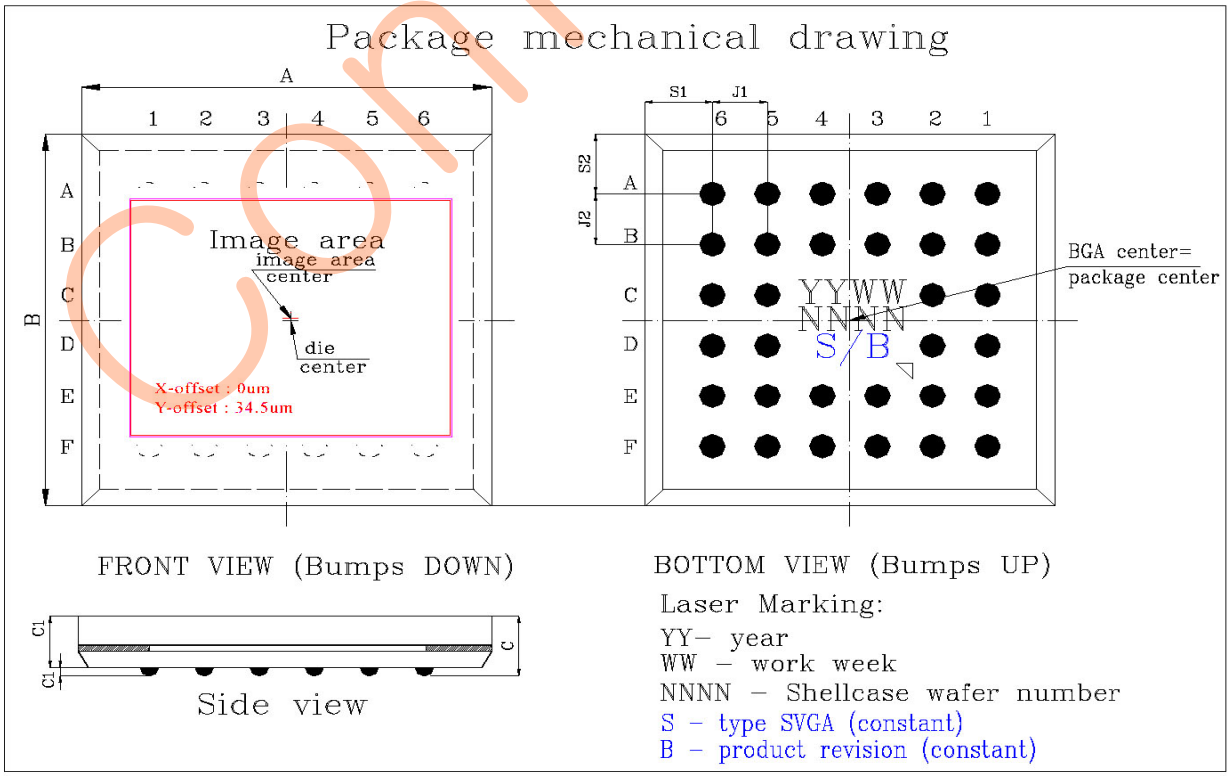
Unit:mm

	Symbol	Normal	Min	Max
Package Body Dimension X	**A**	5.593	5.568	5.618
Package Body Dimension Y	**B**	5.522	5.497	5.547
Package Height	**C**	1.005	0.950	1.065
Package Body Thickness	**C2**	0.840	0.795	0.885
Ball Height	**C1**	0.165	0.140	0.190
Ball Diameter	**D**	0.35	0.320	0.380
Pins Pitch X ,Y axis	**J1,J2**	0.75	.	.
Edge to Ball Center Distance along X	**S1**	0.922	0.892	0.965
Edge to Ball Center Distance along Y	**S2**	0.886	0.856	0.916

	1	2	3	4	5	6
A	STDBY	VREFN	AVDD	DGND-A	DVDD-A	SCL
B	D11	VREFP	AGND	SDA	D7	D6
C	D9	RSTB			D5	D4
D	HVDD	D10			D3	HVDD
E	DGND	D8	DVDD	DGND	PCLK	DVDD
F	MCLK	HSYNC			D2	VSYNC

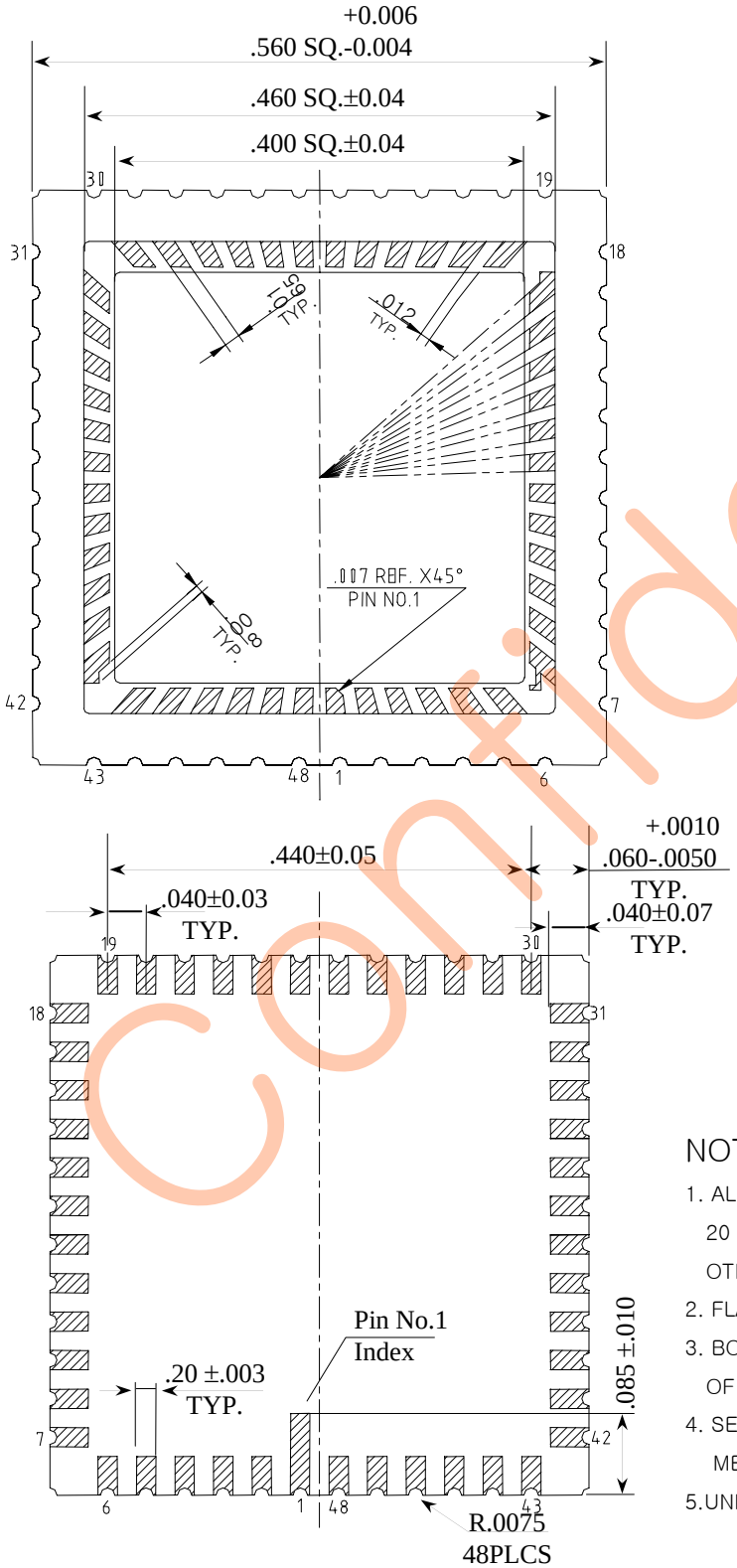
D2~D11 : 10 bit bayer
D4~D11: 8bit YUV

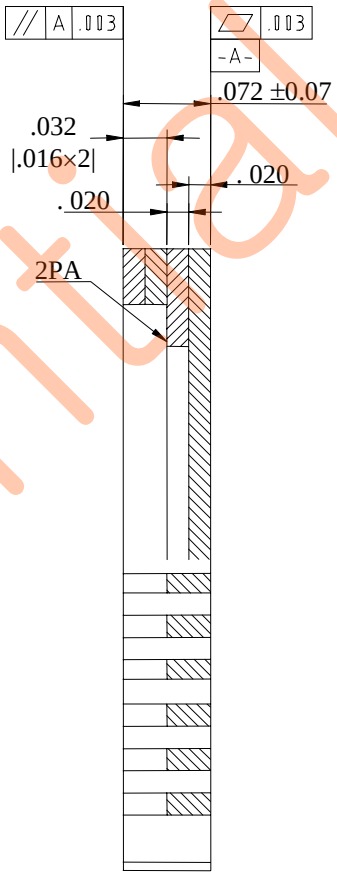
Table 10.Ball matrix



CMOS Image Sensor with 1280 X 1024 Pixel Array and Integrated On-Chip Image Signal Processor

CLCC48Pin Package Specification





NOTES :

1. ALL EXPOSED METALLIZED AREA SHALL BE GOLD PLATED 20 MICRO INCHES MIN. THK. OVER NICKEL PLATE UNLESS OTHERWISE SPECIFIED IN PURCHASE ORDER.
2. FLATNESS PERTAINS TO MATALLIXED PADS ONLY.
3. BOND PAD EDGE SHALL NOT OVER HANG FROM THE EDGE OF THE DIE ATTACH CAVITY.
4. SEAL AREA AND DIE ATTACH AREA SHALL BE WITHOUT METALLIZATION.
5. UNIT:inch

Application Note

- Revision Number

Reg. Addr. (Hex)	Read Value (Hex)	Register Name	Descriptions
02	07	*RevNum*	Revision Number of PO3130R

- Recommended Register Values (Write I2C Addr. : **0xEC**, Read I2C Addr. : **0xED**)

Overview

- The better image can be acquired to set up recommended register value.

(1) Initial Setting

- Basic Setting (Writing Sequence is not important HERE)

Address (Hex)	Recommended value (Hex)	Register Name	Default Value (Hex)	Descriptions
12	**08**	*AmpBias*	02	
1E	**06**	*TgControl2*	0A	
21	**00**	*Reserved*	52	
33	**37**	*Reserved*	3C	
36	**C0**	*Reserved*	30	
37	**C8**	*Reserved*	6C	
3B	**36**	*Reserved*	39	
4B	**FE**	*Reserved*	DD	
51	**1C**	*Reserved*	04	
52	**01**	*Reaerved*	00	
55	**08**	*Reserved*	00	
56	**09**	*LensRGain*	00	
57	**04**	*LensGGain*	00	
58	**03**	*LensBGain*	00	
59	**6F**	*EdgeGain*	AC	
5A	**04**	*EdgeThreshold*	02	
5C	**10**	*Reserved*	03	
5D	**10**	*Reserved*	08	
5E	**10**	*Reserved*	10	
5F	**10**	*Reserved*	1F	

continue…

Address (Hex)	Recommended value (Hex)	Register Name	Default Value (Hex)	Descriptions
61	**00**	*Reserved*	08	
62	**18**	*Reserved*	1B	
63	**30**	*Reserved*	1F	
70	**68**	*Reserved*	70	
80	**80**	*Reserved*	88	
86	**13**	*Reserved*	1F	
87	**18**	*Reserved*	1F	
AA	**3F**	*WWControl*	9F	
AB	**44**	*AETolerance*	22	
B0	**68**	*TergetExp*	70	
B5	**10**	*Reserved*	0F	
B8	**20**	*MaxExp(H)*	10	
B9	**A0**	*MaxExp(L)*	4C	
BC	**04**	*Reserved*	08	
8B	**40**	*ColorMatrix11*	38	Color Matrix
8C	**91**	*ColorMatrix12*	A5	
8D	**8F**	*ColorMatrix13*	0D	
8E	**91**	*ColorMatrix21*	93	
8F	**43**	*ColorMatrix22*	2D	
90	**92**	*ColorMatrix23*	06	
91	**89**	*ColorMatrix31*	83	
92	**9D**	*ColorMatrix32*	AA	
93	**46**	*ColorMatrix33*	4D	

continue…

- Gamma Setting (From Here, Writing sequence is important. Keep the Following Sequence)

Address (Hex)	Recommended value (Hex)	Register Name	Default Value (Hex)	Descriptions
D6	**22**	*GammaSelect*	20	Select R Gamma
73	**00**	*GmCoeff0*	00	R gamma
74	**10**	*GmCoeff1*	1A	
75	**20**	*GmCoeff2*	2A	
76	**2B**	*GmCoeff3*	37	
77	**36**	*GmCoeff4*	42	
78	**49**	*GmCoeff5*	56	
79	**5A**	*GmCoeff6*	68	
7A	**7F**	*GmCoeff7*	87	
7B	**9B**	*GmCoeff8*	A3	
7C	**BA**	*GmCoeff9*	BC	
7D	**D4**	*GmCoeff10*	D4	
7E	**EA**	*GmCoeff11*	EA	
D6	**62**	*GammaSelect*	20	Select G Gamma
73	**00**	*GmCoeff0*	00	G Gamma
74	**10**	*GmCoeff1*	1A	
75	**20**	*GmCoeff2*	2A	
76	**2B**	*GmCoeff3*	37	
77	**36**	*GmCoeff4*	42	
78	**49**	*GmCoeff5*	56	
79	**5A**	*GmCoeff6*	68	
7A	**7F**	*GmCoeff7*	87	
7B	**9B**	*GmCoeff8*	A3	
7C	**BA**	*GmCoeff9*	BC	
7D	**D4**	*GmCoeff10*	D4	
7E	**EA**	*GmCoeff11*	EA	

continue…

Address (Hex)	Recommended value (Hex)	Register Name	Default Value (Hex)	Descriptions
D6	**A2**	*GammaSelect*	20	Select B Gamma
73	**00**	*GmCoeff0*	00	B Gamma
74	**10**	*GmCoeff1*	1A	
75	**20**	*GmCoeff2*	2A	
76	**2B**	*GmCoeff3*	37	
77	**36**	*GmCoeff4*	42	
78	**49**	*GmCoeff5*	56	
79	**5A**	*GmCoeff6*	68	
7A	**7F**	*GmCoeff7*	87	
7B	**9B**	*GmCoeff8*	A3	
7C	**BA**	*GmCoeff9*	BC	
7D	**D4**	*GmCoeff10*	D4	
7E	**EA**	*GmCoeff11*	EA	

 # Above recommended setting includes the following functions

- ***Max.Frame Rate : SXGA 15 fps. @ MCLK = 54 MHz (1x PLL) or 27 MHz (2x PLL)***
- ***Auto Frame Rate Control : Min.Frame Rate = Max.Frame Rate / 2***
- ***Auto Gain Control : Max.Global Gain = 4X***
- ***Output Format : YUV422 (1 ~ 254)***
- ***Weight Window : 3X Center Weight***
- ***VSYNC (positive level), HSYNC (positive level), PCLK (positive edge)***
- ***Pixel Correction, Color Correction, Gamma Correction, AWB, AE***

(2) Additional setting according to the resolution

PO3130R support two sub-sampling methods. (Called as Method 1 and Method 2). Refer to Reg.20h description.

Method 1 gives faster frame rate (Max. 30fps. when MCLK = 27MHz) but worse image quality.

Method 2 gives slower frame rate (Max. 15fps. when MCLK = 54MHz (1x PLL) or 27MHz (2x PLL)) but better image quality.

- SXGA mode (1280x1024)

Address (Hex)	Recommended value (Hex)	Register Name	Default Value (Hex)	Descriptions
20	**44**	*TgContol4*	44	
59	**6F**	*EdgeControl*	AC	

- QSXGA mode (640x512)

(1) Method 1

20	**C4**	*TgContol4*	44	
59	**66**	*EdgeControl*	AC	

(2) Method 2

20	**14**	*TgContol4*	44	
59	**6F**	*EdgeControl*	AC	

-VGA mode (640x480)

- Common

0B	**2D**	*WindowY1(L)*	0D	
0E	**03**	*WindowY2(H)*	04	
0F	**ED**	*WindowY2(L)*	0D	
A3	**2D**	*VSyncStart(L)*	0D	
A4	**03**	*VSyncStop(H)*	04	
A5	**ED**	*VSyncStop(L)*	0D	

(1) Method 1

20	**C4**	*TgContol4*	44	
59	**66**	*EdgeControl*	AC	

(2) Method 2

20	**14**	*TgControl4*	44	
59	**6F**	*EdgeControl*	AC	

- QQSXGA mode (320x256)

(1) Method 1

20	**94**	*TgContol4*	44	
59	**66**	*EdgeControl*	AC	

(2) Method 2

20	**34**	*TgContol4*	44	
59	**6F**	*EdgeControl*	AC	

-QVGA mode (320x240)

- Common

0B	**2D**	*WindowY1(L)*	0D	
0E	**03**	*WindowY2(H)*	04	
0F	**ED**	*WindowY2(L)*	0D	
A3	**2D**	*VSyncStart(L)*	0D	
A4	**03**	*VSyncStop(H)*	04	
A5	**ED**	*VSyncStop(L)*	0D	

(1) Method 1

20	**94**	*TgContol4*	44	
59	**66**	*EdgeControl*	AC	

(2) Method 2

20	**34**	*TgContol4*	44	
59	**6F**	*EdgeControl*	AC	

- CIF mode (352x288)

20	**84**	*TgContol4*	44	
08	**01**	*WindowX1(H)*	00	
09	**0B**	*WindowX1(L)*	D5	
0B	**2D**	*WindowY1(L)*	0D	
0D	**9F**	*WindowX2(L)*	D5	
0E	**03**	*WindowY2(H)*	04	
0F	**ED**	*WindowY2(L)*	0D	
A3	**2D**	*VSyncStart(L)*	0D	
A4	**03**	*VSyncStop(H)*	04	
A5	**ED**	*VSyncStop(L)*	0D	
59	**66**	*EdgeControl*	AC	

- QQVGA mode (160x120)

20	**B4**	*Reserved*	44	
0B	**2D**	*WindowY1(L)*	0D	
0E	**03**	*WindowY2(H)*	04	
0F	**ED**	*WindowY2(L)*	0D	
A3	**2D**	*VSyncStart(L)*	0D	
A4	**03**	*VSyncStop(H)*	04	
A5	**ED**	*VSyncStop(L)*	0D	
59	**66**	*EdgeControl*	AC	

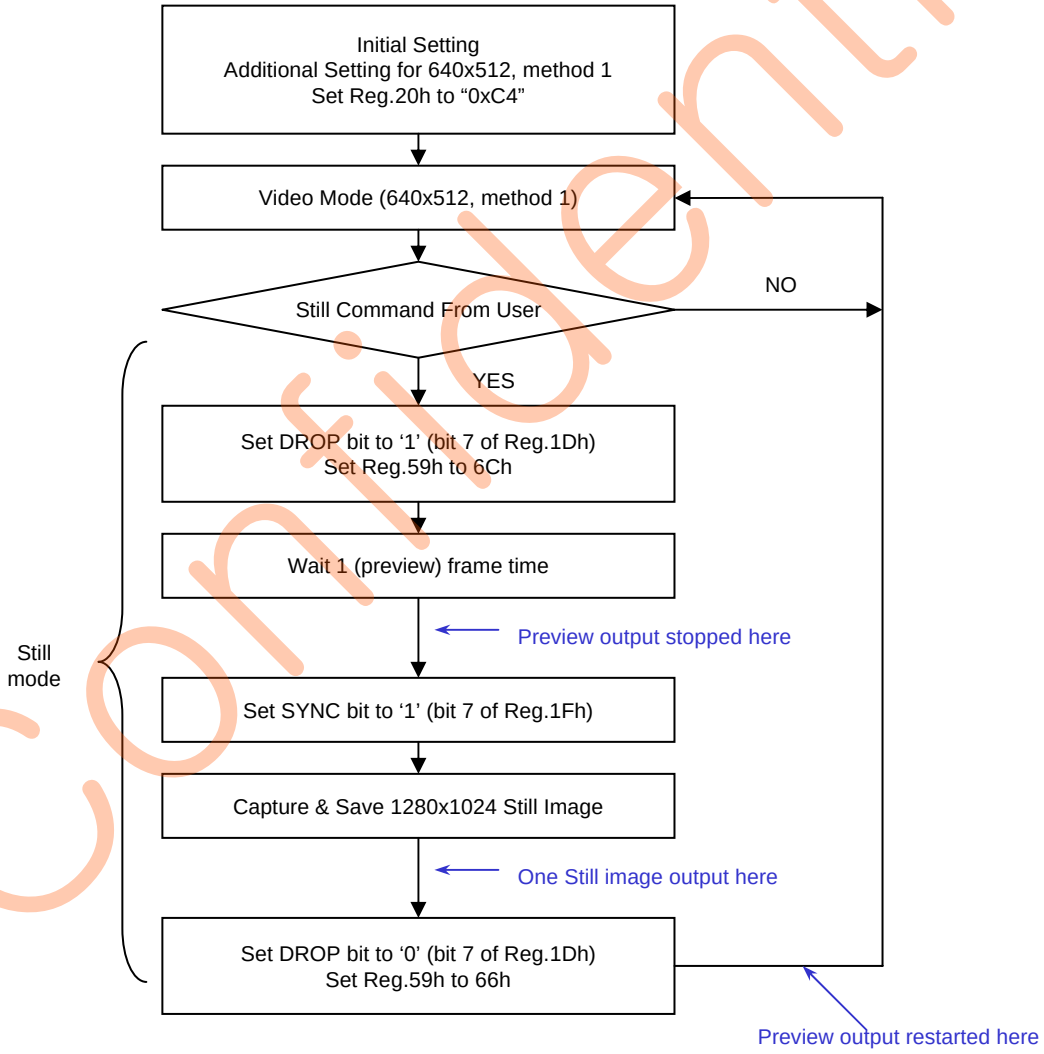
- QCIF mode (176x144)

20	**A4**	*Reserved*	44	
08	**01**	*WindowX1(H)*	00	
09	**0B**	*WindowX1(L)*	D5	
0B	**2D**	*WindowY1(L)*	0D	
0D	**9F**	*WindowX2(L)*	D5	
0E	**03**	*WindowY2(H)*	04	
0F	**ED**	*WindowY2(L)*	0D	
A3	**2D**	*VSyncStart(L)*	0D	
A4	**03**	*VSyncStop(H)*	04	
A5	**ED**	*VSyncStop(L)*	0D	
59	**66**	*EdgeControl*	AC	

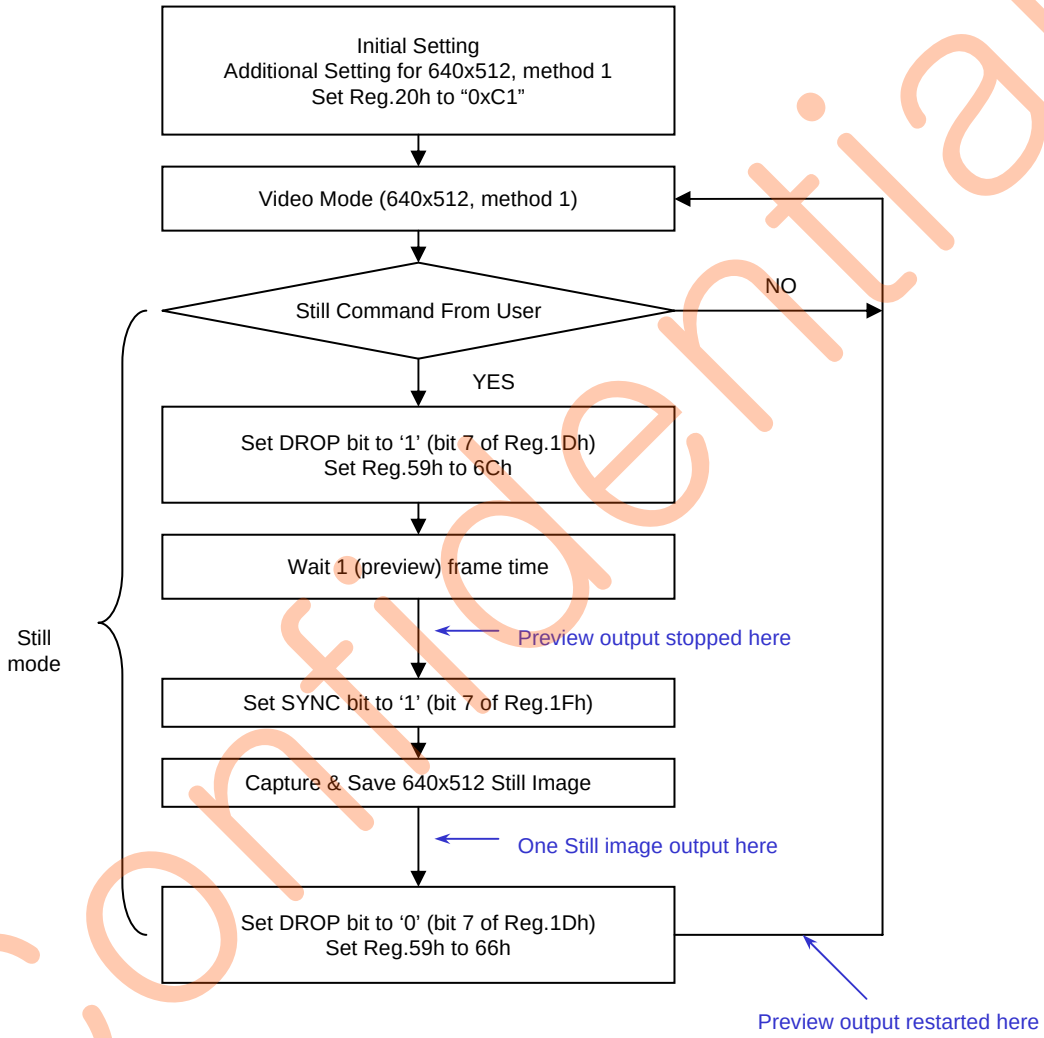
- Still Method

(1) 640x512(preview, method 1) => 1280x1024(still)

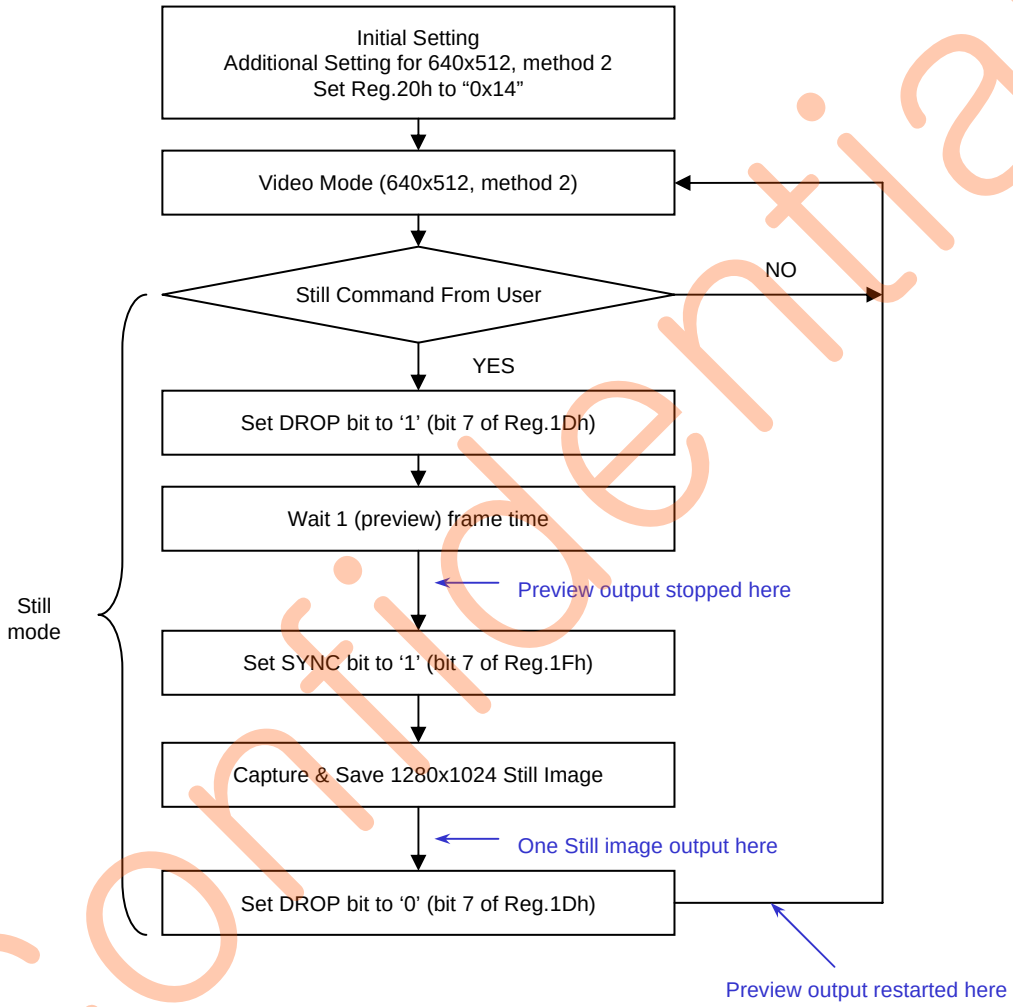
We recommended to use still mode to get still image (1280x1024) while previewing in QSXGA(640x512) mode. Please refer to the datasheet for more information.



(2) 640x512(preview, method 1) => 640x512(still, method 2)



(3) 640x512(preview, method 2) => 1280x1024(still)



- Flicker Free Mode

-Related Registers : Period50H (Reg.47h) ~ Period60L(Reg.4A), FdConrol (Reg.44h)

(1) Manual Flicker Free Mode (50Hz / 60Hz)

Reg. Addr. (Hex)	Register Name	Default Value (Hex)	Appropriate value (Hex)	Descriptions
47	*Period50H*	01	Refer to following example	
48	*Period50L*	2C	,,	
49	*Period60H*	00	,,	
4A	*Period60L*	F4	,,	

Reg. Addr. (Hex)	Register Name	Flicker Off	Flicker On	Descriptions
44	*FdControl*	00	**20 / 40**	60Hz / 50Hz Flicker Free Enable

-Flicker Period Control Register Setting

Related Registers **:** *Reg.47(h), Reg.48(h) – for 50Hz light source.*

Reg.49(h), Reg.4A(h) – for 60Hz light source.

1) CASE 1 : SXGA preview, 1280x1024

Flicker Period Reg. Value (SXGA, 1280x1024) = 64*(MCLK Freq/(Frame Width * 2))/(Flicker Freq.*2)

2) CASE 2 : Method1 QSXGA preview, 640x512

Flicker Period Reg. Value (QSXGA, 640x512) = 4*64*(MCLK Freq/(Frame Width * 2))/(Flicker Freq.*2)

ex) If you're using 24MHz MCLK,

– Flicker Period for 60Hz

Frame Width = 1724 column .

*1) Flicker Period (SXGA) = 64 * (24000000 / (1724 * 2)) / (60 x 2) = 3712 = 0x0E80*

Reg.49(h) = 0x0E; Reg.4A(h) = 0x80;

2) Flicker Period (method1, QSXGA) = 4 64 * (24000000 / (1724 * 2)) / (60 x 2) = 14849 = 0x3A01*

Reg.49(h) = 0x3A; Reg.4A(h) = 0x01;

- Flicker Period for 50Hz

*1) Flicker Period (SXGA) = 64 * (24000000 / (1724 * 2)) / (50 x 2) = 4455 = 0x1167*

Reg.47(h) = 0x11; Reg.48(h) = 0x67;

*2) Flicker Period (method1, QSXGA) = 4 * 64 * (24000000 / (1724 * 2)) / (50 x 2) = 17819 = 0x459B*

Reg.47(h) = 0x45; Reg.48(h) = 0x9B;

** If you use the still mode in the previous section to get SXGA still image while previewing image in QSXGA mode, you use flicker period for QSXGA and don't have to change flicker period before getting SXGA still image.*

(2) Auto Flicker Detection Mode

PO3130R support auto flicker detection mode.

Reg. Addr. (Hex)	Appropriate value	Register Name	Default Value (Hex)	Descriptions
45	(1.667ms * MCLK freq.) / 256	*Regclk167(H)*	01	
46		*Regclk167(L)*	5F	
47	Refer to the example in the previous page.	*Period50H*	01	
48	,,	*Period50L*	2C	
49	,,	*Period60H*	00	
4A	,,	*Period60L*	F4	

Reg. Addr. (Hex)	Flicker On (Hex)	Register Name	Flicker Off (Hex)	Descriptions
44	**8F**	*FdControl*	00	50Hz / 60Hz flicker Auto Detection

- Output Format

Related Registers : ISPControl1 (Reg.4Bh), ISPControl2 (Reg.4Ch), ISPControl4 (Reg.4E), EdgeControl (Reg.59h), Brightness (Reg.98h), Y Contrast (Reg.99h), CG11C (Reg.94h), CG22C (Reg.95h)

1) YCbCr422 (8 Bit, Y range : 16 ~ 235, Cb & Cr range : 16 ~ 240) – CCIR.601

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
4C	**xxxx0000**	*ISPControl2*	00	Cb Y Cr Y…
	xxxx0001			Cr Y Cb Y…
	xxxx0010			Y Cb Y Cr…
	xxxx0011			Y Cr Y Cb…

Reg. Addr. (Hex)	Setting value (Hex)	Register Name	Default Value (Hex)	Descriptions
4E	**40**	*ISPControl4*	70	
94	**20**	*CG11C*	25	
95	**20**	*CG22C*	25	
98	**10**	*Brightness*	00	
99	**80**	*Y Contrast*	96	

2) YUV422 (8 Bit, Y range : 1 ~ 254 , U & V range : 1 ~ 254)

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
4C	**xxxx0000**	*ISPControl2*	00	U Y V Y…
	xxxx0001			V Y U Y…
	xxxx0010			Y U Y V…
	xxxx0011			Y V Y U…

Reg. Addr. (Hex)	Setting value (Hex)	Register Name	Default Value (Hex)	Descriptions
4E	**70**	*ISPControl4*	70	
94	**25**	*CG11C*	25	
95	**25**	*CG22C*	25	
98	**00**	*Brightness*	00	
99	**94**	*Y Contrast*	96	

3) RGB565 (8 Bit)

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
4C	**xxxx1000**	*ISPControl2*	00	R5G3, G3B5…
	xxxx1001			B5G3, G3R5…

4) RGB888 (12 Bit)

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
4C	**xxxx1010**	*ISPControl2*	00	R8G4, G4B8…
	xxxx1011			B8G4, G4R8…

5) ISP BAYER (10 Bit)

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
4C	**xxxx0100**	*ISPControl2*	00	RGRG…GBGB…
	xxxx0101			GBGB…RGRG…
	xxxx0110			GRGR…BGBG…
	xxxx0111			BGBG…GRGR…

6) Raw RGB BAYER (10 Bit)

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
4C	**xxxx0100**	*ISPControl2*	00	RGRG…GBGB…
	xxxx0101			GBGB…RGRG…
	xxxx0110			GRGR…BGBG…
	xxxx0111			BGBG…GRGR…
4B	**E0**	*ISPControl1*	DD	Color Correction Off
4E	**77**	*ISPControl4*	70	Gamma Off
59	**00**	*EdgeControl*	AC	Edge Enhancement Off

- Additional for 1282 x 1026

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
09	**D4**	*WiindowX1_L*	D5	
0B	**0C**	*WindowY1_L*	0D	
0D	**D6**	*WindowX2_L*	D5	
0F	**0E**	*WindowY2_L*	0D	
A3	**0C**	*VsyncStart_L*	0D	
A5	**0E**	*VsyncStop_L*	0D	

- Additional for 1284 x 1028

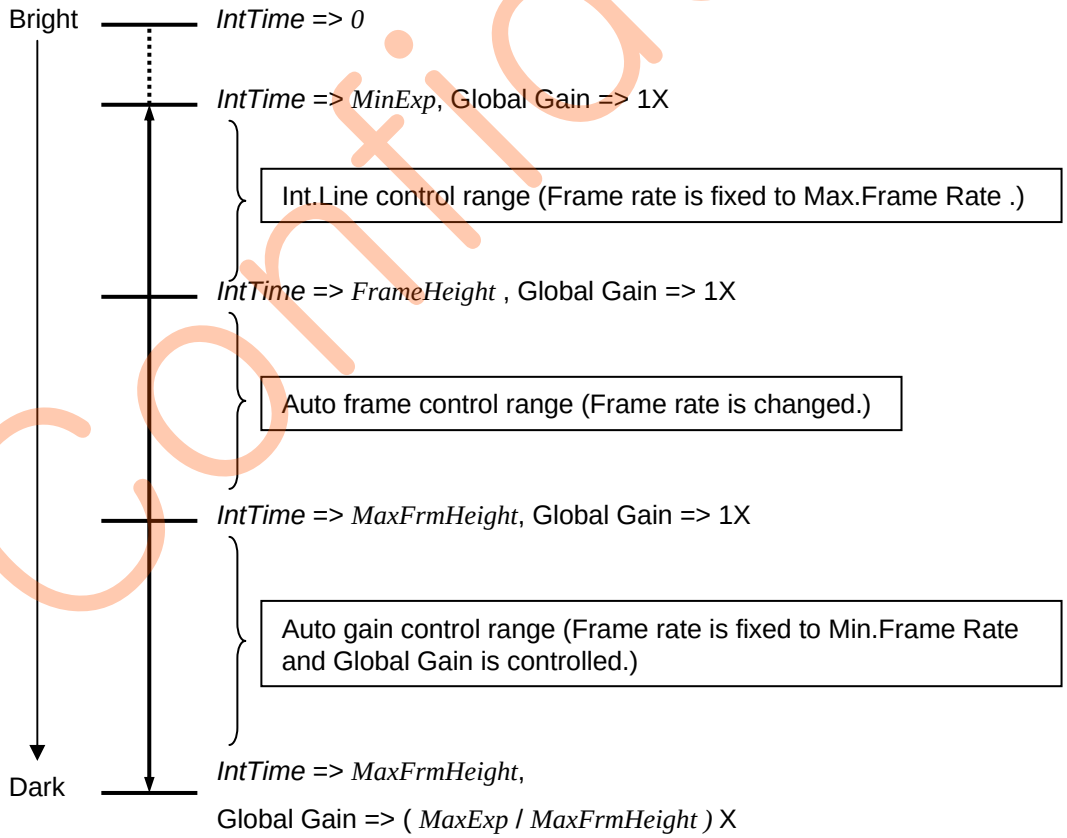
Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
09	**D3**	*WiindowX1_L*	D5	
0B	**0B**	*WindowY1_L*	0D	
0D	**D7**	*WindowX2_L*	D5	
0F	**0F**	*WindowY2_L*	0D	
A3	**0B**	*VsyncStart_L*	0D	
A5	**0F**	*VsyncStop_L*	0D	

- AE Control

(1) Internal AE Control

Related Registers : Int.Time(Reg.1Ah ~ 1Ch), GlobalGain(Reg.15h), AutoControl(Reg.D1h), TargetExp (Reg.B0h), MaxFrmHeight (Reg.B6h, B7h), MaxExp (Reg.B8, B9h), MinExp (Reg.BAh, BBh), RefGain (Reg.B5h), AutoLock (Reg.ABh)

If AE of *AutoControl(Reg.D1*h) register is set to '1', *IntTime(Reg.1A h ~ 1Ch), GlbGain(Reg.15h)* registers are automatically controlled by ISP to control overall brightness of sensor image. The target brightness level of image is set by *TargetExp(Reg.B0h)* register. During auto exposure process, the average brightness of image is controlled to get close to *TargetExp* register value with the margin set by *AutoLock*[3:0](*Reg.ABh*) register. *IntTime* registers are controlled, at first. If Integration Line is limited to the *MaxFrmHeight*(*Reg.B6h, B7h*), then Global Gain is controlled. Variation of *GlbGain* or *IntTime* register are limited by *MaxExp, MinExp, MaxFrameHeight* registers.



1) Auto Frame Control

Auto Frame Control Method can be used to get brighter image in dark condition. Frame rate is automatically controlled by ISP between Max.Frame Rate and Min.Frame Rate.

Max. Frame Rate = (MCLK frequency) / (Frame Height * Frame Width * 2)
Min. Frame Rate = (MCLK frequency) / (*MaxFrmHeight* * Frame Width * 2)

(Frame Height = *FrameHeight* (Reg.06h, 07h) + 1
Frame Width = *FrameWidth* (Reg.04h, 05h) + 1)

Min. Frame Rate is controlled by *MaxFrmHeight* register (Reg.B6h, B7h).
MaxFrmHeight must be bigger than *FrameHeight*..(*MaxFrmHeight* >= *FrameHeight*)

2) Auto Gain Control

Auto Gain Control Method can be used to get brighter image in dark condition. Global gain is controlled automatically by ISP between Max.Global Gain and 1X Global Gain.

Max. Global Gain = (*MaxExp* / *MaxFrmHeight*) X
Min. Global Gain = *MinGlbGain*

MaxExp must be bigger than *MaxFrmHeight. (MaxExp >= MaxFrmHeight)*

(2) External AE Control

Related Registers : AutoControl(Reg.D1h), Exposure (Reg.ADh, AEh, AFh),

If you turn off internal AE function of PO3130R, you can control Integration line and Global gain through *Exposure (Reg.ADh ~ AFh)* registers for implementing external Auto Exposure function. *IntTime* (*Reg.1Ah ~ 1Ch*) and *GlobalGain* (*Reg.15h*) registers aren't accessible by user. *Exposure* (*Reg.ADh ~ AFh*) registers aren't controllable while internal AE is working.

- Disable Internal AE Function

Reg. Addr. (Hex)	Register Name	Descriptions
D1	*AutoControl*	Set Bit 4(AE) to '0' to turn off internal AE function.
AC	*AESpeed*	Set this register to 00h

- Registers for External AE Control

Reg. Addr. (Hex)	Register Name	Descriptions
AD	*Exposure(H)*	
AE	*Exposure(M)*	
AF	*Exposure(L)*	

(1) *MinExp* < *Exposure* ≤ *FrameHeight* (Int.Line Control Range)

(2) *FrameHeight* < *Exposure* ≤ *MaxFrmHeight* (Frame Rate Control Range)

Current Frame Rate = (MCLK frequency) / (*Exposure* * Frame Width * 2)
Min. Frame Rate is limited by *MaxFrmHeight*.

(3) *MaxFrmHeight* < *Exposure* ≤ *MaxExp* (Global Gain Control Range)

Current Global Gain = (*Exposure* / *MaxFrmHeight*) X
Exposure is limited by *MaxExp*.

- AWB Control

(1) Internal AWB Control

Related Registers : RGain(Reg.16h), G1Gain(Reg.17h), BGain(Reg.18h), G2Gain(Reg.19h), AWBRratio(Reg.C2h), AWBBratio(Reg.C3h),

If AWB of *AutoControl(Reg.D1*h) register is set to '1', *RGain*(*Reg.16h*) and *BGain*(*Reg.18h*) registers are automatically controlled by ISP to control the RGB ratio of sensor image. The ratio of average of R, G, B components can be controlled by *AWBRratio and AWBBratio* registers. Those ratios are defined according to the following relation,

$$\overline{B} = \frac{AWBBratio}{128} \times \overline{G} \qquad \overline{R} = \frac{AWBRratio}{128} \times \overline{G}$$

(2) External AWB Control

If you turn off internal AWB function of PO3130R, you can control R, G and B gains through *R, G1, B* and *G2 Gain* (*Reg.16h ~ 19h*) registers for implementing external Auto White Balance function. *R* and *B gain* registers aren't controllable while internal AWB is working.

- Disable Internal AWB Function

Reg. Addr. (Hex)	Register Name	Descriptions
D1	*AutoControl*	Set Bit 5(AWB) to '0' to turn off internal AWB function.

- Registers for external AWB control

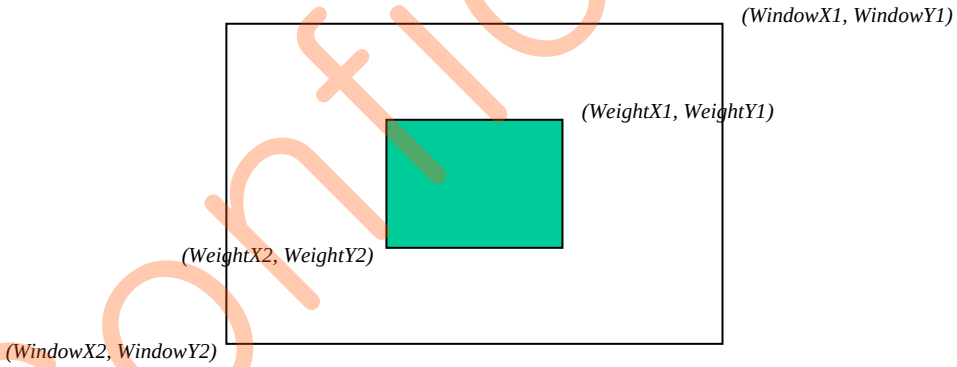
Reg. Addr. (Hex)	Register Name	Default Value (Hex)	Descriptions
16	*R Gain*	40	1X R Gain = 0x40 (2X = 0x80)
17	*G1 Gain*	40	1X G1 Gain = 0x40
18	*B Gain*	40	1X B Gain = 0x40
19	*G2Gain*	40	1X G2 Gain = 0x40

- Backlight Compensation

Related Registers : WeightX1 (Reg.C4h, C5h), WeightX2 (Reg.C6h, C7h), WeightY1 (Reg.C8h, C9h), WeightY2 (Reg.CAh, CBh), WWControl (Reg.AAh),

1) Weight Window

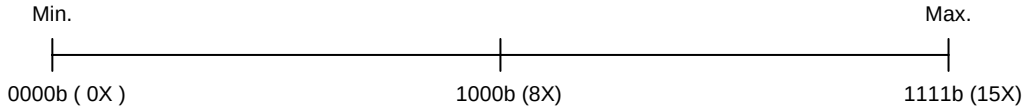
Reg. Addr. (Hex)	Register Name	Default Value (Hex)	Description
C4	*WeightX1(H)*	02	**Minimum** : *WindowX1*(*Reg.08h, 09h*)
C5	*WeightX1(L)*	67	
C6	*WeightX2(H)*	04	**Maximum** : *WindowX2*(*Reg.0Ch, 0Dh*)
C7	*WeightX2(L)*	25	
C8	*WeightY1(H)*	01	**Minimum** : *WindowY1*(*Reg.0Ah, 0Bh*)
C9	*WeightY1(L)*	5D	
CA	*WeightY2(H)*	02	**Maximum**: *WindowY2*(*Reg.0Eh, 0Fh*)
CB	*WeightY2(L)*	B3	



2) Weight Factor

Weight Factor is controlled by *CW[7..4]* (bit7 ~ 4) of *WeightControl* register (*Reg.AAh*).

0000b ≤ Weight Factor *(CW[7..4])* ≤ 1111b



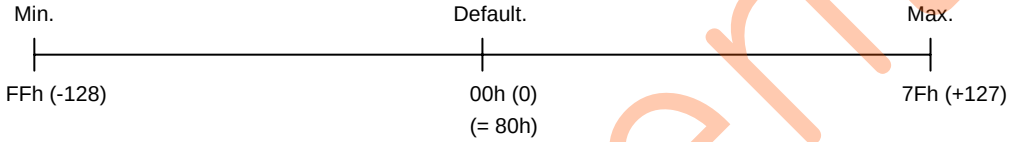
- Brightness / Y Contrast / Saturation (Only available for YCbCr422 & YUV422 output format)

-Related Registers : Brightness (Reg.98h), Contrast (Reg.99h), CG11C (CbGain, Reg.94h), CG22C (CrGain, Reg.95h)

Y *reault* = Y * (Ycontrast / 128) + Ybrightness
Cb *result* = Cb * *CbGain* / 32
Cr *result* = Cr * *CrGain* / 32

(1) Brightness

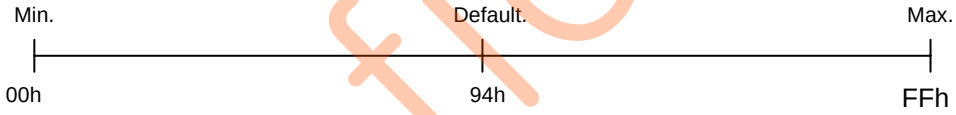
Brightness is controlled by *Brightness* register (*Reg.98h*). The default value of this register is 00h.



* Brightness(98h) : (bit7) | (bit6 ~ bit0) = sign digit | magnitude

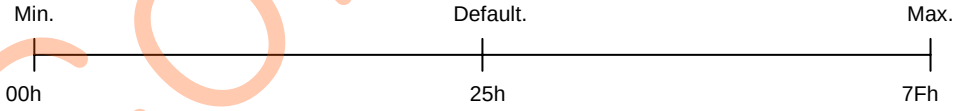
(2) Y Contrast

Contrast is controlled by Y *Contrast* register (*Reg.99h*). The default value of this register is 96h.



(3) Saturation

Saturation is controlled by *CG11C (CbGain)* and *CG22C (CrGain)* registers (*Reg.94h, 95h*) with the same values. The default value of these registers are 25h and these are controllable separately for adjusting color tone.



- Color Correction Matrix

Related Registers : ColorMatrix11 (Reg.8Bh) ~ ColorMatrix33 (Reg.93h)

Color correction can be accomplished by color transform registers (*Reg.8Bh ~ 93h*) by means of the following equation, where ***CC*** is 3x3 color correction matrix.

$$\begin{pmatrix} CT0 & CT1 & CT2 \\ CT3 & CT4 & CT5 \\ CT6 & CT7 & CT8 \end{pmatrix} = \begin{pmatrix} m00 & m01 & m02 \\ m10 & m11 & m12 \\ m20 & m21 & m22 \end{pmatrix} = 32 * CC$$

* m00 ~ m22 : (bit7) | (bit6 ~ bit0) = sign digit | magnitude

<Ex.>

$$\begin{pmatrix} m00 & m01 & m02 \\ m10 & m11 & m12 \\ m20 & m21 & m22 \end{pmatrix} = 32 * \begin{pmatrix} 1.7396 & -1.1444 & 0.4048 \\ -0.6039 & 1.4137 & 0.1902 \\ -0.1025 & -1.3094 & 2.4119 \end{pmatrix}$$

$$= \begin{pmatrix} 55.6672 & -36.6208 & 12.9536 \\ -19.3248 & 45.2384 & 6.0864 \\ -3.28 & -41.9008 & 77.1808 \end{pmatrix} = \begin{pmatrix} 38h & A5h & 0Dh \\ 93h & 2Dh & 06h \\ 83h & AAh & 4Dh \end{pmatrix}$$

- Y target Control

Related Registers : TargetExp (Reg.B0h, Reg.70h)

Y target is controlled by *TargetExp* register (*Reg.B0h, Reg.70h*).

<Ex.>

LEVEL	1	2	3	4	5	6	7	8	9
Reg.B0h	28	38	48	58	68	78	88	98	A8
Reg.70h									

- Sharpness Control

Related Registers : EdgeControl (Reg.59h), EdgeThreshold (Reg.5Ah)

Sharpness is controlled by *EdgeControl* (Reg.59h) and *EdgeThreshold* register (Reg.5Ah). All three values have the following Min. and Max. value.

00000b ≤ *EdgeGain (EdgeControl[4..0])* ≤ 11111b
00h ≤ *EdgeThreshold* ≤ FFh

The lowest sharpness level can be gotten by setting registers as follows.

EdgeGain = 00000b, *EdgeThreshold* = FFh

And, the highest sharpness level can be gotten by setting registers as follows.

EdgeGain = 11111b, *EdgeThreshold* = 00h

But, we recommend to set *EdgeThreshold* register value greater than 01h.

Ex.)

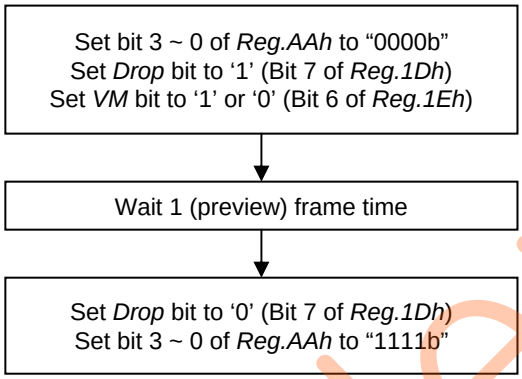
Sharpness Level	Reg. Addr. (Hex)	Recommended value	Register Name	Default Value
0	59	**xxx00000 (b)**	*EdgeControl*	xxx01100 (b)
	5A	**06 (h)**	*EdgeThreshold*	02 (h)
1	59	**xxx00100 (b)**		
	5A	**06 (h)**		
2	59	**xxx01000 (b)**		
	5A	**06 (h)**		
3	59	**xxx01100 (b)**		
	5A	**06 (h)**		
4	59	**xxx10000 (b)**		
	5A	**06 (h)**		
5	59	**xxx10100 (b)**		
	5A	**06 (h)**		
6	59	**xxx11000 (b)**		
	5A	**06 (h)**		

- Vertical / Horizontal Mirror

Related Registers : TgControl1(Reg.1Dh), TgControl2(Reg.1Eh)

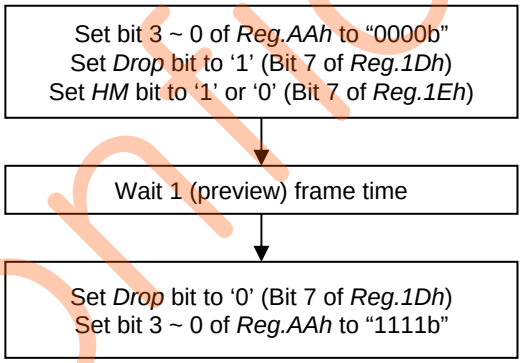
(1) Vertical Mirror

Vertical Mirror is controlled by *VM* bit (Bit 6 of *Reg.1Eh*).



(2) Horizontal Mirror

Horizontal Mirror is controlled by *HM* bit (Bit 7 of *Reg.1Eh*).



- Lens shading Compensation

Related Registers : LensRGain (Reg.56h), LensGGain (Reg.57h), LensBGain (Reg.58h)

- Special Effect (Only available for YCbCr422 & YUV422 output format)

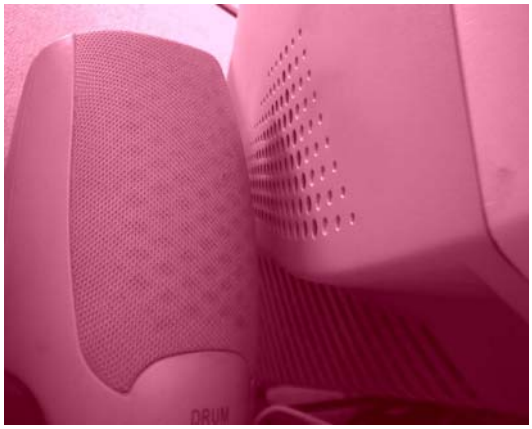
Related Registers : ISPControl3 (Reg.4Dh), CbTone (Reg.9Ch), CrTone (Reg.9Dh)

Reg. Addr. (Hex)	Setting value (Hex)	Register Name	Default Value (Hex)	Descriptions
4D	**1xxxxxxx**	*ISPControl3*	0A	
9C	***Appropriate Value***	*CbTone*	80	
9D	***Appropriate Value***	*CrTone*	80	

Sepia (Reg.9Ch = 98h, Reg.9Dh = 1Ch)

Green (Reg.9Ch = 98h, Reg.9Ch = 98h)

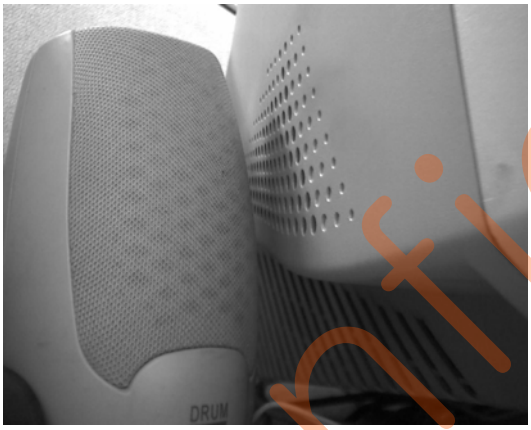
Aqua (Reg.9Ch = 28h, Reg.9Dh = A0h)



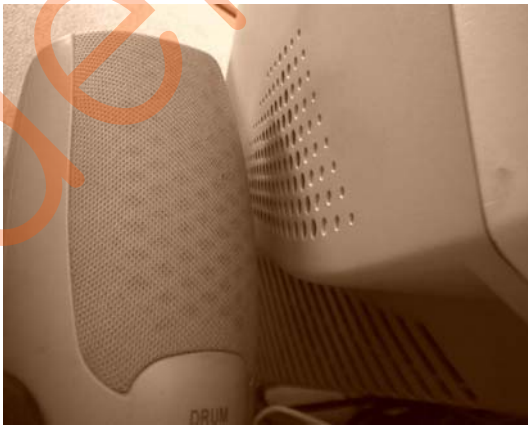
Red (Reg.9Ch = 80h, Reg.9Dh = 28h)

Cool (Reg.9Ch = 20h, Reg.9Dh = 98h)

Warm (Reg.9Ch = 90h, Reg.9Dh = 28h)



BW (Reg.9Ch = 80h, Reg.9Dh = 80h)



Antique (Reg.9Ch = 10h, Reg.9Dh = 90h)

- PCB Layout Considerations

It is important that care be given to the PCB layout to reduce power noise. Figure 1 and 2 show the recommended connection diagram for the PO3130R.

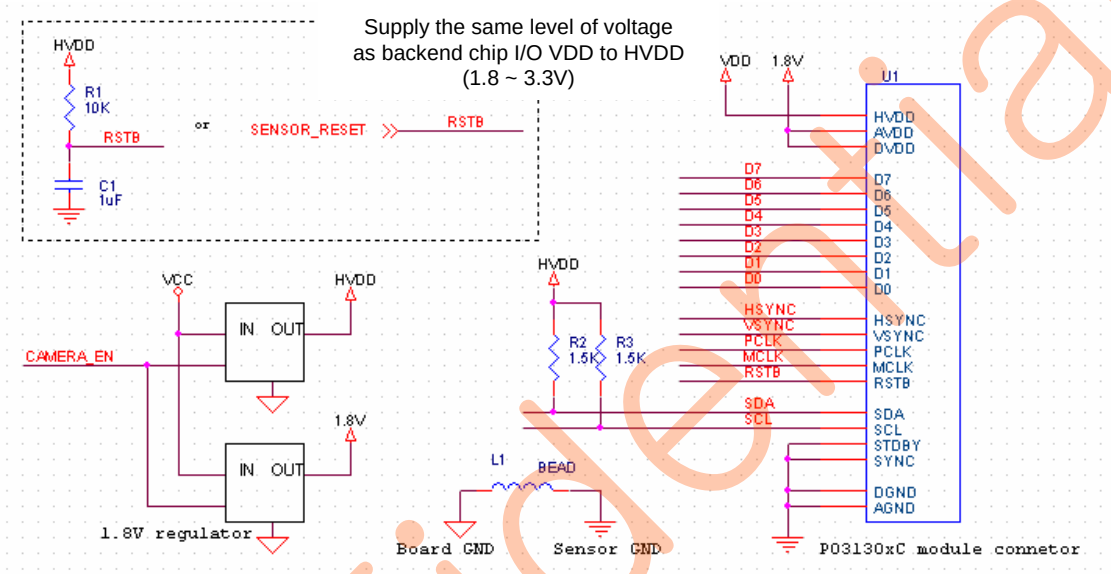


Figure 1. PO3130xC module typical connection diagram

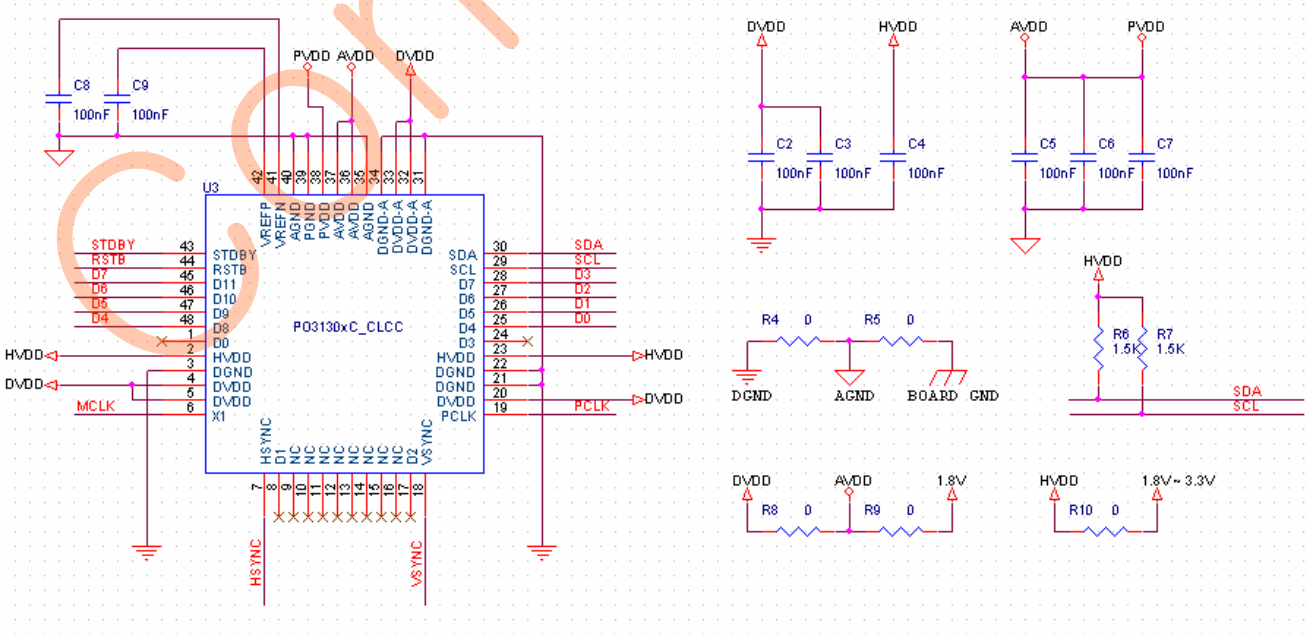


Figure 2. PO3130xC CLCC typical connection diagram

Ground Planes

The ground plain should connect to the regular PCB ground plane at a single point

Power Planes

The PC board layout should have the distinct power plane for PO3130xC. This power plane should have the separate regulator or be connected to the regular PCB power plane(VCC) at a single point through a ferrite bead, as illustrated in Figure 2. This power plane also has two distinct power planes, one for analog pins and one for digital pins. The analog power plane should encompass AVDD and PVDD pins, and the digital power plane should encompass DVDD pin.

Supply Decoupling

Noise on the PO3130xC power plane can be reduced by the use of multiple decoupling capacitors. (See Figure 2.) Optimum performance is achieved by the use of 0.1uF ceramic capacitors. Each of the power pins should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to power pins with the capacitor leads as short as possible, thus minimizing lead inductance.

- Stand-by method

1. Standby pin (Hardware Method)

⇒ You can control stand-by mode by using STDBY pin.

LOW : normal mode
HIGH : stand-by (power-down) mode

2. I2C Stand-by (Software Method)

⇒ You can control stand-by mode by setting *STDBY* bit (bit 6) of *Reg.1Fh.*
⇒ ***STDBY pin must be connected to DGND***

'0' : normal mode
'1' : stand-by (power-down) mode