PAS202BCB SINGLE-CHIP CMOS VGA COLOR DIGITAL IMAGE SENSOR
PAS202BBB SINGLE-CHIP CMOS VGA B&W DIGITAL IMAGE SENSOR

General Description

The PAS202BCB/PAS202BBB is a highly integrated CMOS active-pixel image sensor that has a VGA resolution of 644H x 484V. To have an excellent image quality, the PAS202BCB/PAS202BBB outputs 10-bit RGB raw data through a parallel data bus. It is available in color or monochrome and in 28-pin LCC.

The PAS202BCB/PAS202BBB can be programmed to set the exposure time for different luminance condition via I2C™ serial control bus. By programming the internal register sets, it performs on-chip frame rate adjustment, offset correction DAC and programmable gain control.

Features

- **VGA(644 x 484 pixels) resolution, ~1/4" Lens**
- **Bayer-RGB color filter array**
- **On-chip 10-bit pipelined A/D converter**
- **Output format: 10-bit parallel RGB raw data**
- **On-chip 9-bit background compensation DAC**
- **On-chip programmable gain amplifier**
  - **4-bit color gain amplifier(x3)**
  - **5-bit global gain amplifier (x5)**
- **Continuous variable frame time(1/2sec~1/30sec)**
- **Continuous variable exposure time**
- **I2C Interface**
- **Digitally programmable registers**
- **Single 3.3V supply voltage**
- **100 mW low power dissipation**
- **350 uW low power down dissipation**
- **Flash light timing**
- **Mirror output**

Key Specification

Supply Voltage	3.3V ± 10%
Resolution	644(H) x 484(V)
Array diagonal	4.5mm (~1/4"Optic)
Pixel Size	5.6μmX5.6μm
Frame rate	~30 fps
System clock	Up to 48 MHz
Max. pixel rate	12MHz
Sensitivity	0.6V/Lux-sec(green)
PGA gain	29.5 dB max.
Color filter	RGB Bayer Pattern
Exposure Time	~ Frame time to 4 pxclk
Scan Mode	Progressive
S/N Ratio	>42 dB
Package	28 pins LCC

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1. Pin Assignment

PIN No.	PIN NAME	Type	Definition
1	VSSAY	GND	Analog ground
2	VLRST	BIAS	Fixed bias input voltage, 1.65V
3	PXD<9>	OUT	Digital data output
4	PXD<8>	OUT	Digital data output
5	PXD<7>	OUT	Digital data output
6	PXD<6>	OUT	Digital data output
7	PXD<5>	OUT	Digital data output
8	VDDQ	PWR	Digital VDD, 3.3V
9	VSSQ	GND	Digital ground
10	PXD<4>	OUT	Digital data output
11	PXD<3>	OUT	Digital data output
12	PXD<2>	OUT	Digital data output
13	PXD<1>	OUT	Digital data output
14	PXD<0>	OUT	Digital data output
15	SYSCLK	IN	Master clock input
16	PXCLK	OUT	Pixel clock output
17	HSYNC	OUT	Horizontal Synchronization clock
18	VSYNC	OUT	Vertical Synchronization clock
19	SCL	IN	I2C clock
20	SDA	I/O	I2C bi-directional data
21	VDDD	PWR	Digital VDD, 3.3V
22	VSSD	GND	Digital ground
23	CSB	IN	Chip select
24	VCM	BYPASS	Analog voltage reference
25	VRT	BYPASS	Analog voltage reference
26	VRB	BYPASS	Analog voltage reference
27	VSSA	GND	Analog ground
28	VDDA	PWR	Analog VDD, 3.3V

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2. Block Diagram

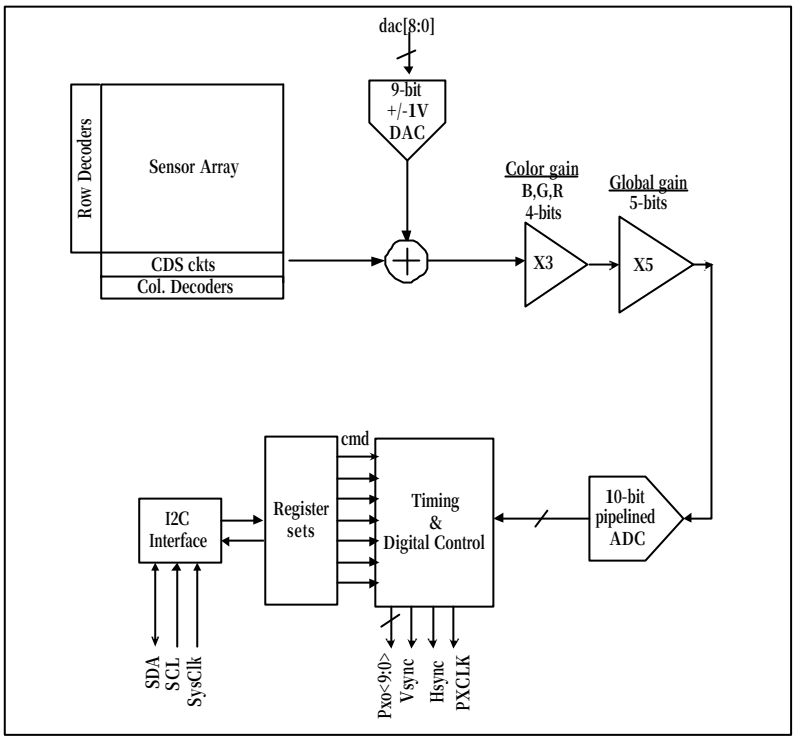


Fig 2.1 – Block diagram of the PAS202BCB/PAS202BBB

3. Output Format

3.1. Pixel Array And Pixel Color Pattern

The output image format of PAS202BCB/PAS202BBB is VGA (640x480 pixel array). To provide the co-processor with the extra information it needs for interpolation at the edges of the pixel array, an border of 2 pixels on all 4 sides of the array are available. Fig 3.1. illustrates the pixel array and pixel color pattern.

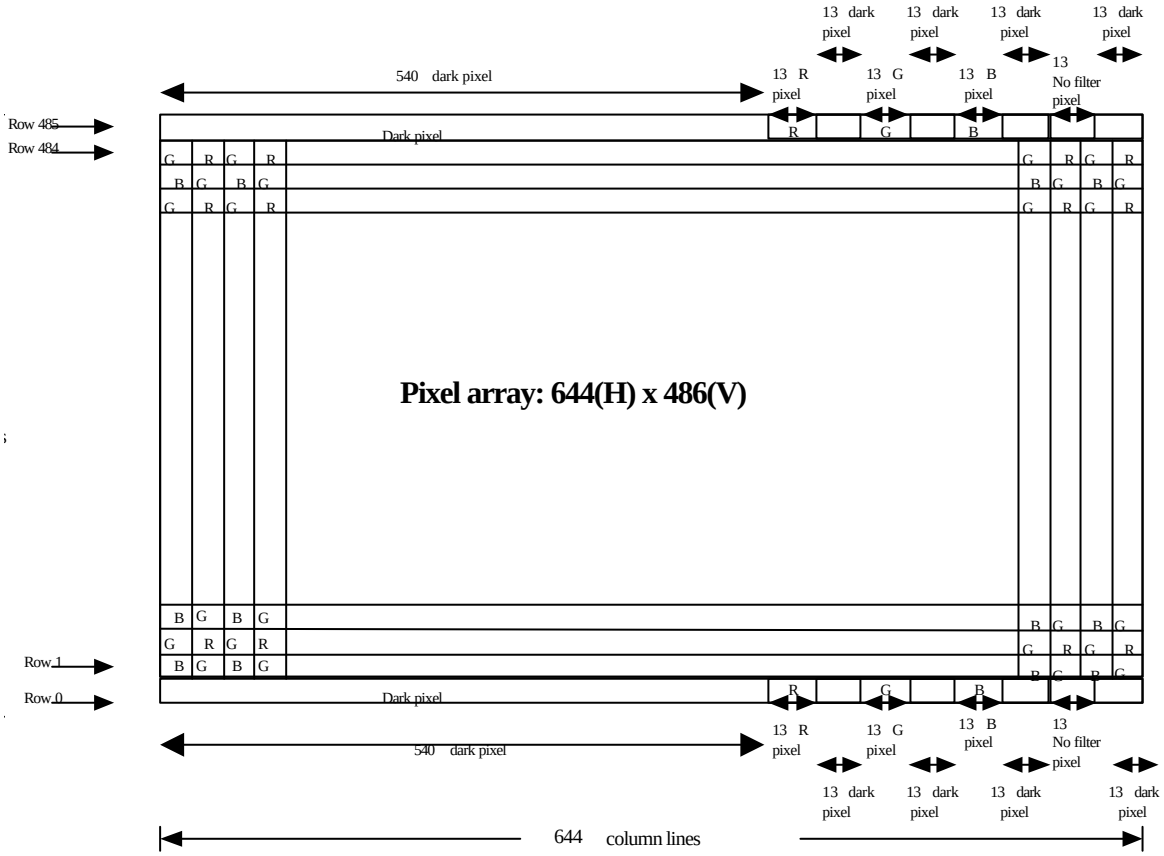


Fig 3.1. Pixel array and pixel color pattern

Note:

1. Pixel color pattern does not apply to monochrome sensor.
2. Pixel read-out proceeds from left to right, and from bottom row to top row.
3. Pixel array not drawn to scale.

3.2 Output timing:

Pixel per line is programmable, 772 pixels ~ 1156 pixels.

4+4 blank pixel for each line. (See Fig 3.2. Fig 3.3)

1+1 Dark line for each frame.(See Fig 3.4. Fig 3.5)

Dark line output format: Fig 3.6.

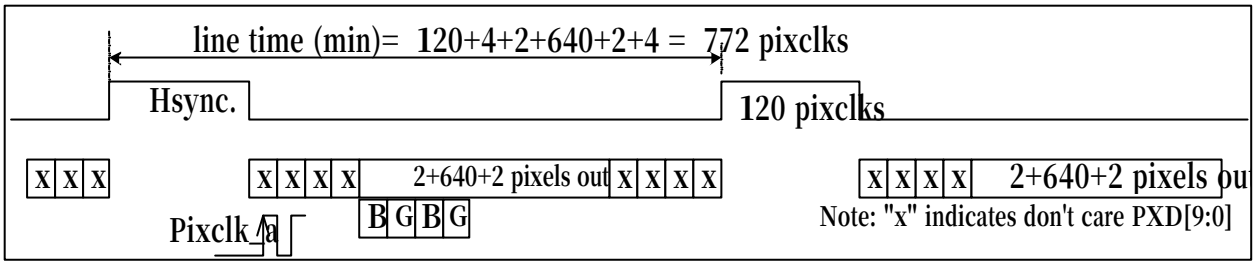


Fig 3.2. Inter-line timing (default)

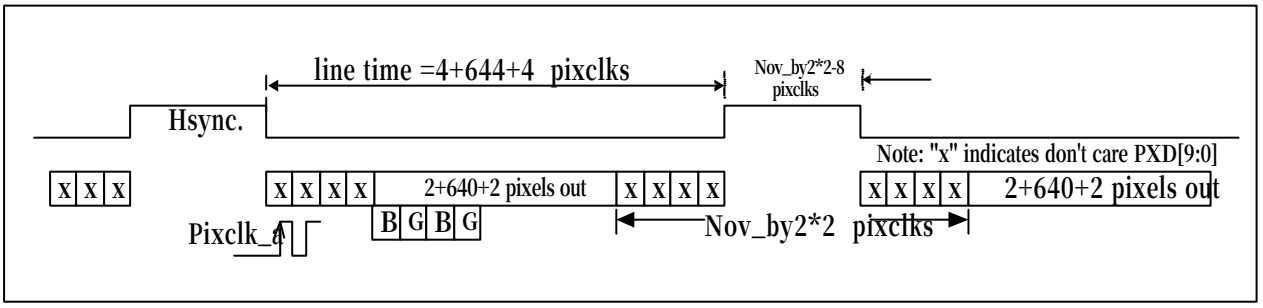


Fig 3.3. Inter-line timing (programmable)

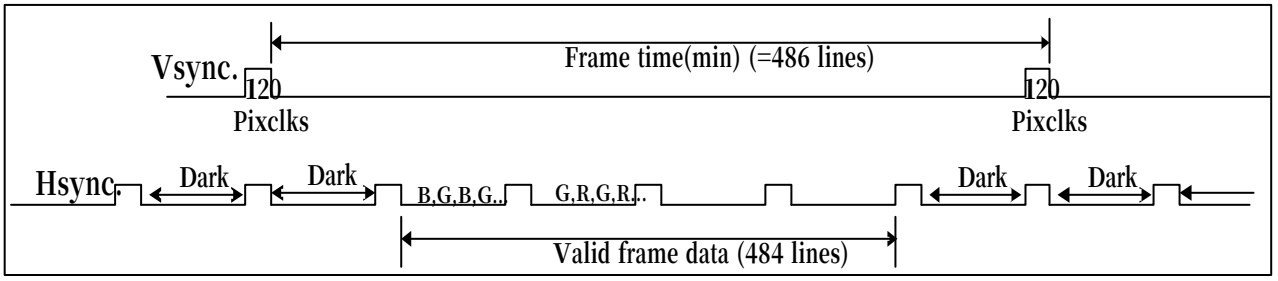


Fig 3.4. Inter-frame timing (default)

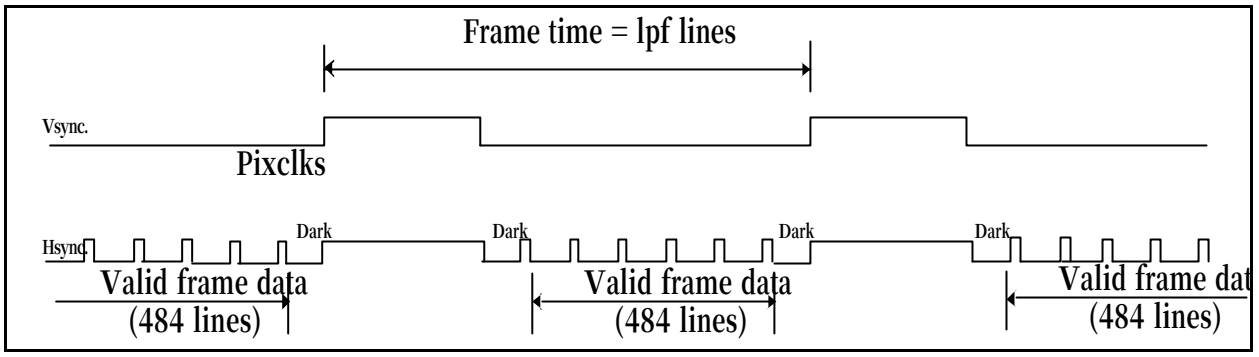


Fig 3.5. Inter-frame timing (programmable)

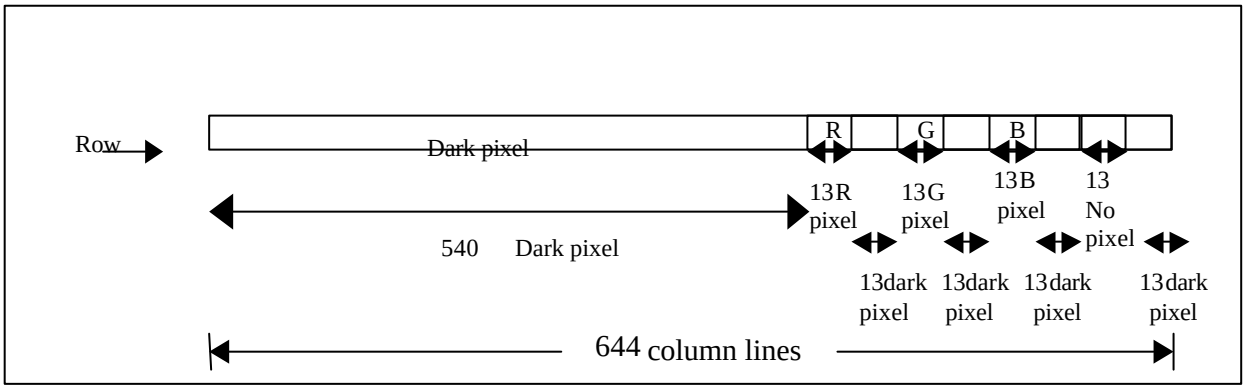


Fig 3.6. Dark line output format

4. I2C Bus

PAS202BCB/PAS202BBB supports I2C-bus transfer protocol and is acting as slave device. The 7 bits unique slave address is 1000000 and supports receiving / transmitting speed up to 400kHz.

4.1 I2C bus overview

- Only two wires SDA (serial data) and SCL (serial clock) carry information between the devices connected to the I2C bus. Normally both SDA and SCL lines are open collector structure and pull high by external pull-up resistors.
- Only the master can initiates a transfer (start), generates clock signals, and terminates a transfer (stop).
- Start and stop condition: A high to low transition of the SDA line while SCL is high defines a start condition. A low to high transition of the SDA line while SCL is high defines a stop condition. Please refer to Fig 4.1.
- Valid data: The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read/write control bit is the LSB of the first byte. Please refer to Fig 4.2.
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge: The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

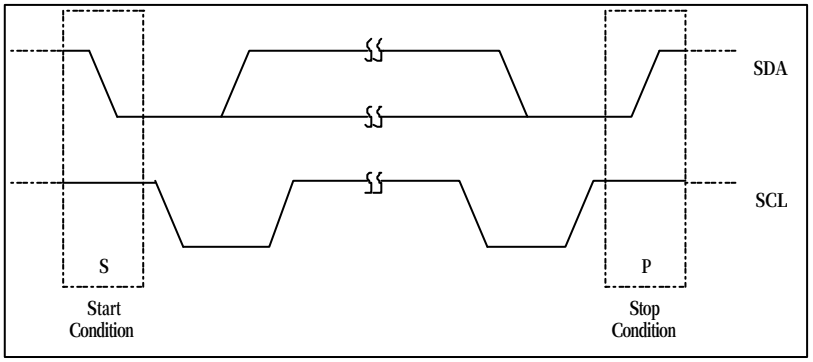


Fig 4.1 Start and Stop Conditions

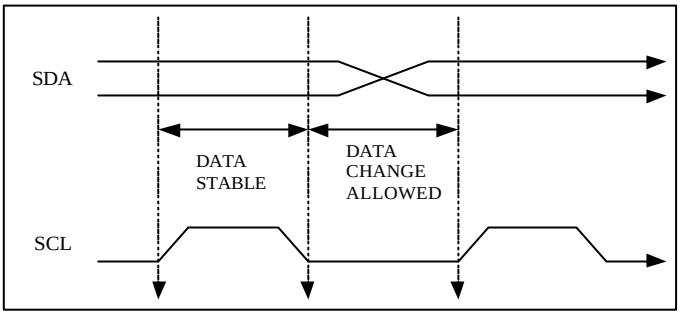
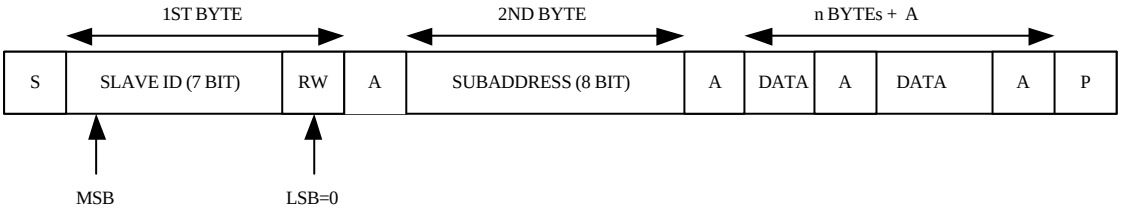


Fig 4.2 Valid Data

4.2 Data Transfer Format

4.2.1 Master transmits data to slave (write cycle)

- S : Start
- A : Acknowledge by slave
- P : Stop
- RW : The LSB of 1ST byte to decide whether current cycle is read or write cycle.
  RW=1 read cycle, RW=0 write cycle.
- SUBADDRESS : The address values of PAS202BCB/PAS202BBB internal control registers (Please refer to PAS202BCB/PAS202BBB register description)

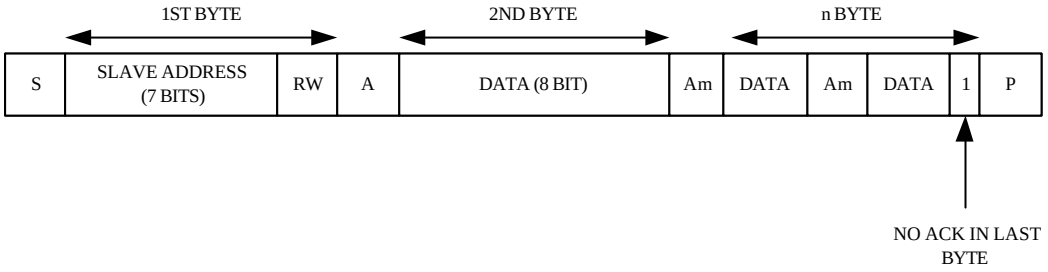


During write cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read/write control bit to SDA line. After slave(PAS202BCB/PAS202BBB) issues acknowledgment, the master places 2nd byte (sub-address) data on SDA line. Again follow the PAS202BCB/PAS202BBB acknowledgment, the master places the 8 bits data on SDA line and transmit to PAS202BCB/PAS202BBB control register (address was assigned by 2nd byte). After PAS202BCB/PAS202BBB issue acknowledgment, the master can generate a stop condition to end of this write cycle. In the condition of multi-byte write, the PAS202BCB/PAS202BBB sub-address is automatically increment after each DATA byte transferred. The data and A cycles is repeat until last byte write. Every control

registers value inside PAS202BCB/PAS202BBB can be programming via this way. (Please refer to Fig 4.3.)

4.2.2 Slave transmits data to master (read cycle)

- The sub-address was taken from previous write cycle
- The sub-address is automatically increment after each byte read
- Am : Acknowledge by master
- Note there is no acknowledgment from master after last byte read



During read cycle, the master generates start condition and then place the 1st byte data that are combined slave address (7 bits) with a read/write control bit to SDA line. After issue acknowledgment, 8 bits DATA was also placed on SDA line by PAS202BCB/PAS202BBB. The 8 bit data was read from PAS202BCB/PAS202BBB internal control register that address was assigned by previous write cycle. Follow the master acknowledgment, the PAS202BCB/PAS202BBB place the next 8 bits data (address is increment automatically) on SDA line and then transmit to master serially. The DATA and Am cycles is repeat until the last byte read. After last byte read, Am is no longer generated by master but instead by keep SDA line high. The slave (PAS202BCB/PAS202BBB) must releases SDA line to master to generate STOP condition. (Please refer to Fig 4.3.)

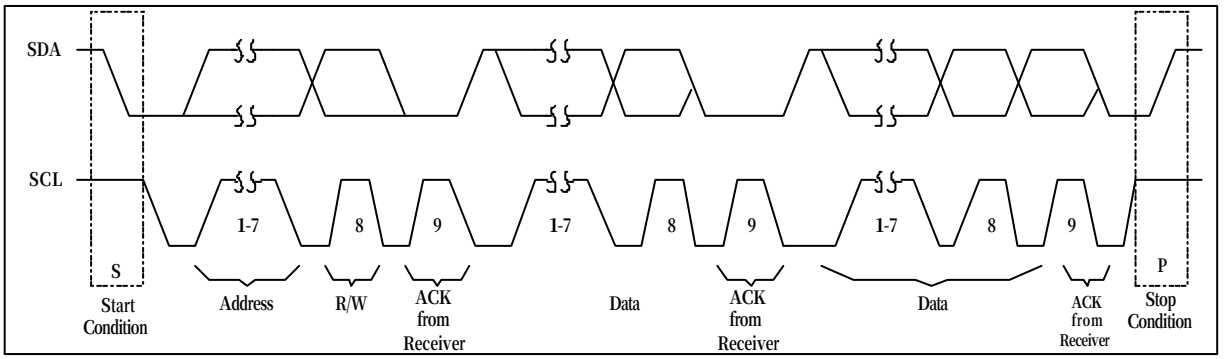


Fig 4.3 Data Transfer Format

4.3 I2C Bus Timing

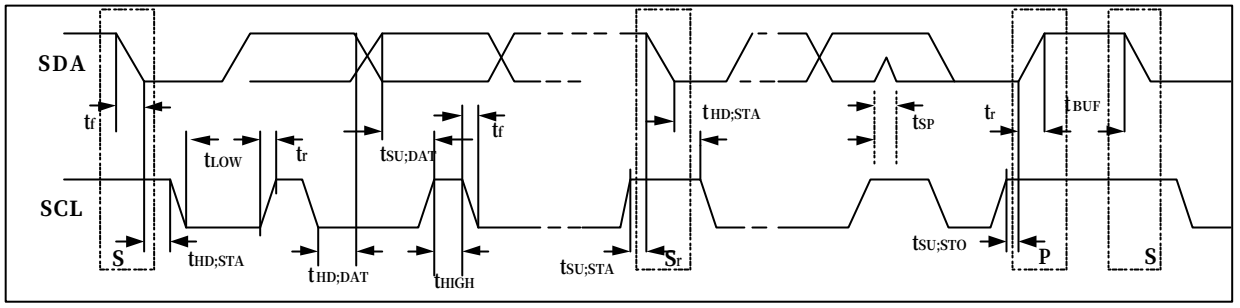


Fig 4.4 I2C Bus Timing

4.4 I2C Bus Timing Specification

PARAMETER	SYMBOL	STANDARD-MODE		UNIT
		MIN.	MAX.	
SCL clock frequency	f_{scl}	10	400	kHz
Hold tie (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	-	us
Low period of the SCL clock	t_{LOW}	4.7	-	us
HIGH period of the SCL clock	t_{HIGH}	0.75	-	us
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	us
Data hold time. For I2C-bus device	$t_{HD;DAT}$	0	3.45	us
Data set-up time	$t_{SU;DAT}$	250	-	ns
Rise time of both SDA and SCL signals	t_r	30	N.D.	ns(note1)
Fall time of both SDA and SCL signals	t_f	30	N.D.	ns(note1)
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	us
Bus free time between a STOP and START	t_{BUF}	4.7	-	us
Capacitive load for each bus line	C_b	1	15	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	0.1 V_{DD}	-	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	0.2 V_{DD}	-	V

Note 1: It depends on the "high" period time of SCL.

5. Specifications

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
Vdd	DC supply voltage	-0.5	3.8	V
Vin	DC input voltage	0.5	Vdd+0.5	V
Vout	DC output voltage	-0.5	Vdd+0.5	V

DC Electrical Characteristics (VDD=3.3V±10%, Ta=0°C~40°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Type :PWR					
VDD	Analog and digital operating voltage	3.00	3.3	3.60	V
IDD	Operating Current		30		mA
Type :IN & I/O Reset and SYSCLK					
VIH	Input voltage HIGH	2.0		VDD	V
VIL	Input voltage LOW	0		0.8	V
Cin	Input capacitor			10	pF
Ilkg	Input leakage current			1.0	uA
Type : OUT & I/O for PXD0:9, PXCLK, H/VSYNC & SDA, load 20pf, 3.3volts					
VOH	Output voltage HIGH	Vdd-0.2			V
VOL	Output voltage LOW			0.2	V

AC Operating Condition

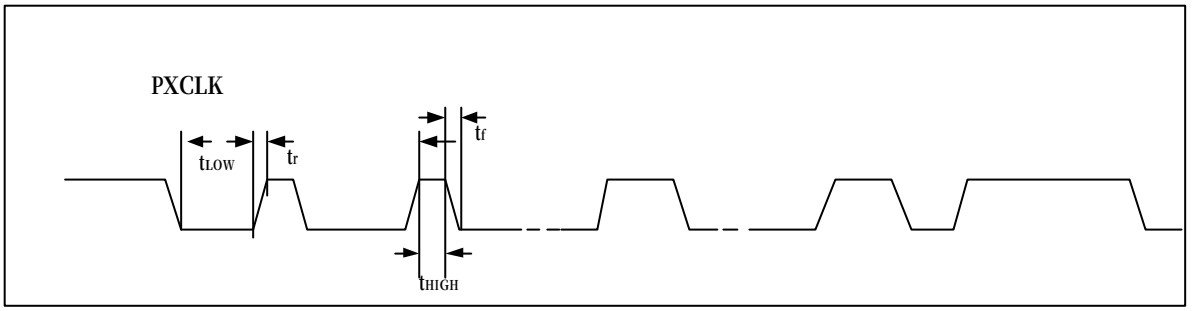
Symbol	Parameter	Min.	Typ.	Max.	Unit
fsysclk	Master clock frequency	8		48	MHz
fpxclk	Pixel clock output frequency			12	MHz

Sensor Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Photo response non-uniformity	PRNU		1.7		%	
Saturation output voltage	Vsat.		1.2		V	
Dark output voltage	Vdark		53		mV/sec	
Dark signal non-uniformity	DSNU		2.79		Lsb	
Sensitivity (Red channel)	R		0.8		V/Lux-sec	
Sensitivity (Green channel)	G		0.6		V/Lux-sec	
Sensitivity (Blue channel)	B		0.6		V/Lux-sec	
Column non-uniformity	Cnu			1.56	%	

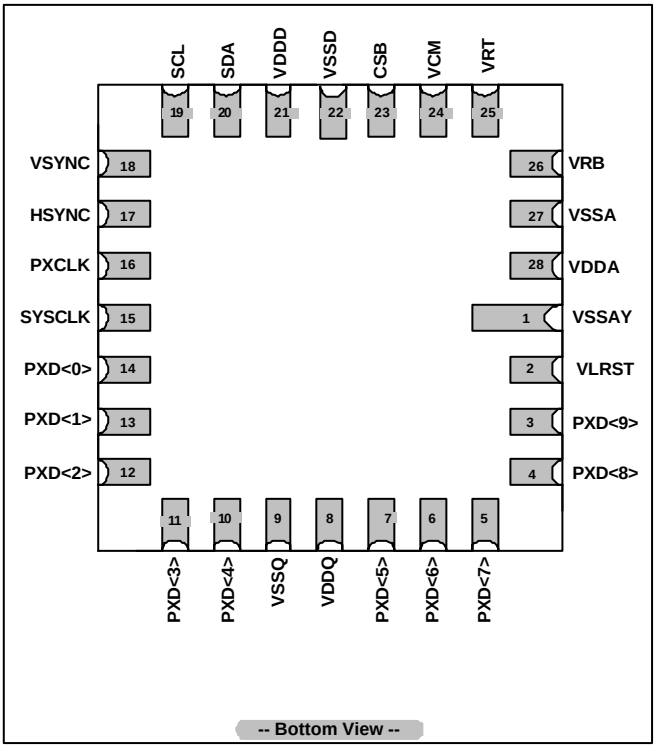
PXCLK Timing Specification @12M Hz

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{LOW}	Low period of the PXCLK duty cycle	40%	50%	60%	%
t_{HIGH}	High period of the PXCLK duty cycle	40%	50%	60%	%
t_r	Rise time signal		10		ns
t_f	Fall time signal		10		ns
C_b	Capacitive load for each bus line		15		pF

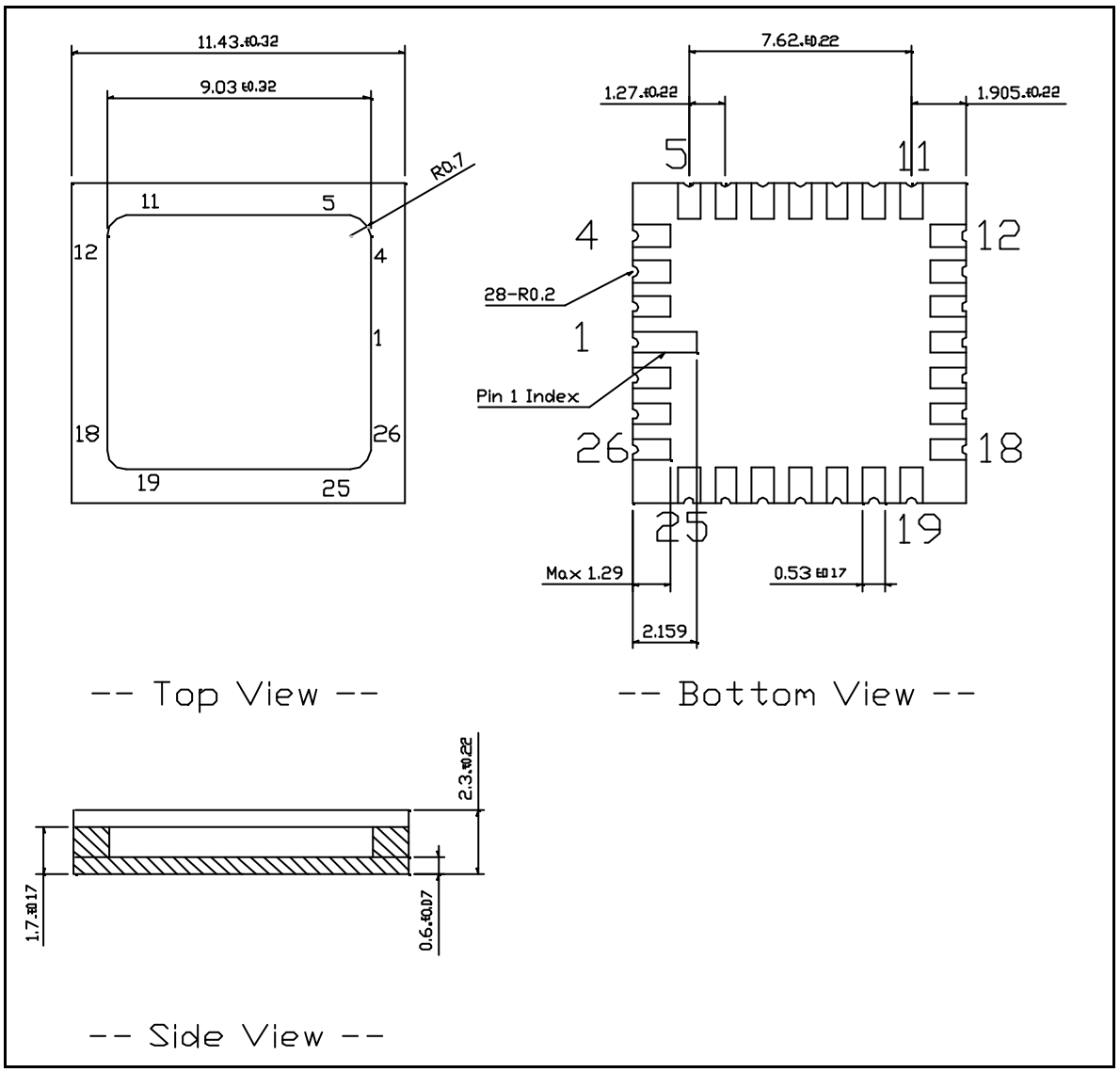


6. Package Information

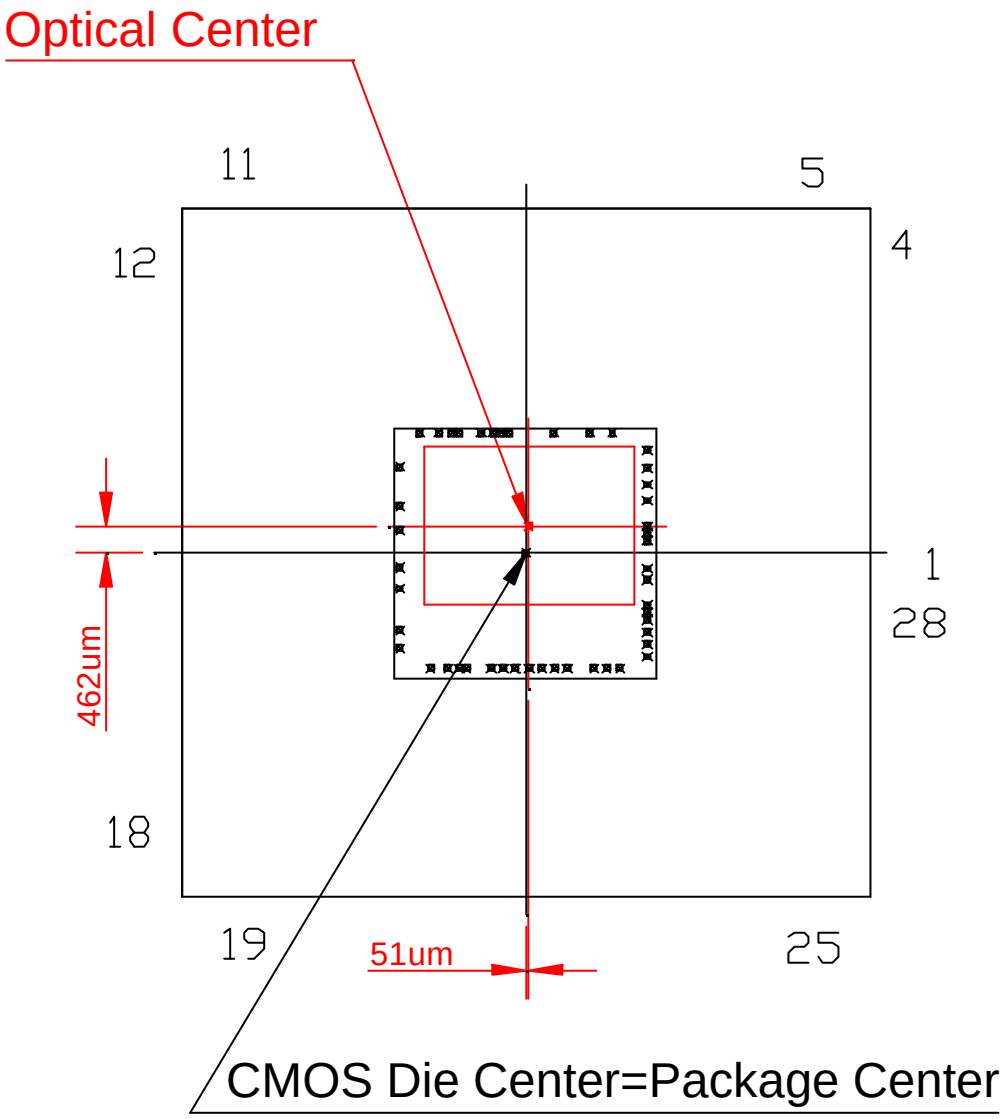
6.1. Pin Connection Diagram



6.2. Package Outline



6.3. Optical Center(Sensor Array Center)and Die/Package Center Offset



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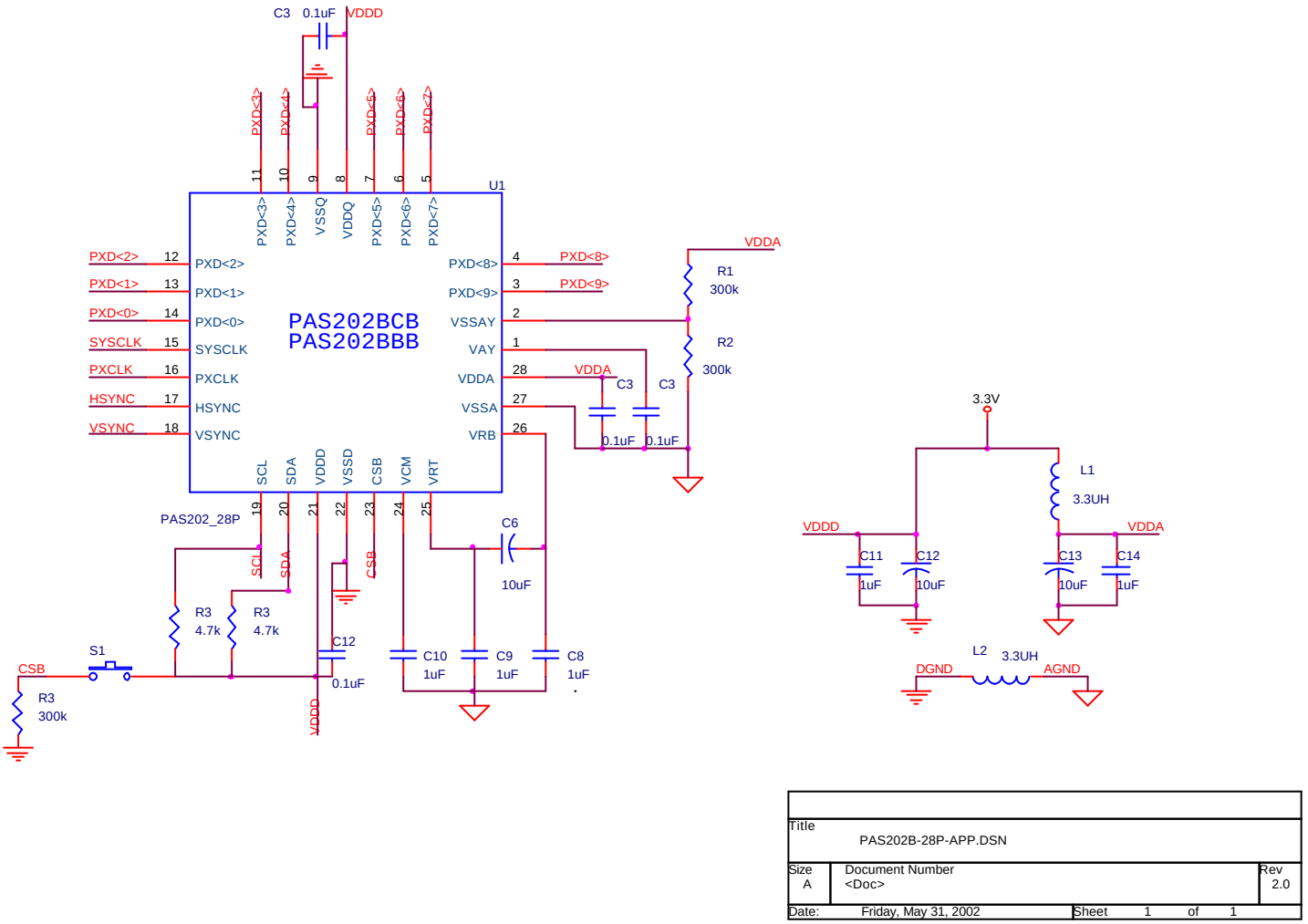
7. Referencing Application Circuit



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Date: Friday, May 31, 2002	Sheet 1 of 1	