1/6-Inch SOC VGA CMOS Digital Image Sensor

MT9V112I2ASTC

Features

- Micron® DigitalClarity™ CMOS Imaging technology
- System-On-a-Chip (SOC)—Completely integrated camera system
- Ultra-low power, low cost, progressive scan CMOS image sensor
- Superior low-light performance
- On-chip image flow processor (IFP) performs sophisticated processing:
  - Color recovery and correction
  - Sharpening
  - Gamma
  - Lens shading correction,
  - On-the-fly defect correction
- Filtered image downscaling to arbitrary size with smooth, continuous zoom and pan
- Automatic Features:
  - Auto exposure (AE)
  - Auto white balance (AWB)
  - Auto black reference (ABR)
  - Auto flicker avoidance
  - Auto color saturation
  - Auto defect identification and correction
- Fully automatic Xenon and LED-type flash support, fast exposure adaptation
- Multiple parameter contexts, easy/fast mode switching
- Camera control sequencer automates:
  - Snapshots
  - Snapshots with flash
  - Video clips
- Simple two-wire serial programming interface
- ITU-R BT.656 (YCbCr), 565RGB, 555RGB, or 444RGB formats (progressive scan)
- Raw and processed Bayer formats

Applications

- Cellular phones
- PDAs
- Toys
- Other battery-powered products

Table 1: Key Performance Parameters

Parameter		typical Value
Optical Format		1/6-inch (4:3)
Active Imager Size		2.30mm(H) x 1.73mm(V) 2.88mm Diagonal
Active Pixels		640H x 480V
Pixel Size		3.6µm x 3.6µm
Color Filter Array		RGB Bayer Pattern
Shutter type		Electronic Rolling Shutter (ERS)
Maximum Data Rate/ Master Clock		12 MPS–13.5 MPS/ 24 MHz–27 MHz
Frame Rate (VGA 640H x 480V)		30 fps at 27 MHz
ADC Resolution		10-bit, on-chip
Responsivity		1.0V/lux-sec (550nm)
Dynamic Range		71dB
SNR_{MAX}		44dB
Supply Voltage	I/O Digital	1.7V–3.1V (VDD nominal)
	Core Digital	1.7V–1.9V or 2.5V–3.1V (1.8V or 2.8V nominal)
	Analog	2.5V–3.1V (2.8V nominal)
Power Consumption		76mW at 1.8V, 15 fps
Operating temperature		–30°C to +70°C
Packaging		36-Ball ICSP, wafer or die

Ordering Information

Table 2: Available Part Numbers

Part Number	Description
MT9V112I2ASTC	36-Ball iCSP (standard)
MT9V112I9ASTC	36-Ball iCSP (lead-free)

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General Description

The Micron Imaging MT9V112 is a VGA-format, single-chip camera CMOS active-pixel digital image sensor. this device combines the MT9V012 image sensor core with fourth-generation digital image flow processor technology from Micron Imaging. It captures high-quality color images at VGA resolution.

The VGA CMOS image sensor features DigitalClarity—the Micron breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The sensor is a complete camera-on-a-chip solution designed specifically to meet the low-power, low-cost demands of battery-powered products such as cellular phones, PDAs, and toys. It incorporates sophisticated camera functions on-chip and is programmable through a simple two-wire serial interface.

The MT9V112 performs sophisticated processing functions including color recovery, color correction, sharpening, programmable gamma correction, auto black reference clamping, auto exposure, automatic 50Hz/60Hz flicker avoidance, lens shading correction, auto white balance, and on-the-fly defect identification and correction. Additional features include day/night mode configurations; special camera effects such as sepia tone and solarization; and interpolation to arbitrary image size with continuous filtered zoom and pan. The device supports both Xenon and LED-type flash light sources in several snapshot modes.

The MT9V112 can be programmed to output progressive-scan images up to 30 frames per second (fps). The image data can be output in any one of six 8-bit formats:

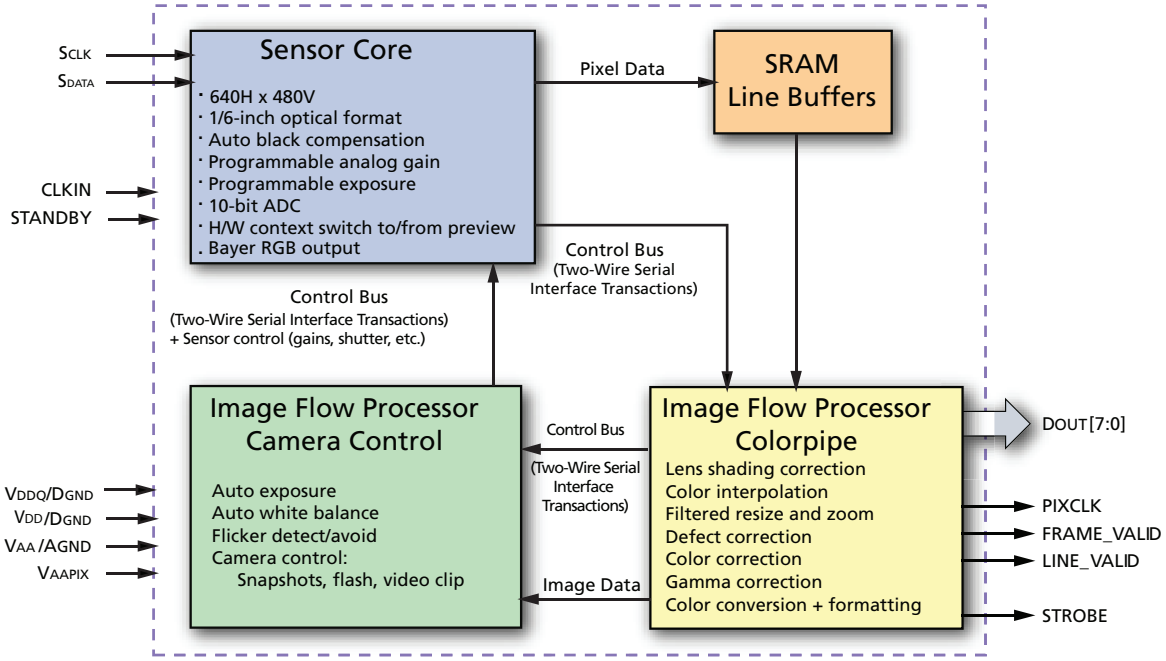
- ITU-R BT.656 (formerly CCIR656, progressive scan only) YCbCr
- 565RGB
- 555RGB
- 444RGB
- Raw Bayer
- Processed Bayer

The FRAME_VALID and LINE_VALID signals are output on dedicated balls, along with a pixel clock that is synchronous with valid data.

Functional Overview

The MT9V112 is a fully-automatic, single-chip camera, requiring only a power supply, lens, and clock source for basic operation. Output video is streamed via a parallel 8-bit DOUT port, shown in *Figure 1, Functional Block Diagram, on page 7*. The output pixel clock is used to latch data, while FRAME_VALID and LINE_VALID signals indicate the active video. The MT9V112 internal registers are configured using a two-wire serial interface.

Figure 1: Functional Block Diagram



The device can be put in a low-power sleep mode by asserting STANDBY and shutting down the clock. Output signals can be tri-stated. Both tri-stating output signals and entry in STANDBY mode also can be achieved via two-wire serial interface register writes.

The MT9V112 accepts input clocks up to 27 MHz, delivering up to 30 fps for VGA resolution images.

Internal Architecture

Internally, the MT9V112 consists of a sensor core and an image flow processor. The IFP is divided in two sections: the colorpipe (CP), and the camera controller .

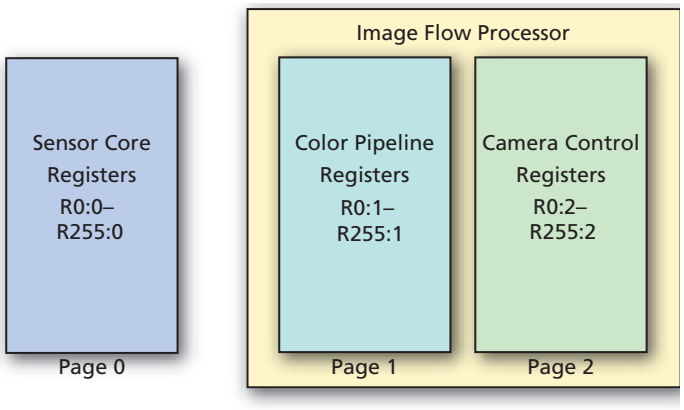
The sensor core captures raw Bayer-encoded images that are then input to the IFP.

The CP section of the IFP processes the incoming stream to create interpolated, color-corrected output, and the CC section controls the sensor core to maintain the desired exposure and color balance, and to support snapshot modes.

Register Overview

The sensor core, CP, and CC registers are grouped in three separate address spaces, shown in *Figure 2, Internal Registers Grouping, on page 8*.

Figure 2: Internal Registers Grouping



NOTE:

Internal registers are grouped in three address spaces. Program R240 selects the desired address space.

The register notation is defined in the section below. When accessing internal registers via the two-wire serial interface, select the desired address space by programming the R240 register.

The sensor registers are summarized in *Table 12, Sensor Registers – Address Page 0, on page 33*. The colorpipe registers are summarized in *Table 8, Colorpipe Registers – Address Page 1, on page 13*. The camera control registers are summarized in *Table 9, Camera Control Registers – Address Page 2, on page 16*.

Register Notation

The following register address notations are used:

- R<decimal address>:<address page>
  Example: R9:0—Shutter width register in sensor page (page 0). Used to uniquely specify a register.
- R<decimal address>
  Example: R240—Page address register. Used when the register address is global in all three pages or when by context the address page is understood.
- 0x<2 digit hex address>
  Example: 0xF0—Page address register. Used when the register address is global in all three pages, or when by context the address page is understood.
- 0x<3 digit hex address>
  Example: 0x105— Page 1, Aperture Correction register (0x05). Same as 0x<2 digit hex address> notation; leading digit signifies page number.

When accessing internal registers via the two-wire serial interface, select the desired address space by programming the R240 register.

The MT9V112 accelerates mode-switching with hardware-assisted context switching, and supports taking snapshots, flash snapshots, and video clips using a configurable sequencer.

The MT9V112 supports a range of color formats derived from four primary color representations: YCbCr, RGB, raw Bayer (unprocessed, directly from the sensor), and processed Bayer (Bayer format data regenerated from processed RGB). The device also supports a variety of output signaling/timing options:

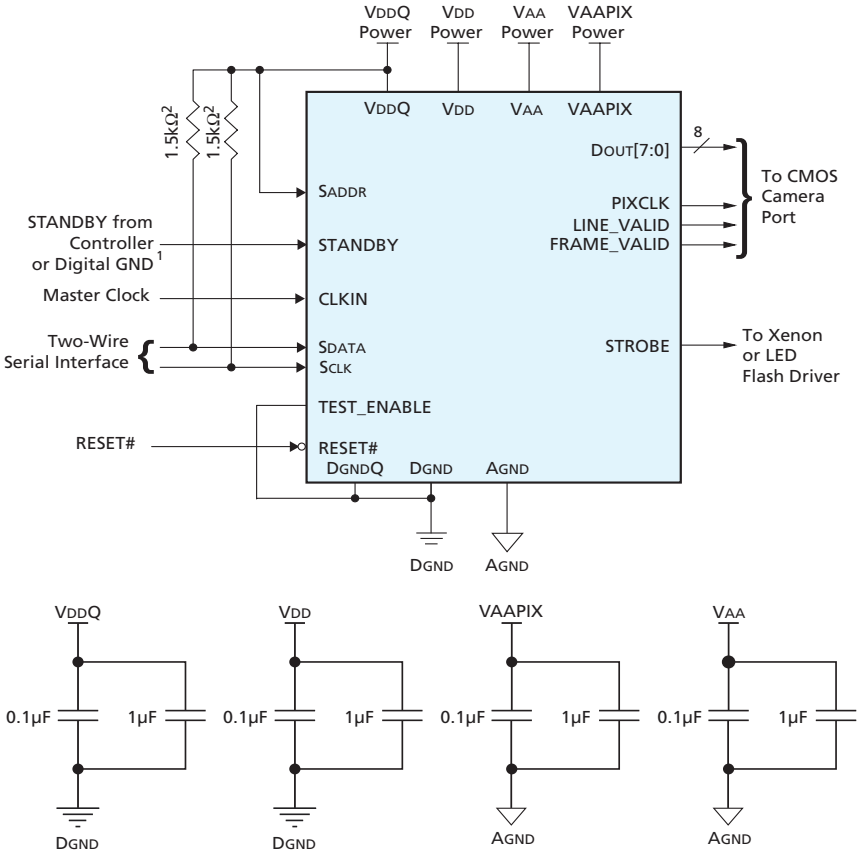
- Standard FRAME_VALID/LINE_VALID video interface with gated pixel clocks
- ITU-R BT.656 marker-embedded video interface with either gated or uniform pixel clocking

Typical Connections

Figure 3, Typical Configuration (connection), on page 9 shows typical MT9V112 device connections. For low-noise operation, the MT9V112 requires separate power supplies for analog and digital. Incoming digital and analog ground conductors can be tied together next to the die. Both power supply rails should be decoupled to ground using capacitors. The use of inductance filters is not recommended.

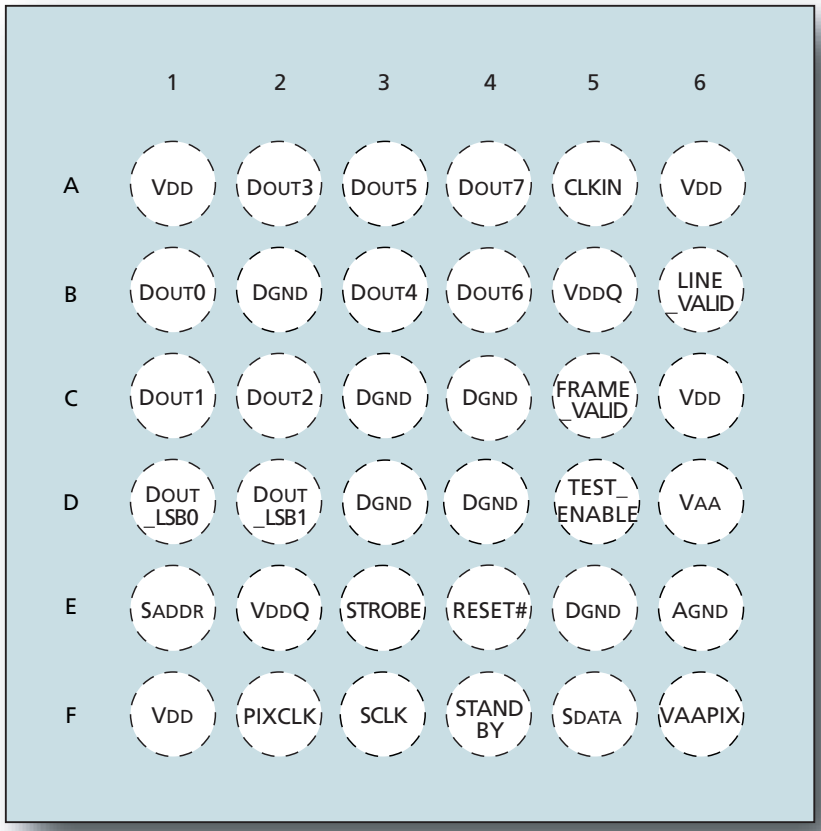
The MT9V112 also supports different digital core (VDD/DGND) and I/O power (VDDQ/DGND) power domains that can be at different voltages.

Figure 3: Typical Configuration (connection)



Notes:
1. MT9V112 STANDBY can be connected to customer's ASIC controller directly or to Digital GND, depending on the capability of the controller.
2. A 1.5KΩ resistor value is recommended, but may be greater for slower two-wire speed.

Figure 4: 36-Ball ICSP Assignment



Top View
(Ball Down)

Table 3: Ball Descriptions

Ball Assignment	Name	Type	Description	Notes
A5	CLKIN	Input	Master clock in sensor.	–
E4	RESET#	Input	Active LOW: Active LOW: RESET.	2
E1	SADDR	Input	Two-Wire Serial Interface Device ID selection 1:0xBA, 0:0x90.	–
D5	TEST_ENABLE	Input	Tie to DGND for normal operation. (Manufacturing use only.)	–
F3	SCLK	Input	Two-Wire Serial Interface Clock.	–
F4	STANDBY	Input	Multifunctional signal to control device addressing, power-down, and state functions (covering output enable function).	–
F5	SDATA	Input/Output	Two-Wire Serial Interface Data I/O.	–
B1, C1, C2, A2, B3, A3, B4, A4	DOUT[7:0]	Output	Pixel Data Output bit 0, DOUT[7] (most significant bit (MSB)), DOUT[0] (least significant bit (LSB)).	1
D1	DOUT_LSB0	Output	Sensor bypass mode output 0—typically left unconnected for normal SOC operation.	–
D2	DOUT_LSB1	Output	Sensor bypass mode output 1—typically left unconnected for normal SOC operation.	–
C5	FRAME_VALID	Output	Active HIGH: FRAME_VALID; indicates active frame.	–
B6	LINE_VALID	Output	Active HIGH: LINE_VALID, DATA_VALID; indicates active pixel.	–
F2	PIXCLK	Output	Pixel clock output.	–
E3	STROBE	Output	Active HIGH: STROBE (Xenon) or turn on (LED) flash.	–
E6	AGND	Supply	Analog ground.	–
B2, C3, C4, D3, D4, E5	DGND	Supply	Core digital ground.	–
D6	VAA	Supply	Analog power: 2.5V–3.1V (2.8V nominal).	–
F6	VAAPIX	Supply	Pixel array analog power supply: 2.5V–3.1V (2.8V nominal).	–
A1, A6, C6, F1	VDD	Supply	Core digital power: 1.7V–1.9V or 2.5V–3.1V (1.8V or 2.8V nominal).	–
B5, E2	VDDQ	Supply	I/O digital power: 1.7V–3.1V (VDD nominal).	–

Notes:
1. DOUT[7:0] are implemented with bidirectional buffers. Care must be taken that all inputs are driven and all outputs are driven if tri-stated.
2. A proper reset sequence requires an active CLKIN signal after the RESET# signal has been driven low. For more details about the reset sequence refer to the MT9V112 Developer Guide.

Output Data Ordering

Data ordering formats are defined in the following tables.

Table 4: Data Ordering in YCbCr Mode

Mode	Byte	Byte + 1	Byte +	Byte + 3
Default	Cbi	Yi	Cri	Yi+1
Swap CrCb	Cri	Yi	Cbi	Yi+1
SwapYC	Yi	Cbi	Yi+1	Cri
Swap CrCb, SwapYC	Yi	Cri	Yi+1	Cbi

Table 5: Output Data Ordering in Processed Bayer Mode

Mode	Line	Byte	Byte + 1	Byte + 2	Byte + 3
Default	First	Gi	Ri+1	Gi+2	Ri+3
	Second	Bi	Gi+1	Bi+2	Gi+3
Flip Bayer Col	First	Ri	Gi+1	Ri+2	Gi+3
	Second	Gi	Bi+1	Gi+2	Bi+3
Flip Bayer Row	First	Bi	Gi+1	Bi+2	Gi+3
	Second	Gi	Ri+1	Gi+2	Ri+3
Flip Bayer Col, Flip Bayer Row	First	Gi	Bi+1	Gi+2	Bi+3
	Second	Ri	Gi+1	Ri+2	Gi+3

Table 6: Output Data Ordering in RGB Mode

Mode (Swap disabled)	Byte	D7	D6	D5	D4	D3	D2	D1	D0
RGB565	First	R7	R6	R5	R4	R3	G7	G6	G5
	Second	G4	G3	G2	B7	B6	B5	B4	B3
RGB555	First	0	R7	R6	R5	R4	R3	G7	G6
	Second	G5	G4	G3	B7	B6	B5	B4	B3
RGB444x	First	R7	R6	R5	R4	G7	G6	G5	G4
	Second	B7	B6	B5	B4	0	0	0	0
RGBx444	First	0	0	0	0	R7	R6	R5	R4
	Second	G7	G6	G5	G4	B7	B6	B5	B4

Table 7: Output Data Ordering in (8 + 2) Bypass Mode

Mode	Byte	D7	D6	D5	D4	D3	D2	D1	D0
8 + 2 bypass	First	B9	B8	B7	B6	B5	B4	B3	B2
	Second	0	0	0	0	0	0	B1	B0

Table 8: Colorpipe Registers – Address Page 1

Register # Decimal (HEX)	Register Name	Data Format	Default Value Decimal (HEX)	Module
5 (0x05)	Aperture Correction	0000 0000 0000 dddd	3 (0x0003)	Interp
6 (0x06)	Operating Mode Control	dddd dddd 0ddd dddd	28686 (0x700E)	Cfg
8 (0x08)	Output Format Control	0000 0ddd dddd dddd	128 (0x0080)	Cfg
37 (0x25)	Color Saturation Control	0000 0000 00dd dddd	5 (0x0005)	rgb2yuv
52 (0x34)	Luma Offset	dddd dddd dddd dddd	16 (0x0010)	CamInt
53 (0x35)	Luma Clip	dddd dddd dddd dddd	61456 (0xF010)	CamInt
58 (0x3A)	Output Format Control 2A	0ddd dddd dddd dddd	512 (0x0200)	CamInt
59 (0x3B)			1066 (0x042A)	LensCorr
60 (0x3C)			1024 (0x0400)	LensCorr
71 (0x47)			24 (0x0018)	
72 (0x48)	test Pattern Generator Control	0000 0000 d000 0ddd	0 (0x0000)	FifoInt
83 (0x53)			7700 (0x1E14)	GmaCorr
84 (0x54)			17966 (0x462E)	GmaCorr
85 (0x55)			34666 (0x876A)	GmaCorr
86 (0x56)			47008 (0xB7A0)	GmaCorr
87 (0x57)			57548 (0xE0CC)	GmaCorr
88 (0x58)			0 (0x0000)	GmaCorr
104 (0x68)	Reserved	—	17 (0x0011)	—
128 (0x80)			3 (0x0003)	LensCorr
129 (0x81)			0 (0x0000)	LensCorr
130 (0x82)			0 (0x0000)	LensCorr
131 (0x83)			0 (0x0000)	LensCorr
132 (0x84)			0 (0x0000)	LensCorr
133 (0x85)			0 (0x0000)	LensCorr
134 (0x86)			0 (0x0000)	LensCorr
135 (0x87)			0 (0x0000)	LensCorr
136 (0x88)			0 (0x0000)	LensCorr
137 (0x89)			0 (0x0000)	LensCorr
138 (0x8A)			0 (0x0000)	LensCorr
139 (0x8B)			0 (0x0000)	LensCorr
140 (0x8C)			0 (0x0000)	LensCorr
141 (0x8D)			0 (0x0000)	LensCorr

Table 8: Colorpipe Registers – Address Page 1 (Continued)

Register # Decimal (HEX)	Register Name	Data Format	Default Value Decimal (HEX)	Module
142 (0x8E)			0 (0x0000)	LensCorr
143 (0x8F)			0 (0x0000)	LensCorr
144 (0x90)			0 (0x0000)	LensCorr
145 (0x91)			0 (0x0000)	LensCorr
146 (0x92)			0 (0x0000)	LensCorr
147 (0x93)			0 (0x0000)	LensCorr
148 (0x94)			0 (0x0000)	LensCorr
149 (0x95)			0 (0x0000)	LensCorr
153 (0x99)	Line Counter	???? ???? ???? ????	N/A	CamInt
154 (0x9A)	Frame Counter	???? ???? ???? ????	N/A	CamInt
155 (0x9B)	Output Format Control 2—Context B	0ddd dddd dddd dddd	512 (0x0200)	CamInt
157 (0x9D)			9390 (0x24AE)	—
159 (0x9F)	Reserved—obsolete	—	0 (0x0000)	–
160 (0xA0)	Reserved—obsolete	—	640 (0x0280)	–
161 (0xA1)	Reducer Horizontal Size Resize—Context B	0000 0ddd dddd dddd	480 (0x01E0)	Interp
162 (0xA2)	Reserved—obsolete	—	0 (0x0000)	–
163 (0xA3)	Reserved—obsolete	—	480 (0x01E0)	–
164 (0xA4)	Reducer Vertical Size Resize—Context B	0000 0ddd dddd dddd	480 (0x01E0)	Interp
165 (0xA5)	Reducer Horizontal Pan Resize	0d00 0ddd dddd dddd	0 (0x0000)	Interp
166 (0xA6)	Reducer Horizontal Zoom Resize	0000 0ddd dddd dddd	640 (0x0280)	Interp
167 (0xA7)	Reducer Horizontal Size Resize—Context A	0000 0ddd dddd dddd	320 (0x0140)	Interp
168 (0xA8)	Reducer Vertical Pan Resize	0d00 0ddd dddd dddd	0 (0x0000)	Interp
169 (0xA9)	Reducer Vertical Zoom Resize	0000 0ddd dddd dddd	480 (0x01E0)	Interp
170 (0xAA)	Reducer Vertical Size Resize—Context A	0000 0ddd dddd dddd	240 (0x00F0)	Interp
171 (0xAB)	Reducer Current Zoom Horizontal	0000 0??? ???? ????	640 (0x0280)	Interp
172 (0xAC)	Reducer Current Zoom Vertical	0000 0??? ???? ????	480 (0x01E0)	Interp
174 (0xAE)	Reducer Zoom Step Size	dddd dddd dddd dddd	3081 (0x0C09)	Interp
175 (0xAF)	Reducer Zoom Control	0000 00dd 0ddd dddd	0 (0x0000)	Interp
180 (0xB4)	Reserved	—	32 (0x0020)	—
182 (0xB6)			0 (0x0000)	LensCorr
183 (0xB7)			0 (0x0000)	LensCorr
184 (0xB8)			0 (0x0000)	LensCorr
185 (0xB9)			0 (0x0000)	LensCorr
186 (0xBA)			0 (0x0000)	LensCorr
187 (0xBB)			0 (0x0000)	LensCorr
188 (0xBC)			0 (0x0000)	LensCorr
189 (0xBD)			0 (0x0000)	LensCorr
190 (0xBE)			0 (0x0000)	LensCorr

Table 8: Colorpipe Registers – Address Page 1 (Continued)

Register # Decimal (HEX)	Register Name	Data Format	Default Value Decimal (HEX)	Module
191 (0xBF)			0 (0x0000)	LensCorr
192 (0xC0)			0 (0x0000)	LensCorr
193 (0xC1)			0 (0x0000)	LensCorr
194 (0xC2)			0 (0x0000)	LensCorr
195 (0xC3)			0 (0x0000)	LensCorr
196 (0xC4)			0 (0x0000)	LensCorr
200 (0xC8)	Global Context Control	dddd dddd dddd dddd	0 (0x0000)	CntxCtl
201 (0xC9)	Reserved	dddd dddd dddd dddd	0 (0x0000)	—
202 (0xCA)	Reserved	—	N/A	—
203 (0xCB)	Reserved	—	N/A	—
204 (0xCC)	Reserved	—	N/A	—
205 (0xCD)	Reserved	—	N/A	—
206 (0xCE)	Reserved	—	N/A	—
207 (0xC)	Reserved	—	N/A	—
208 (0xD0)	Reserved	—	N/A	—
220 (0xDC)			7700 (0x1E14)	GmaCorr
221 (0xDD)			17966 (0x462E)	GmaCorr
222 (0xDE)			34666 (0x876A)	GmaCorr
223 (0xDF)			47008 (0xB7A0)	GmaCorr
224 (0xE0)			57548 (0xE0CC)	GmaCorr
225 (0xE1)			0 (0x0000)	GmaCorr
226 (0xE2)	Effects Mode	dddd dddd 0000 0ddd	28672 (0x7000)	GmaCorr
227 (0xE3)	Effects Sepia	dddd dddd dddd dddd	45091 (0xB023)	GmaCorr

Note: 0 = “Don't Care” bit.
d = R/W bit
? = R/O bit.

Table 9: Camera Control Registers – Address Page 2

Register # Decimal (HEX)	Register Name	Data Format	Default Value Decimal (HEX)	Module
2 (0x02)			174 (0x00AE)	ColorCorr
3 (0x03)			10531 (0x2923)	ColorCorr
4 (0x04)			1188 (0x04A4)	ColorCorr
9 (0x09)			182 (0x00B6)	ColorCorr
10 (0x0A)			208 (0x00D0)	ColorCorr
11 (0x0B)			144 (0x0090)	ColorCorr
12 (0x0C)			217 (0x00D9)	ColorCorr
13 (0x0D)			150 (0x0096)	ColorCorr
14 (0x0E)			54 (0x0036)	ColorCorr
15 (0x0F)			77 (0x0073)	ColorCorr
16 (0x10)			93 (0x005D)	ColorCorr
17 (0x11)			201 (0x00C9)	ColorCorr
18 (0x12)			N/A	ColorCorr
19 (0x13)			N/A	ColorCorr
20 (0x14)			N/A	ColorCorr
21 (0x15)			73 (0x0049)	ColorCorr
22 (0x16)			23 (0x0017)	ColorCorr
23 (0x17)			1 (0x0011)	ColorCorr
24 (0x18)			46 (0x002E)	ColorCorr
25 (0x19)			52 (0x0034)	ColorCorr
26 (0x1A)			3 (0x0003)	ColorCorr
27 (0x1B)			62 (0x003E)	ColorCorr
28 (0x1C)			77 (0x004D)	ColorCorr
29 (0x1D)			90 (0x005A)	ColorCorr
30 (0x1E)			108 (0x006C)	AWB
31 (0x1F)			160 (0x00A0)	AWB
32 (0x20)			51220 (0xC814)	AWB
33 (0x21)			32896 (0x8080)	AWB
34 (0x22)			55648 (0xD960)	AWB
35 (0x23)			55648 (0xD960)	AWB
36 (0x24)			32512 (0x7F00)	AWB
38 (0x26)	Auto Exposure Horizontal Window Boundaries	dddd dddd dddd dddd	32768 (0x8000)	AE
39 (0x27)	Auto Exposure Vertical Window Boundaries	dddd dddd dddd dddd	32776 (0x8008)	AE
40 (0x28)			61218 (0xEF22)	AWB
41 (0x29)			36211 (0x8D73)	AWB
42 (0x2A)			208 (0x00D0)	AWB
43 (0x2B)	Auto Exposure Horizontal Center Window Boundaries	dddd dddd dddd dddd	24608 (0x6020)	AE
44 (0x2C)	Auto Exposure Vertical Center Window Boundaries	dddd dddd dddd dddd	24608 (0x6020)	AE
45 (0x2D)	AWB Window Boundaries	dddd dddd dddd dddd	61600 (0xF0A0)	AWB
46 (0x2E)	Auto Exposure target and Precision Control	dddd dddd dddd dddd	3146 (0x0C4A)	AE
47 (0x2F)	Auto Exposure Speed and Sensitivity Control—Context A	dddd dddd dddd dddd	57120 (0xDF20)	AE
48 (0x30)			N/A	AWB

Table 9: Camera Control Registers – Address Page 2 (Continued)

Register # Decimal (HEX)	Register Name	Data Format	Default Value Decimal (HEX)	Module
49 (0x31)			N/A	AWB
50 (0x32)			N/A	AWB
51 (0x33)			5230 (0x146E)	AE
54 (0x36)			30736 (0x7810)	AE
55 (0x37)			768 (0x0300)	AE
56 (0x38)			1088 (0x0440)	AE
57 (0x39)			1702 (0x06A6)	AE
58 (0x3A)			1702 (0x06A6)	AE
59 (0x3B)			1371 (0x055B)	AE
60 (0x3C)			1371 (0x055B)	AE
61 (0x3D)			6105 (0x17D9)	AE
62 (0x3E)			7423 (0x1CFF)	AWB
63 (0x3F)			N/A	AE
70 (0x46)			55552(0xD900)	AE
75 (0x4B)	Reserved	—	0 (0x0000)	—
76 (0x4C)			N/A	AE
77 4D)			N/A	AE
79 (0x4F)	Reserved	—	0 (0x0000)	—
87 (0x57)			470 (0x01D6)	AE
88 (0x58)			564 (0x0234)	AE
89 (0x59)			1970 (0x01D6)	AE
90 (0x5A)			564 (0x0234)	AE
91 (0x5B)	Flicker Control 0	?000 0000 0000 0ddd	2 (0x0002)	FD
92 (0x5C)			4108 (0x100C)	FD
93 (0x5D)			5392 (0x1510)	FD
94 (0x5E)			26952 (0x6948)	ColorCorr
95 (0x5F)			14632 (0x3928)	ColorCorr
96 (0x60)			2 (0x0002)	ColorCorr
97 (0x61)			32896 (0x8080)	
98 (0x62)	Auto Exposure Digital Gains Monitor	???? ???? ???? ????	4112 (0x1010)	AE
99 (0x63)	Reserved	—	N/A	—
100 (0x64)	Reserved	—	23036(0x59FC)	—
101 (0x65)			0 (0x000)	AE
103 (0x67)	Auto Exposure Digital Gain Limits	dddd dddd dddd dddd	16400 (0x4010)	AE
104 (0x68)	Reserved	—	17 (0x0011)	—
106 (0x6A)	Reserved	—	N/A	—
107 (0x6B)	Reserved	—	N/A	—
108 (0x6C)	Reserved	—	N/A	—
109 (0x6D)	Reserved	—	N/A	—
110 (0x6E)	Reserved	—	N/A	—
111 (0x6F)	Reserved	—	N/A	—
112 (0x70)	Reserved	—	N/A	—
113 (0x71)	Reserved	—	N/A	—
114 (0x72)	Reserved	—	N/A	—
115 (0x73)	Reserved	—	N/A	—

Table 9: Camera Control Registers – Address Page 2 (Continued)

Register # Decimal (HEX)	Register Name	Data Format	Default Value Decimal (HEX)	Module
116 (0x74)	Reserved	—	N/A	—
117 (0x75)	Reserved	—	N/A	—
118 (0x76)	Reserved	—	N/A	—
119 (0x77)	Reserved	—	N/A	—
120 (0x78)	Reserved	—	N/A	—
121 (0x79)	Reserved	—	N/A	—
122 (0x7A)	Reserved	—	N/A	—
123 (0x7B)	Reserved	—	N/A	—
124 (0x7C)	Reserved	—	N/A	—
125 (0x7D)	Reserved	—	N/A	—
130 (0x82)			1020 (0x03FC)	AE
131 (0x83)			769 (0x0301)	AE
132 (0x84)			193 (0x00C1)	AE
133 (0x85)			929 (0x03A1)	AE
134 (0x86)			980 (0x03D4)	AE
135 (0x87)			983 (0x03D7)	AE
136 (0x88)			921 (0x0399)	AE
137 (0x89)			1016 (0x03F8)	AE
138 (0x8A)			28 (0x001C)	AE
139 (0x8B)			957 (0x03BD)	AE
140 (0x8C)			987 (0x03DB)	AE
141 (0x8D)			957 (0x03BD)	AE
142 (0x8E)			1020 (0x03FC)	AE
143 (0x8F)			990 (0x03DE)	AE
144 (0x90)			990 (0x03DE)	AE
145 (0x91)			990 (0x03DE)	AE
146 (0x92)			990 (0x03DE)	AE
147 (0x93)			31 (0x001F)	AE
148 (0x94)			65 (0x0041)	AE
149 (0x95)			867 (0x0363)	AE
150 (0x96)	Reserved	—	0 (0x0000)	—
151 (0x97)	Reserved	—	N/A	—
152 (0x98)	Reserved	—	255 (0x00FF)	—
153 (0x99)	Reserved	—	1 (0x0001)	—
156 (0x9C)	Auto Exposure Speed and Sensitivity—Context B	dddd dddd dddd dddd	57120 (0xDF20)	AE
180 (0xB4)	Reserved	—	32 (0x0020)	—
181 (0xB5)	Reserved	—	N/A	—
198 (0xC6)	Reserved	—	0 (0x0000)	—
199 (0xC7)	Reserved	—	N/A	—
200 (0xC8)	Global Context Control	dddd dddd dddd dddd	0 (0x0000)	CntxCtl
201 (0xC9)		—	N/A	CntxCtl
202 (0xCA)		—	N/A	CntxCtl
203 (0xCB)		—	0 (0x0000)	CntxCtl
204 (0xCC)			0 (0x0000)	CntxCtl

Table 9: Camera Control Registers – Address Page 2 (Continued)

Register # Decimal (HEX)	Register Name	Data Format	Default Value Decimal (HEX)	Module
205 (0xCD)			2190 (0x21A0)	CntxCtl
206 (0xCE)			7835 (0x1E9B)	CntxCtl
207 (0xCF)			19018(0x4A4A)	CntxCtl
208 (0xD0)			5773 (0x168D)	CntxCtl
209 (0xD1)			77 (0x004D)	CntxCtl
210 (0xD2)			0 (0x0000)	CntxCtl
211 (0xD3)			0 (0x0000)	CntxCtl
212 (0xD4)			520 (0x0208)	CntxCtl
213 (0xD5)			0 (0x0000)	CntxCtl
239 (0xEF)			8 (0x0008)	AWB
242 (0xF2)			0 (0x0000)	AWB
243 (0xF3)	Reserved	—	0 (0x0000)	—
245 (0xF5)			135 (0x0040)	ColorCorr
246 (0xF6)			127 (0x007F)	ColorCorr
255 (0xFF)			43136(0xA880)	ColorCorr

Note: 0 = “Don't Care” bit. The exceptions: R0:0 and R255:0, which are hardwired R/O binary values.

d = R/W bit

? = R/O bit.

Image Flow Processor Register Description

Configuration

The vast majority of IFP registers associate to one of the IFP modules. These modules are identified in Table 8 on page 13 and in Table 9 on page 16. Detailed register descriptions follow in Table 10 below and in Table 11 on page 27. A few registers create effects across a number of module functions. These include R240 page map register (R/W); R6:1 0x106 operating mode control register (R/W); R8:1 0x108 output format control register (R/W); the R62:2 0x23E gain types and CCM threshold register—the gain threshold for CCM adjustment (R/W).

Table 10: Colorpipe Register Description

Bit Fields	Description
R5:1—0x105 – Aperture Correction	
Default	0x0003
Description	Aperture correction scale factor used for sharpening.
Bit 3	Enables automatic sharpness reduction control (see R51:2 0x233).
Bits 2:0	Sharpening factor: 000: No sharpening. 001: 25% sharpening. 010: 50% sharpening. 011: 75% sharpening. 100: 100% sharpening. 101: 125% sharpening. 110: 150% sharpening. 111: 200% sharpening.
R6:1—0x106 – Operating Mode Control (R/W)	
Default	0x700E
Description	this register specifies the operating mode of the IFP.
Bit 15	Enables manual white balance. User can set the base matrix and color channel gains. this bit must be asserted and de-asserted with a frame in between to force new color correction settings to take effect.
Bit 14	Enables auto exposure.
Bit 13	Enables on-the-fly defect correction.
Bit 12	Reserved—obsolete. The user should write a “0” to this bit.
Bit 11	not used.
Bit 10	Enables lens shading correction. 1: Enables lens shading correction.
Bits 9:8	Reserved.
Bit 7	Enables flicker detection. 1: Enables automatic flicker detection.
Bit 6	Reserved for future expansion.
Bit 5	Reserved.
Bit 4	Bypasses color correction matrix. 0: Normal color processing. 1: Outputs “raw” color bypassing color correction.
Bits 3:2	Auto exposure back light compensation control. 00: Auto exposure sampling window is specified by R38:2 and R39:2 (“large window”). 01: Auto exposure sampling window is specified by R43:2 and R44:2 (“small window”). 1X: Auto exposure sampling window is specified by the weighted sum of the large window and the small window, with the small window weighted four times more heavily. (X = “0” or “1”.)

Table 10: Colorpipe Register Description (Continued)

Bit Fields	Description
Bit 1	Enables auto white balance. 0: Freezes white balance at current values. 1: Enables auto white balance.
Bit 0	Reserved for future expansion.
R8:1—0X108 – Output Format Control (R/W)	
Default	0x0080
Description	This register specifies the output timing and format in conjunction with R58:1 or R155:1 (depending on the context).
Bits 15:11	Reserved for future expansion.
Bit 10	Gate PIXCLK. 0: PIXCLK not gated. 1: PIXCLK gated with LINE_VALID.
Bit 9	Flip Bayer columns in processed Bayer output mode. 0: Column order is green, red and blue, green. 1: Column order is red, green and green, blue.
Bit 8	Flip Bayer row in processed Bayer output mode. 0: First row contains green and red; the second row contains blue and green. 1: First row contains blue and green; the second row contains green and red.
Bit 7	Controls the values used for the protection bits in Rec. ITU-R BT.656 codes. 0: Use zeros for the protection bits. 1: Use the correct values.
Bit 5	Multiplexes Y (in YCbCr mode) or green (in RGB mode) channel on all channels (monochrome). 1: Forces Y/G onto all channels.
Bit 4	Disables Cb color output channel (Cb = 128) in YCbCr mode and disables the blue color output channel (B = 0) in RGB mode. 1: Forces Cab to 128 or B to 0.
Bit 3	Disables Y color output channel (Y = 128) in YCbCr and disables the green color output channel (G = 0) in RGB mode. 1: Forces Y to 128 or G to 0.
Bit 2	Disables Cr color output channel (Cr = 128) in YCbCr mode and disables the red color output channel (R = 0) in RGB mode. 1: Forces Cr to 128 or R to 0.
Bit 1	Toggles the assumptions about Bayer vertical CFA shift. 0: Row containing red comes first. 1: Row containing blue comes first.
Bit 0	Toggles the assumptions about Bayer horizontal CFA shift. 0: Green comes first. 1: Red or blue comes first.
R37:1—0x125 – Color Saturation Control (R/W)	
Default	0x0005
Description	This register specifies the color saturation control settings.
Bit 5:3	Specify overall attenuation of the color saturation. 000: Full color saturation 001: 75% of full saturation 010: 50% of full saturation 011: 37.5% of full saturation 100: 25% of full saturation 101: 150% of full saturation 110: Black and white

Table 10: Colorpipe Register Description (Continued)

Bit Fields	Description
Bit 2:0	Specify color saturation attenuation at high luminance (linearly increasing attenuation from no attenuation to monochrome at luminance of 224). 000: No attenuation. 001: Attenuation starts at luminance of 216. 010: Attenuation starts at luminance of 208. 011: Attenuation starts at luminance of 192. 100: Attenuation starts at luminance of 160. 101: Attenuation starts at luminance of 96.
R52:1—0x134 – Luma Offset (can be used to control brightness) (R/W)	
Default	0x0010
Description	Offset added to the luminance prior to output.
Bits 15:8	Offset in RGB mode.
Bits 7:0	Y Offset in YCbCr mode.
R53:1—0x135 – Luma Clip (R/W)	
Default	0xF010
Description	Clipping limits for output luminance.
Bits 15:8	Highest value of output luminance.
Bits 7:0	Lowest value of output luminance.
R58:1—0x13A – Output Format Control 2—Context A (R/W)	
Default	0x0200
Description	Output format control 2—context A.
Bit 14	Output processed Bayer data.
Bit 13	Debug flicker luma.
Bit 12	
Bit 11	Enables embedding Rec. ITU-R BT.656 synchronization codes in the output data. See R155:1.
Bit 10	Entire image processing is bypassed and raw Bayer is output directly. In YCbCr or RGB mode: 0: Normal operation, sensor core data flows through IFP. 1: Bypass IFP and output Imager data directly (full 10 bits). The image data still passes through the camera interface FIFO and the 10 bits are formatted to two output bytes through the camera interface; i.e., 8 + 2. Data rate is effectively the same as default 16-bit /per pixel modes. Auto exposure/AWB, etc., still function and control the sensor, though they are assuming some gain/correction through the colorpipe. See R155:1.
Bit 9	Inverts output pixel clock. By default, this bit it asserted and data is launched off the falling edge of PIXCLK for capture by the receiver on the rising edge. See R155:1.
Bit 8	Enables RGB output. 0: Output YCbCr data. 1: Output RGB format data as defined by R58:1[7:6].
Bits 7:6	RGB output format: 00: 16-bit RGB565. 01: 15-bit RGB555. 10: 12-bit RGB444x. 11: 12-bit RGBx444.
Bits 5:4	test Ramp output: 00: Off. 01: By column. 10: By row. 11: By frame.
Bit 3	Outputs RGB or YCbCr values are shifted 3 bits up. Use with R58:1[5:4] to test LCDs with low color depth.

Table 10: Colorpipe Register Description (Continued)

Bit Fields	Description
Bit 2	Averages two nearby chrominance bytes. See R155:1.
Bit 1	In YCbCr mode swap C and Y bytes. In RGB mode, swap odd and even bytes. See R155:1.
Bit 0	In YCbCr mode, swaps Cb and Cr channels. In RGB mode, swaps R and B channels. See R155:1.
R72:1—0x148 - Test Pattern Generator control (R/W)	
Default	0x0000
Description	This register enables test pattern generation at the input of the image processor. Values greater than "0" turn on the test pattern generator. The brightness of the flat-color areas depends on the value programmed (from 6–1) in this register. The value 7 produces the color bar pattern. Value 0 selects the sensor image.
Bit 7	Test pattern selection.
Bits 2:0	0: Normal operation. 1: Forces WB digital gains to 1.0.
R153:1—0x199 – Line Counter (R/O)	
Default	N/A
Description	Use line counter to determine the number of the line currently being output.
Bits 15:0	Line count.
R154:1—0x19A – Frame Counter (R/O)	
Default	N/A
Description	Use frame counter to determine the index of the frame currently being output.
Bits 15:0	Frame count.
R155:1—0x19B – Output Format Control 2—Context B (R/W)	
Default	0x0200
Description	Output format control 2—context B.
Bit 14	Output processed Bayer data.
Bit 13	Reserved.
Bit 12	
Bit 11	Enables embedding Rec. ITU-R BT.656 synchronization codes to the output data. See R58:1.
Bit 10	Entire image processing is bypassed and raw Bayer is output directly. In YCbCr or RGB mode: 0: Normal operation, sensor core data flows through IFP. 1: Bypass IFP and output Imager data directly (full 10 bits). The image data still passes through the camera interface FIFO and the 10 bits are formatted to two output bytes through the camera interface; i.e., 8 + 2. Data rate is effectively the same as default 16-bit /per pixel modes. auto exposure/AWB, etc. still function and control the sensor, though they are assuming some gain/correction through the colorpipe. See R58:1.
Bit 9	Inverts output pixel clock. By default, this bit it asserted and data is launched off the falling edge of PIXCLK for capture by the receiver on the rising edge. See R58:1.
Bit 8	Enables RGB output. 0: Output YCbCr data. 1: Output RGB format data as defined by R155:1[7:6]. See R58:1.
Bits 7:6	RGB output format: 00: 16-bit RGB565. 01: 15-bit RGB555. 10: 12-bit RGB444x. 11: 12-bit RGBx444.
Bits 5:4	Test Ramp output: 00: Off. 01: By column. 10: By row. 11: By frame.

Table 10: Colorpipe Register Description (Continued)

Bit Fields	Description
Bit 3	Output RGB or YCbCr values are shifted 3 bits up. Use with R58:1[5:4] to test LCDs with low color depth.
Bit 2	Averages two nearby chrominance bytes. See R58:1
Bit 1	In YCbCr mode swap C and Y bytes. In RGB mode, swap odd and even bytes. See R58:1.
Bit 0	In YCbCr mode, swaps Cb and Cr channels. In RGB mode, swaps R and B channels. See R58:1.
R161:1—0x1A1 – Reducer Horizontal Output Size —Context B (R/W)	
Default	0x0280
Description	Controls reducer horizontal output size in Context B (Sensor Window Width >= Reducer Zoom Window Width >= Reducer Horizontal Output Size).
Bits 10:0	X Size.
R164:1—0x1A4 – Reducer Vertical Output Size —Context B (R/W)	
Default	0x01E0
Description	Controls reducer vertical output size in context B. (Sensor Window Height >= Reducer Zoom Window Height >= Reducer Vertical Output Size).
Bits 10:0	Y Size.
R165:1—0x1A5 – Reducer Horizontal Pan Resize (R/W)	
Default	0x0000
Description	Controls reducer horizontal pan. Pan and Zoom settings are not context switchable. The same field of view is active for both context A and context B.
Bit 14	0: MT9V112-compatible offset from X = 0. 1: Centered origin at 320 for more convenient zoom and resize.
Bits 10:0	X Pan: Unsigned offset from X = 0 (Bit 14 = 0), or two's complement from X = 320 (Bit 14 = 1).
R166:1—0x1a6 – Reducer Horizontal Zoom Resize (R/W)	
Default	0x0280
Description	Controls reducer horizontal zoom. Pan and Zoom settings are not context switchable. The same field of view is active for both context A and context B.
Bits 10:0	X Zoom.
R167:1—0x1a7 – Reducer Horizontal Output Size Resize—Context A (R/W)	
Default	0x0140
Description	Controls reducer horizontal output size in context A.
Bits 10:0	X Size.
R168:1—0x1A8 – Reducer Vertical Pan Resize (R/W)	
Default	0x0000
Description	Controls reducer vertical pan. Pan and Zoom settings are not context switchable. The same field of view is active for both context A and context B.
Bit 14	0: MT9V112-compatible origin at Y = 0. 1**:** Centered origin at Y = 240 for more convenient zoom and resize.
Bits 10:0	Y Pan: unsigned offset from y = 0 (Bit 14 = 0), or two's complement from Y = 240 (Bit 14 = 1).
R169:1—0x1A9 – Reducer Vertical Zoom Resize (R/W)	
Default	0x0IE0
Description	Controls reducer vertical zoom. Pan and Zoom settings are not context switchable. The same field of view is active for both context A and context B.
Bits 10:0	Y Zoom.
R170:1—0x1AA – Reducer Vertical Output Size Resize—Context A (R/W)	
Default	0x00F0
Description	Controls reducer vertical output size in context A.
Bits 10:0	Y Size.
R171:1—0x1AB – Reducer Current Horizontal Zoom (R/O)	

Table 10: Colorpipe Register Description (Continued)

Bit Fields	Description
Default	0x0280
Description	Current horizontal zoom.
Bits 13:12	IR X shift. 0: No IR 1: 2x 2: 4x 3: 8x
Bits 11:0	Current zoom window width. After automatic zoom (R175:1), copy R171:1 to the snapshot X Zoom register R166:1 (context A) or R160:1 (context B) so the snapshot has the same field of view as preview. Also copy to snapshot X Size register R167:1 (context A) or R161 (context B) for largest snapshot.
R172:1—0x1AC – Reducer Current Vertical Zoom (R/O)	
Default	0x01E0
Description	Current vertical zoom.
Bits 13:12	IR Y Shift. 0: No IR 1: 2x 2: 4x 3: 8x
Bits 11:0	Current zoom window height. After automatic zoom (R175:1), copy R172:1 to the snapshot Y Zoom register R169:1 (context A) or R163:1 (context B) so the snapshot has the same field of view as preview. Also copy to snapshot X Size register R170:1 (context A) or R164 (context B) for largest snapshot.
R174:1—0x1AE – Reducer Zoom Step Size (R/W)	
Default	0x0C09
Description	Zoom step sizes. Should be a multiple of the aspect ratio 5:4 for VGA or 4:3 VGA or 11:9 for CIF.
Bits 15:8	Zoom step size in X.
Bits 7:0	Zoom step size in Y.
R175:1—0x1AF – Reducer Zoom Control (R/W)	
Default	0x0000
Description	Resize Interpolation and zoom control.
Bit 15:10	Reserved.
Bit 9	Starts automatic “zoom out” in step sizes defined in R174:1.
Bit 8	Starts automatic “zoom in” in step sizes defined in R174:1.
Bit 7:0	Reserved.
R200:1—0x1C8 – Global Context Control (R/W)	
Default	0x0000
Description	Defines sensor and colorpipe context for current frame. Registers R200:0, R200:1, and R200:2 are shadows of each other. See description in R200:2. It is recommended that all updates to R200:n are handled by means of a write to R200:2.
Bit 15:0	See R200:2[15:0].
R226:1—0x1E2 – Effects Mode (R/W)	
Default	0x7000
Description	This register specifies which of several special effects to apply to each pixel passing through the pixel pipe.
Bits 15:8	Solarization threshold.

Table 10: Colorpipe Register Description (Continued)

Bit Fields	Description
Bits 2:0	Specification of the effects mode. 000: No effect (pixels pass through unchanged). 001: Monochrome (chromas set to 0). 010: Sepia (chromas set to the value in the effects sepia register). 011: Negative (all color channels inverted). 100: Solarize (luma conditionally inverted). 101: Solarize2 (luma conditionally inverted, chromas inverted when luma inverted).
R227:1—0x1E3 – Effects Sepia (R/W)	
Default	0xB023
Description	This register specifies the chroma values for the sepia effect. In sepia mode, the chroma values of each pixel are set to this value. By default, this register contains a brownish color, but it can be set to an arbitrary color.
Bit 15	Sign of Cb.
Bits 14:8	Magnitude of Cb in 0.7 fixed point.
Bit 7	Sign of Cr.
Bits 6:0	Magnitude of Cr in 0.7 fixed point.

Table 11: Camera Control Register Description

Bit Fields	Description
R38:2—0x226 – Auto Exposure Horizontal Window Boundaries (R/W)	
Default	0x8000
Description	This register specifies the left and right boundaries of the window used by the auto exposure measurement engine. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the right-most edge of the frame, 64 (decimal) is the middle of the frame, and 0 is the left-most edge of the frame.
Bits 15:8	Right window boundary.
Bits 7:0	Left window boundary.
R39:2—0x227 – Auto Exposure Vertical Window Boundaries (R/W)	
Default	0x8008
Description	This register specifies the top and bottom boundaries of the window used by the auto exposure measurement engine. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the bottom edge of the frame, 64 (decimal) is the middle of the frame, and 0 is the top edge of the frame.
Bits 15:8	Bottom window boundary.
Bits 7:0	Top window boundary.
R43:2—0x22B – Auto Exposure Horizontal Center Window Boundaries (R/W)	
Default	0x6020
Description	This register specifies the left and right boundaries of the window used by the auto exposure measurement engine in back light compensation mode. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the right-most edge of the frame, 64 (decimal) is the middle of the frame, and 0 is the left-most edge of the frame.
Bits 15:8	Right window boundary.
Bits 7:0	Left window boundary.
R44:2—0x22C – Auto Exposure Vertical Center Window Boundaries (R/W)	
Default	0x6020
Description	This register specifies the top and bottom boundaries of the window used by the auto exposure measurement engine in back light compensation mode. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the bottom edge of the frame, 64 (decimal) is the middle of the frame, and “0” is the top edge of the frame.
Bits 15:8	Bottom window boundary.
Bits 7:0	top window boundary.
R45:2—0x22D – AWB Window Boundaries (R/W)	
Default	0xF0A0
Description	This register specifies the boundaries of the window used by the AWB measurement engine. Essentially, it describes the AWB measurement window in terms relative to the size of the image—horizontally, in units of 1/10ths of the width of the image; vertically, in units of 1/16 of the height of the image. So although the positioning is highly quantized, the window remains roughly in place as the resolution changes.
Bits 15:12	Bottom window boundary (in units of blocks).
Bits 11:8	top window boundary (in units of blocks).
Bits 7:4	Right window boundary (in units of 2 blocks).
Bits 3:0	Left window boundary (in units of 2 blocks).
R46:2—0x22E – Auto Exposure target and Precision Control (R/W)	
Default	0x0C4A

Table 11: Camera Control Register Description (Continued)

Bit Fields	Description
Description	This register specifies the luma target of the auto exposure algorithm and the size of the window/range around the target in which no auto exposure adjustment is made. This window is centered on target, but the value programmed in the register is 1/2 of the window size.
Bits 15:8	Half-size of the auto exposure stability window/range.
Bits 7:0	Luma value of the auto exposure target.
R47:2—0x22F – Auto Exposure Speed and Sensitivity Control—Context A (R/W)	
Default	0xDF20
Description	This register specifies the speed and sensitivity to changes of auto exposure in context A.
Bit 15	Reserved.
Bit 14	
Bits 13:12	
Bit 11	Reserved.
Bit 10	Reserved.
Bit 9	Reserved.
Bits 8:6	Factor of reduction of the difference between current luma and target luma. In one adjustment auto exposure advances from current luma to target as follows: 000: 1/4 way going down, 1/8 going up. 001: 1/4 way in both directions. 010: 1/2 way in both directions. 011: 1/2 way going down, 1/4 going up. 100: All the way in both directions (fast adaptation!). 101: 3/4 way in both directions. 110: 7/8 way in both directions. 111: Reserved. Currently the same as “100”
Bit 5	Reserved.
Bits 4:3	Auto exposure luma is updated every N frames, where N is given by this field.
Bits 2:0	Hysteresis control via time-averaged smoothing of luma data. Luma measurements for auto exposure are time-averaged as follows: 000: Auto exposure luma = current luma. 001: Auto exposure luma = 1/2 current luma + 1/2 buffered value. 010: Auto exposure luma = 1/4 current luma + 3/4 buffered value. 011: Auto exposure luma = 1/8 current luma + 7/8 buffered value. 100: Auto exposure luma = 1/16 current luma + 15/16 buffered value. 101: Auto exposure luma = 1/32 current luma + 31/32 buffered value. 110: Auto exposure luma = 1/64 current luma + 63/64 buffered value. 111: Auto exposure luma = 1/128 current luma + 127/128 buffered value.
R91:2—0x25B - Flicker Control (R/W)	
Default	0x0002
Description	Primary Flicker Control Register.
Bit 15	(Read only) 50Hz/60Hz detected. 0: 50Hz detected. 1: 60Hz detected.
Bit 2	
Bit 1	When in “manual” flicker mode (R91:2[0] = 1), defines which flicker frequency to avoid. 0: Forces 50Hz detection. 1: Forces 60Hz detection.
Bit 0	0: Auto flicker detection. 1: Manual Mode.
R98:2—0x262 – Auto Exposure Digital Gains Monitor (R/W)	

Table 11: Camera Control Register Description (Continued)

Bit Fields	Description
Default	N/A
Description	These digital gains are applied within the IFP; they are independent of the imager gains.
Bits 15:8	Post-lens correction digital gain (writable if auto exposure is disabled).
Bits 7:0	Pre-lens correction digital gain (writable if auto exposure is disabled).
R103:2—0x267 – Auto Exposure Digital Gain Limits (R/W)	
Default	0x4010
Description	This register specifies the upper limits of the digital gains used by the auto exposure algorithm. The values programmed to this register are 16 times the absolute gain values. The value of 16 represents the gain 1.0.
Bits 15:8	Maximum limit on post-lens correction digital gain.
Bits 7:0	Maximum limit on pre-lens correction digital gain.
R156:2—0x29C – Auto Exposure Speed and Sensitivity Control—Context B (R/W)	
Default	0xDF20
Description	This register specifies the speed and sensitivity to auto exposure changes in context B.
Bit 15	Reserved.
Bit 14	
Bits 13:12	
Bit 11	Reserved.
Bit 10	Reserved.
Bit 9	Reserved.
Bits 8:6	Factor of reduction of the difference between current luma and target luma. In one adjustment, auto exposure advances from current luma to target as follows: 000: 1/4 way going down, 1/8 going up. 001: 1/4 way in both directions. 010: 1/2 way in both directions. 011: 1/2 way going down, 1/4 going up. 100: All the way in both directions (fast adaptation!). 101: 3/4 way in both directions. 110: 7/8 way in both directions. 111: Reserved. Currently the same as “100.”
Bit 5	Reserved.
Bits 4:3	Auto exposure luma is updated every N frames, where N is given by this field.
Bits 2:0	Hysteresis control via time-averaged smoothing of luma data. Luma measurements for auto exposure are time-averaged as follows: 000: Auto exposure luma = current luma. 001: Auto exposure luma = 1/2 current luma + 1/2 buffered value. 010: Auto exposure luma = 1/4 current luma + 3/4 buffered value. 011: Auto exposure luma = 1/8 current luma + 7/8 buffered value. 100: Auto exposure luma = 1/16 current luma + 15/16 buffered value. 101: Auto exposure luma = 1/32 current luma + 31/32 buffered value. 110: Auto exposure luma = 1/64 current luma + 63/64 buffered value. 111: Auto exposure luma = 1/128 current luma + 127/128 buffered value.
R200:2—0x2C8 – Global Context Control (R/W)	
Default	0x0000
Description	Defines sensor and colorpipe context for current frame. Context A is typically used to define preview or viewfinder mode, while context B is typically used for snapshots. The bits of this register *directly* control the respective functions, so care must be taken when writing to this register if a bad frame is to be avoided during the context switch.

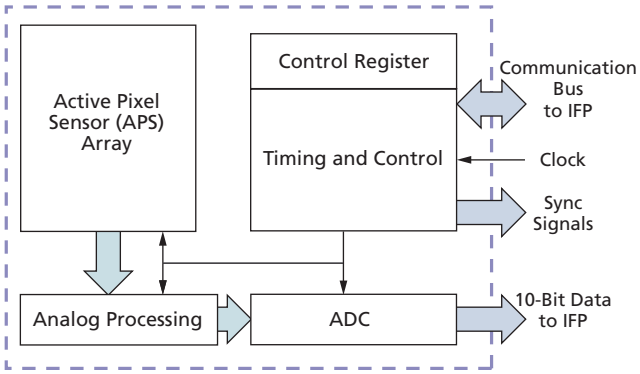
Table 11: Camera Control Register Description (Continued)

Bit Fields	Description
Bit 15	Controls assertion of sensor restart on update of global context control register. This helps ensure that the very next frame is generated with the new context (a problem with regard to exposure due to the rolling shutter). This bit is automatically cleared once the restart has occurred. 0: Do not restart sensor. 1: Restart sensor.
Bit 14	Reserved.
Bit 13	Reserved.
Bit 12	Reserved.
Bit 11	Reserved.
Bit 10	Resize/zoom context. Switch resize/zoom contexts: 0: Context A 1: Context B
Bit 9	Output format control 2 Context. See R0x13A and R0x19B. 0: Context A. 1: Context B.
Bit 8	Gamma table context. 0: Context A. 1: Context B.
Bit 7	Arm Xenon Flash.
Bit 6	Blanking control. This is primarily for use by the internal sequencer when taking automated (e.g., flash) snapshots. Setting this bit stops frames from being sent to ensure that the desired frame during a snapshot sequence is the only frame captured by the host. 0: No blanking. 1: Blank frames to host.
Bit 5	Reserved.
Bit 4	Reserved.
Bit 3	Sensor Read Mode context (skip mode, power mode (second ADC on/off), see R0x021 and R0x020. 0: Context A 1: Context B
Bit 2	LED Flash ON 0: Turn off LED Flash 1: Turn on LED Flash
Bit 1	Vertical blanking context: 0: Context A 1: Context B
Bit 0	Horizontal blanking context: 0: Context A 1: Context B

Sensor Core Overview

The sensor consists of a pixel array of 695 x 504 total, an analog readout chain, 10-bit ADC with programmable gain and black offset, and timing and control.

Figure 5: Sensor Core Block Diagram



Pixel Data Format

Pixel Array Structure

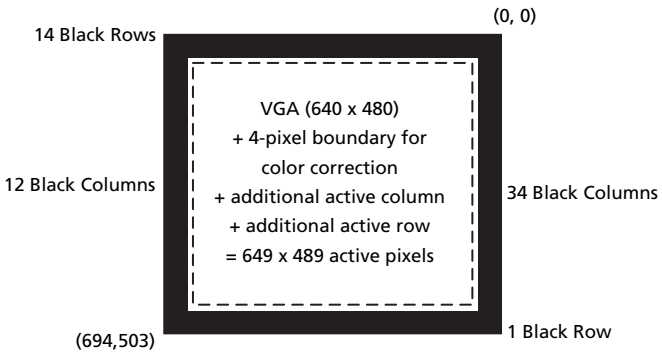
The sensor core pixel array is configured as 695 columns by 504 rows, shown in Figure 6. The first 34 columns and the first 14 rows of pixels are optically black, and can be used to monitor the black level. The last 12 columns and the last row of pixels also are optically black.

The black row data is used internally for the automatic black level adjustment. However, these black rows can also be read out by setting the sensor to raw data output mode.

There are 649 columns by 489 rows of optically-active pixels that provide a four-pixel boundary around the VGA (640 x 480) image to avoid boundary effects during color interpolation and correction.

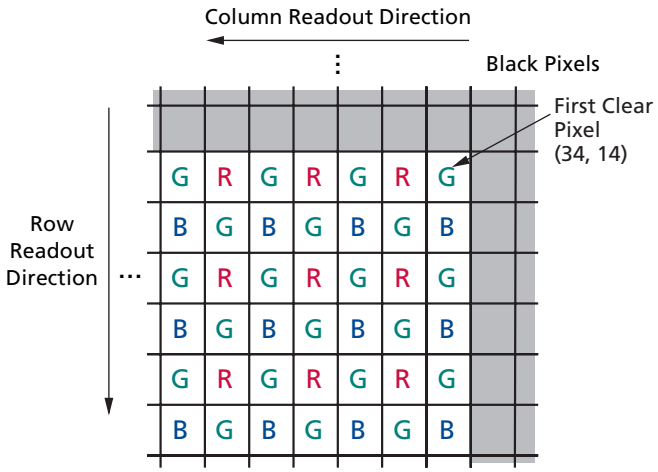
The additional active column and additional active row are used to enable horizontally and vertically mirrored readout to start on the same color pixel.

Figure 6: Pixel Array Description



The sensor core uses an RGB Bayer color pattern, shown in Figure 7. The even-numbered rows contain green and red color pixels, and odd-numbered rows contain blue and green color pixels. The even-numbered columns contain green and blue color pixels; odd-numbered columns contain red and green color pixels.

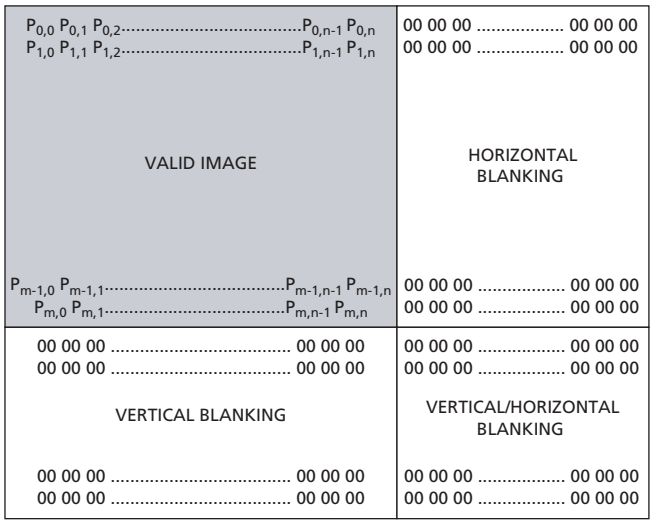
Figure 7: Pixel Color Pattern Detail (top right corner)



Output Data Format

The sensor core image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking, shown in Figure 8. LINE_VALID is HIGH during the shaded region of the figure. FRAME_VALID timing is described in *"Appendix A" on page 55*.

Figure 8: Spatial Illustration of Image Readout



Sensor Core Registers

Table 12: Sensor Registers – Address Page 0

Register# Decimal (HEX)	Register Name	Data Format	Default Value Decimal (HEX)
0 (0x00)	Chip Version	0001 0010 0010 1001 (LSB)	4649 (0x1229)
1 (0x01)	Row Start	0000 0ddd dddd dddd	18 (0x12)
2 (0x02)	Column Start	0000 0ddd dddd dddd	38 (0x0026)
3 (0x03)	Row Width	0000 0ddd dddd dddd	480 (0x01E0)
4 (0x04)	Column Width	0000 0ddd dddd dddd	640 (0x280)
5 (0x05)	Horizontal Blanking—Context B	00dd dddd dddd dddd	203 (0xCB)
6 (0x06)	Vertical Blanking—Context B	0ddd dddd dddd dddd	11 (0x0B)
7 (0x07)	Horizontal Blanking—Context A	00dd dddd dddd dddd	203 (0xCB)
8 (0x08)	Vertical Blanking—Context A	0ddd dddd dddd dddd	11 (0x0B)
9 (0x09)	Shutter Width	dddd dddd dddd dddd	470 (0x1D6)
10 (0x0A)	Row Speed	ddd0 000d dddd dddd	17 (0x0011)
11 (0x0B)	Extra Delay	00dd dddd dddd dddd	0 (0x0000)
12 (0x0C)	Shutter Delay	00dd dddd dddd dddd	0 (0x0000)
13 (0x0D)	Reset	d000 00dd 00dd dddd	8 (0x0008)
32 (0x20)	Read Mode—Context B	dd00 0ddd dddd dddd	1792 (0x0700)
33 (0x21)	Read Mode—Context A	0000 0d00 0000 dd00	1024 (0x0400)
34 (0x22)			299 (0x012B)
35 (0x23)	Flash Control	??dd dddd dddd dddd	1544 (0x0608)
36 (0x24)			16384 (0x4000)
43 (0x2B)	Green1 Gain	0000 0ddd dddd dddd	32 (0x0020)

Table 12: Sensor Registers – Address Page 0 (Continued)

Register# Decimal (HEX)	Register Name	Data Format	Default Value Decimal (HEX)
44 (0x2C)	Blue Gain	0000 0ddd dddd dddd	32 (0x0020)
45 (0x2D)	Red Gain	0000 0ddd dddd dddd	32 (0x0020)
46 (0x2E)	Green2 Gain	0000 0ddd dddd dddd	32 (0x0020)
47 (0x2F)	Global Gain	0000 0ddd dddd dddd	32 (0x0020)
48 (0x30)			1066 (0x042A)
49 (0x31)	Reserved	—	7168 (0x1C00)
50 (0x32)	Reserved	—	42 (0x002A)
51 (0x33)	Reserved	—	833 (0x0341)
52 (0x34)	Reserved	—	49160 (0xC009)
53 (0x35)	Reserved	—	8226 (0x2022)
54 (0x36)	Reserved	—	61680 (0xF0F0)
55 (0x37)	Reserved	—	0 (0x0000)
59 (0x3B)	Reserved	—	33 (0x0021)
60 (0x3C)	Reserved	—	6688 (0x1A20)
61 (0x3D)	Reserved	—	8222 (0x201E)
62 (0x3E)	Reserved	—	8224 (0x2020)
63 (0x3F)	Reserved	—	4128 (0x1020)
64 (0x40)	Reserved	—	8192 (0x2000)
65 (0x41)			215 (0x00D7)
66 (0x42)	Reserved	—	1911 (0x0777)
88 (0x58)	Reserved	—	0 (0x000)
89 (0x59)		0000 0000 dddd dddd	12 (0x000C)
90 (0x5A)	Reserved	—	57354 (0xE00A)
91 (0x5B)			N/A
92 (0x5C)			N/A
93 (0x5D)			N/A
94 (0x5E)			N/A
95 (0x5F)			8989 (0x231D)
96 (0x60)			128 (0x0080)
97 (0x61)			0 (0x0000)
98 (0x62)			0 (0x0000)
99 (0x63)			0 (0x0000)
100 (0x64)			0 (0x0000)
112 (0x70)	Reserved	—	31498 (0x7B0A)
113 (0x71)	Reserved	—	31498 (0x7B0A)
114 (0x72)	Reserved	—	6414 (0x190E)
115 (0x73)	Reserved	—	29967 (0x750F)
116 (0x74)	Reserved	—	22322 (0x5732)
117 (0x75)	Reserved	—	22068 (0x5634)
118 (0x76)	Reserved	—	29493 (0x7335)
119 (0x77)	Reserved	—	12306 (0x3012)
120 (0x78)	Reserved	—	30978 (0x7902)
121 (0x79)	Reserved	—	29958 (0x7506)
122 (0x7A)	Reserved	—	30474 (0x770A)
123 (0x7B)	Reserved	—	30729 (0x7809)

Table 12: Sensor Registers – Address Page 0 (Continued)

Register# Decimal (HEX)	Register Name	Data Format	Default Value Decimal (HEX)
124 (0x7C)	Reserved	—	32006 (0x7D06)
125 (0x7D)	Reserved	—	12560 (0x3110)
126 (0x7E)	Reserved	—	126 (0x007E)
127 (0x7F)	Reserved	—	31745 (0x7C01)
128 (0x80)	Reserved	—	22788 (0x5904)
129 (0x81)	Reserved	—	22788 (0x5904)
130 (0x82)	Reserved	—	22282 (0x570A)
131 (0x83)	Reserved	—	22539 (0x580B)
132 (0x84)	Reserved	—	18188 (0x470C)
133 (0x85)	Reserved	—	18446 (0x480E)
134 (0x86)	Reserved	—	23298 (0x5B02)
135 (0x87)	Reserved	—	92 (0x005C)
200 (0xC8)	Context Control	d000 0000 d000 dddd	11 (0x000B)
240 (0xF0)	Page Map	0000 0000 0000 0ddd	0 (0x0000)
241 (0xF1)	Bytewise Address	Reserved	Reserved
245 (0xF5)	Reserved	—	1023 (0x03FF)
246 (0xF6)	Reserved	—	511 (0x01FF)
247 (0xF7)	Reserved	—	0 (0x0000)
248 (0xF8)	Reserved	—	0 (0x0000)
249 (0xF9)	Reserved	—	0 (0x0000)
250 (0xFA)	Reserved	—	0 (0x0000)
251 (0xFB)	Reserved	—	0 (0x0000)
252 (0xFC)	Reserved	—	0 (0x0000)
253 (0xFD)	Reserved	—	0 (0x0000)
255 (0x00)	Chip Version	0001 0010 0010 1001 (LSB)	4649 (0x1229)

Note: 0 = “Don't Care” bit.
d = R/W bit
? = R/O bit.

Table 13: Sensor Core Register Descriptions

Bit Field	Description	Default (HEX)	Sync'd to Frame start	Bad Frame	Read/ Write
R0:0—0x000 – Chip Version (R/O)					
Bits 15:0	Hardwired read only.	0x1229			R
R1:0—0x001 – Row Start					
Bits 10:0 Row Start	The first row to be read out (not counting dark rows that may be read). To window the image down, set this register to the starting Y value. Setting a value less than 8 is not recommended since the dark rows should be read using Reg0x022.	0x12	Y	YM	W
R2:0—0x002 – Column Start					
Bits 10:0 Col Start	The first column to be read out (not counting dark columns that may be read). To window the image down, set this register to the starting X value. Setting a value below 0x18 is not recommended since readout of dark columns should be controlled by Reg0x022.	0x26	Y	YM	W
R3:0—0x003 – Row Width					
Bits 10:0 Row Width	Number of rows in the image to be read out (not counting dark rows or border rows that may be read).	0x1E0	Y	YM	W
R4:0—0x004 – Column Width					
Bits 10:0 Col Width	Number of columns in image to be read out (not counting dark columns or border columns that may be read).	0x284	Y	YM	W
R5:0—0x005 – Horizontal Blanking—Context B					
Bits 10:0 Horizontal Blanking B	Number of blank columns in a row when context B is chosen (bit 0, Reg0x0C8 = 1). The extra columns are added at the beginning of a row. The minimum supported value is 132.	0xCB	Y	YM	W
R6:0—0x006 – Vertical Blanking—Context B					
Bits 14:0 Vertical Blanking B	Number of blank rows in a frame when context B is chosen (bit 1, Reg0x0C8 = 1). This number must be equal to or larger than the number of dark rows read out in a frame specified by Reg0x022.	0x0B	Y	N	W
R7:0—0x007 – Horizontal Blanking—Context A					
Bits 10:0 Horizontal Blanking A	Number of blank columns in a row when context A is chosen (bit 0, Reg0x0C8 = 0). The extra columns are added at the beginning of a row. The minimum supported value is 132.	0xCB	Y	YM	W
R8:0—0x008 – Vertical Blanking—Context A					
Bits 14:0 Vertical Blanking A	Number of blank rows in a frame when context A is chosen (bit 1, Reg0x0C8 = 1). This number must be equal to or larger than the number of dark rows read out in a frame specified by Reg0x022.	0xB	Y	N	W
R9:0—0x009 – Shutter Width					
Bits 15:0 Shutter Width	Integration time in number of rows. In addition to this register, the shutter delay register (Reg0x0C) and the overhead time influences the integration time for a given row time.	0x1D6	Y	N	W
R10:0—0x00A – Row Speed					
Bit 13	Invert to cb clock.	—	—	—	—
Bit 8 Invert Pixel Clock	Invert pixel clock. When set, LINE_VALID, FRAME_VALID, and DATA_OUT is set to the falling edge of PIXCLK. When clear, they are set to the rising edge if there is no pixel clock delay.	0x0	N	0	W

Table 13: Sensor Core Register Descriptions (Continued)

Bit Field	Description	Default (HEX)	Sync'd to Frame start	Bad Frame	Read/ Write
Bits 7:4 Delay Pixel Clock	Delay PIXCLK in half-master-clock cycles. When set, the pixel clock can be delayed in increments of half-master- clock cycles compared to the synchronization of FRAME_VALID, LINE_VALID, and DATA_OUT.	0x1	N	0	W
Bits 3:0 Pixel Clock Speed	The pixel clock period is doubled, so the ADC clock period remains the same for one programmed register value. The value "0" is not allowed, and "1" is used instead.	0x1	Y	YM	W
R11:0—0x00B – Extra Delay					
Bits 13:0 Extra Delay	Extra blanking inserted between frames specified in pixel clocks. Can be used to get a more exact frame rate. For integration times less than a frame, however, it might affect the integration times for parts of the image.	0x0	Y	0	W
R12:0—0x00C – Shutter Delay					
Bits 10:0 Shutter Delay	The amount of time from the end of the sampling sequence to the beginning of the pixel RESET sequence. This variable is automatically halved in low-power mode, so the time in use remains the same. This register has an upper value defined by the fact that the RESET needs to finish prior to readout of that row to prevent changes in the row time.	0x0	Y	N	W
R13:0—0x00D – RESET					
Bit 15 Synchronize Changes	0: Normal operation, updates changes to registers that affect image brightness at the next frame boundary (integration time, integration delay, gain, horizontal blanking and vertical blanking, window size, row/column skip, or row mirror). 1: Do not update any changes to these settings until this bit is returned to "0." All registers that are frame-synchronized are affected by this bit setting.	0x0	N	0	W
Bit 13 Stop_soc	Setting this bit turns off all SOC clocks.	0x0	N	0	W
Bit 12 Div 2	0: CLKIN equals the master clock frequency. 1: CLKIN is divided by two before going to master clock control. This bit is designed to allow a single clock to drive both sensors in a dual camera application. This function will divide down the clock from the higher speed sensor and apply it to the slower sensor.	0x0	N	0	W
Bit 10 Switch two-wire Interface ID	Setting this bit converts the two-wire interface ID from default to the other (0xBA/0xBB => 0x90/0x91).	0x0	N	N	W
Bit 9 Restart Bad Frames	When set, a forced restart occurs when a bad frame is detected. This can shorten the delay when waiting for a good frame because the delay when masking out a bad frame is the integration time rather than the full frame time.	0x0	N	0	W
Bit 8 Show Bad Frames	0: Only output good frames (default) A bad frame is defined as the first frame following a change to: window size or position, horizontal blanking, pixel clock speed, zoom, row or column skip, or mirroring. 1: Output all frames (including bad frames)	0x0	N	0	W

Table 13: Sensor Core Register Descriptions (Continued)

Bit Field	Description	Default (HEX)	Sync'd to Frame start	Bad Frame	Read/ Write
Bit 7 Inhibit STANDBY	Setting this bit stops STANDBY from affecting entry to or exit from the low-power state.				
Bit 6 Drive Signals	By default, asserting STANDBY causes the ball interface to enter High-Z. Setting this bit stops STANDBY from contributing to output enable control.				
Bit 5 RESET SOC	This RESET signal is fed directly to the SOC part of the chip, and has no functionality in a stand alone sensor.	0x0	N	0	W
Bit 4 Output Disable	When set, the output signals are tri-stated. When clear, the output pins can also be tri-stated when bit6 of R13:0 is 0 and Hard STANDBY is asserted.	0x0	N	0	W
Bit 3 Chip Enable	0: Stop sensor readout. When this is returned to "1," sensor readout restarts and begins resetting the starting row in a new frame. To reduce the digital power, the master clock to the sensor can be disabled or STANDBY can be used. 1: Normal operation.	0x1	N	YM	W
Bit 2 STANDBY	0: Normal operation (default) 1: Disable analog circuitry and internal clocks. Whenever this bit is set to "1" the chip enable bit (bit 3) should be set to "0."	0x0	N	YM	W
Bit 1 Restart	Setting this bit causes the sensor to abandon the current frame and start resetting the first row. The delay before the first valid frame is read out equals the integration time. This bit always reads "0."	0x0	N	YM	W
Bit 0 RESET	Setting this bit puts the sensor in RESET mode; this sets the sensor to its default power-up state. Clearing this bit resumes normal operation.	0x0	N	YM	W
R32:0—0x020 – Read Mode—Context B					
Bit 15 XOR Line Valid	0: LINE_VALID determined by bit 9. Ineffective if Continuous LINE_VALID is set. 1: LINE_VALID = "Continuous" Line Valid XOR Frame Valid,	0x0	N	0	W
Bit 14 Continuous Line Valid	0: Normal LINE_VALID (default, no line valid during vertical blanking). 1: "Continuous" LINE_VALID (continue producing line valid during vertical blanking).	0x0	N	0	W
Bit 10	Reserved.	0x1	Y	0	R
Bit 9 Show Border	This bit indicates whether to show the border enabled by bit 8. When bit 8 is 0, this bit has no meaning. When bit 8 is 1, this bit decides whether the border pixels should be treated as extra active pixels (1) or extra blanking pixels (0).	0x1	N	0	W
Bit 8 Over Sized	When this bit is set, a 4-pixel border is output around the active image array independent of readout mode (skip, zoom, mirror, etc.). Setting this bit therefore adds eight to the numbers of rows and columns in the frame.	0x1	Y	YM	W
Bits 7:6		0x0	Y	YM	W
Bit 5 Column Skip 4x	0: Normal readout. 1: READ out two columns, and then skip six columns (as with rows).	0x0	Y	YM	W

Table 13: Sensor Core Register Descriptions (Continued)

Bit Field	Description	Default (HEX)	Sync'd to Frame start	Bad Frame	Read/ Write
Bit 4 Row Skip 4x	0: Normal readout. 1: READ out two rows, and then skip six rows (i.e., row 8, row 9, row 16, row 17…).	0x0	Y	YM	W
Bit 3 Column Skip 2x — Context B	When READ mode context B is selected (bit 3, Reg0x0C8 = 1): 0: Normal readout. 1: READ out two columns, and then skip two columns (as with rows).	0x0	Y	YM	W
Bit 2 Row Skip 2x— Context B	When READ mode context B is selected (bit 3, Reg0x0C8 = 1): 0: Normal readout. 1: READ out two rows, then skip two rows (i.e., row 8, row 9, row 12, row 13…).	0x0	Y	YM	W
Bit 1 Mirror Columns	Read out columns from right to left (mirrored). When set, column readout starts from column (Col Start + Col Size) and continues down to (Col Start + 1). When clear, readout starts at Col Start and continues to (Col Start + Col Size - 1). This ensures that the starting color is maintained.	0x0	Y	YM	W
Bit 0 Mirror Rows	Read out rows from bottom to top (upside down). When set, row readout starts from row (Row Start + Row Size) and continues down to (Row Start + 1). When clear, readout starts at Row Start and continues to (Row Start + Row Size - 1). This ensures that the starting color is maintained.	0x0	Y	YM	W
R33:0—0x021 – Read Mode—Context A					
Bit 10	Reserved.	0x1	Y	0	R
Bit 3 Column Skip 2x — Context A	When READ mode context A is selected (bit 3, Reg0x0C8 = 0): 0: Normal readout. 1: READ out two columns, and then skip two columns (as with rows).	0x0	Y	YM	W
Bit 2 Row Skip 2x— Context A	When READ mode context A is selected (bit 3, Reg0x0C8 = 0): 0: Normal readout. 1: READ out two rows, and then skip two rows (i.e., row 8, row 9, row 12, row 13…).	0x0	Y	YM	W
R35:0—0x023 – Flash Control					
Bit 15 Flash STROBE	Read-only bit that indicates whether FLASH_STROBE is enabled.	0x0	0	0	R
Bit 14	Reserved.	—	—	—	—
Bit 13 Xenon Flash	Enable Xenon flash. When set, the FLASH_STROBE output signal is pulsed HIGH for the programmed period during vertical blanking. This is achieved by keeping the integration time equal to one frame and the pulse width less than the vertical blanking time.	0x0	Y	N	W
Bits 12:11 Frame Delay	Delay of the flash pulse measured in frames.	0x0	N	N	W
Bit 10 End of RESET	0: In Xenon mode, the flash should be enabled after the readout of a frame. 1: In Xenon mode, the flash should be triggered after the resetting of a frame.	0x1	N	N	W

Table 13: Sensor Core Register Descriptions (Continued)

Bit Field	Description	Default (HEX)	Sync'd to Frame start	Bad Frame	Read/ Write
Bit 9 Every Frame	0: Flash should be enabled for one frame only. 1: Flash should be enabled every frame.	0x1	N	N	W
Bit 8 LED Flash	Enables LED flash. When set, the FLASH_STROBE goes on prior to the start of a frame RESET. When disabled, the FLASH_STROBE remains HIGH until readout of the current frame completes.	0x0	Y	Y	W
Bits 7:0 Xenon Count	Length of FLASH_STROBE pulse when Xenon flash is enabled. The value specifies the length in 1,024 master clock cycle increments.	0x08	N	N	W
R43:0—0x02B – Green1 Gain					
Bits 11:9 Digital Gain	Total gain = (Bit 9 + 1) x (Bit 10 + 1) x (Bit 11 + 1) x analog gain (each bit gives 2x gain).	0x0	Y	N	W
Bits 8:7 Analog Gain	Analog gain = (Bit 8 + 1) x (Bit 7 + 1) x initial gain (each bit gives 2x gain).	0x0	Y	N	W
Bits 6:0 Initial Gain	Initial gain = bits (6:0) x 0.03125.	0x20	Y	N	W
R44:0—0x02C – Blue Gain					
Bits 11:9 Digital Gain	Total gain = (Bit 9 + 1) x (Bit 10 + 1) x (Bit 11 + 1) x analog gain (each bit gives 2x gain).	0x0	Y	N	W
Bits 8:7 Analog Gain	Analog gain = (Bit 8 + 1) x (Bit 7 + 1) x initial gain (each bit gives 2x gain).	0x0	Y	N	W
Bits 6:0 Initial Gain	Initial gain = bits (6:0) x 0.03125.	0x20	Y	N	W
R45:0—0x02D – Red Gain					
Bits 11:9 Digital Gain	Total gain = (Bit 9 + 1) x (Bit 10 + 1) x (Bit 11 + 1) x analog gain (each bit gives 2x gain).	0x0	Y	N	W
Bits 8:7 Analog Gain	Analog gain = (Bit 8 + 1) x (Bit 7 + 1) x initial gain (each bit gives 2x gain).	0x0	Y	N	W
Bits 6:0 Initial Gain	Initial gain = bits (6:0) x 0.03125.	0x20	Y	N	W
R46:0—0x02E – Green2 Gain					
Bits 11:9 Digital Gain	Total gain = (Bit 9 + 1) x (Bit 10 + 1) x (Bit 11 + 1) x analog gain (each bit gives 2x gain).	0x0	Y	N	W
Bits 8:7 Analog Gain	Analog gain = (Bit 8 + 1) x (Bit 7 + 1) x initial gain (each bit gives 2x gain).	0x0	Y	N	W
Bits 6:0 Initial Gain	Initial gain = bits (6:0) x 0.03125.	0x20	Y	N	W
R47:0—0x02F – Global Gain					
Bits 11:0 Global Gain	This register can be used to set all four gains at once. When read, it returns the value stored in Reg0x2B.	0x20	Y	N	W
R200:0—0x0C8 – Context Control					
Bit 15 Restart	Setting this bit causes the sensor to abandon the current frame and start resetting the first row. Same physical register as Reg0x00D, bit 1.	0x0	N	YM	W

Table 13: Sensor Core Register Descriptions (Continued)

Bit Field	Description	Default (HEX)	Sync'd to Frame start	Bad Frame	Read/ Write
Bit 7 Xenon Flash Enable	Enable Xenon flash. Same physical register as Reg0x023, bit 13.	0x0	Y	N	W
Bit 3 Read Mode Select	0: Use read mode, context A, Reg0x021. 1: Use read mode, context B, Reg0x020. Bits found only in the read mode context B register are not context switched.	0x1	Y	YM	W
Bit 2 LED Flash Enable	Enable LED flash. Same physical register as Reg0x023, bit 8.	0x0	Y	Y	W
Bit 1 Vertical Blanking Select	0: Use vertical blanking, context A, Reg0x008. 1: Use vertical blanking, context B, Reg0x006.	0x1	Y	YM	W
Bit 0 Horizontal Blanking Select	0: Use horizontal blanking, context A, Reg0x007. 1: Use horizontal blanking, context B, Reg0x005.	0x1	Y	YM	W
R240:0—0x0F0 – Page Map					
Bits 2:0 Page Map	Page mapping register. Must be kept at 0 to be able to write to/ read from sensor. Used in the SOC to access other pages with registers.	0x0	N	0	W
R241:0—0x0F1 – Byte-Wise Address					
Bit 0 Byte-Wise Address	Special address to perform 8-bit (instead of 16-bit) reads and writes to the sensor. For additional information, see "Two-Wire Serial Interface Sample" on page 56 and "Appendix A" on page 55.	N/A	0	0	0
R255:0—0x000 – Chip Version (R/O)					
Bits 15:0	Hardwired read only.	0x1229			R

Note: notation used in the above table:

Sync'd to frame start

0 = not applicable, e.g., read-only register.

N = the register value is updated and used immediately.

Y = the register value is updated at next frame start as long as the synchronize-changes bit is 0. Frame start is defined as when the first dark row is read out. By default, this is eight rows before FRAME_VALID goes HIGH.

Bad frame

A bad frame is a frame where all rows do not have the same integration time, or offsets to the pixel values changed during the frame.

0 = not applicable, e.g., read-only register.

N = Changing the register value does not produce a bad frame.

Y = Changing the register value might produce a bad frame.

YM = Yes, but the bad frame is masked out unless the show-bad-frames feature is enabled.

Read / Write

R = read-only register/bit.

W = read / Write register/bit.

Modes and Timing

This section provides an overview of typical usage modes for the MT9V112.

Contexts

The MT9V112 supports hardware-accelerated context switching. A number of parameters have two copies of their setup registers; this allows two “contexts” to be loaded at any given time. These are referred to as context A and context B. Context selection for any single parameter is determined by the global context control register (GCCR, see R200:2).

There are copies of this register in each address page. A write to any one of them has the identical effect. However, a read from address page 0 only returns the subset bits of R200 that are specific to the sensor core.

Contexts are generically named because they can be utilized for a variety of purposes. One typical usage model is to define context A as viewfinder or preview mode and context B as snapshot mode. The device defaults are configured with this in mind. this mechanism enables the user to have settings for viewfinder and snapshot modes loaded at the same time, and then switch between them with a single write to a register (e.g., R200:2).

Viewfinder/Preview and Full-Resolution/Snapshot Modes

No context switching is necessary in the sensor core because this is a single ADC device. Context switching occurs in the colorpipe stage.

Preview Mode

QVGA (320 x 240) images are generated at up to 30 fps. The reduced-size images are generated by a scaling down operation. The sensor always outputs a VGA size image to the colorpipe in both context A and context B.

Snapshot Mode

VGA (640 x 480) images are generated at up to 30 fps. this is typically selected by setting R200:n[10] = 1 selecting resize/zoom context B.

Switching Modes

Typically, switching to snapshot mode is achieved by writing R200:2 = 0x9F0B. this restarts the sensor and sets most contexts to context B. Following this write, a read from R200:1 or R200:2 results in 0x1F0B being read.

The MSB is cleared automatically by the sensor. A read from R200:0 results in 0x000B, as only the lower 4 bits and the restart MSB are implemented in the sensor core.

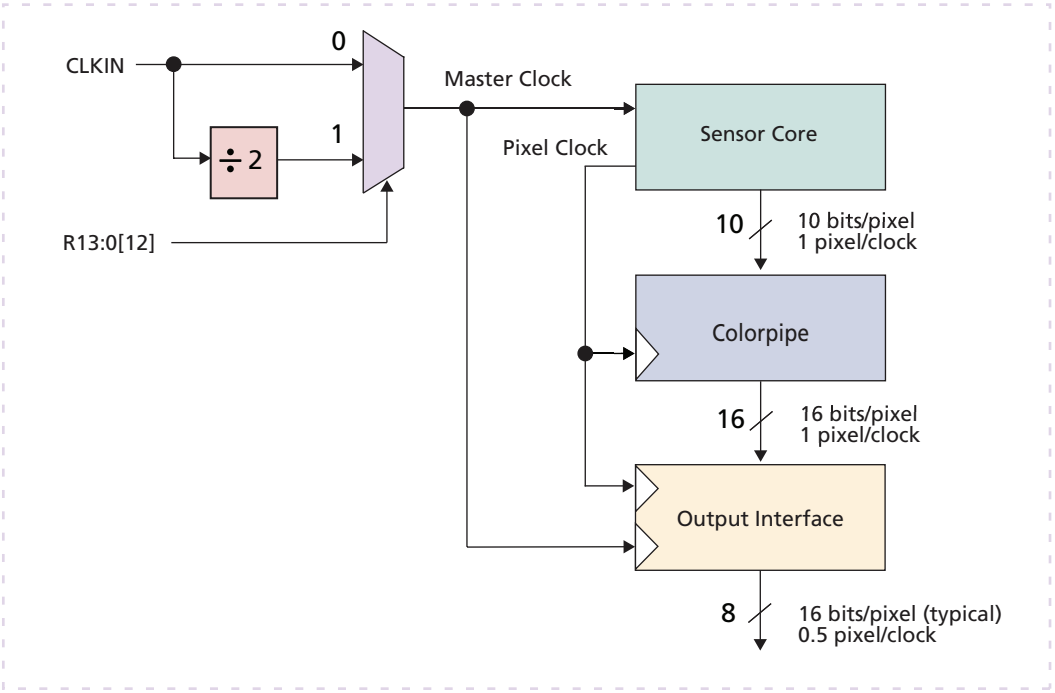
Clocks

The sensor core is a master in the system. The sensor core frame rate defines the overall image flow pipeline frame rate. Horizontal blanking and vertical blanking are influenced by the sensor configuration, and are also a function of certain image flow pipeline functions—particularly resize. The relationship of the primary clocks are depicted in Figure 9 on page 43.

The image flow pipeline typically generates up to 16-bits per pixel—for example, YCbCr or RGB565—but has only an 8-bit port through which to communicate this pixel data. There is no phase-locked loop (PLL), so the primary input clock (CLKIN) must be twice the fundamental pixel rate (defined by the sensor pixel clock).

To generate VGA images at 30 fps, the sensor core requires a clock in the 24 MHz–27 MHz range. The device defaults assume a 24 MHz clock, and minimum clock frequency is 2 MHz.

Figure 9: Primary Sensor Core Clock Relationships



Note: If R13:0[12] = 0 then the Master Clock will be equal to the frequency of CLKIN.
If R13:0[12] = 1 then the Master Clock will be 1/2 of the frequency of CLKIN.
Frequency of Master Clock = 2*Frequency of Pixel Clock

Tuning Frame Rates

Actual frame rates can be tuned by adjusting various sensor parameters. The sensor registers are in address page 0, some of which are shown in Table 14.

Table 14: Register Address Functions

Register	Function
R0x04:0	Column width, typically 640 in the MT9V112
R0x03:0	Row width, typically 480 in the MT9V112
R0x07:0, R0x05:0	Horizontal blanking, default is 203 (units of sensor pixel clocks)
R0x08:0, R0x06:0	Vertical blanking, default is 11 (rows including black rows)

Default Blanking Calculations

the MT9V112 default blanking calculations are shown in Table 15.

Table 15: Blanking Parameter Calculations

Parameter	Calculation
PC_PERIOD Sensor Pixel Clock Period	(2/24)µs = 0.083µs
A: Active Data time (per line): R0 x 04:0 + 8 (border) * PC_PERIOD	648 x (2/24) = 54µs
Q: Horizontal Blanking: [R0 x 05:0 | R0 x 07:0] * PC_PERIOD	154 x (2/24) = 12.83µs
Row time = Q + A	66.83µs
P: Frame Start / End Blanking: 6 * PC_PERIOD	6 x (2/24) = 0.5µs
V: Vertical Blanking: [R0 x 06:0 | R0 x 08:0] * (Q + A) + (Q - 2 * P)	(11 x 66.83) + (12.83 - 1.0) = 747µs
F: Total Frame time: (R0 x 03:0 + [R0 x 06:0 | R00 x 08:0]) * (Q + A)	(488 + 11) x 66.83µs = 33349.83 µs ≥ 30 fps

In the MT9V112, the sensor core adds four border pixels all the way around the image, taking the active image size to 648 x 488 in full power mode. this is achieved through the default settings:

- Oversize and show border bits are set by default
- Oversize and show border bits are not context switchable, and therefore, their location is only in read mode context B.

User Blanking Calculations

When calculating blanking for different clock rates, minimum values for horizontal blanking and vertical blanking must be taken into account. Table 16 shows minimum values for each register.

.

Table 16: User Blanking Minimum Values

Parameter	Minimum
Horizontal Blanking	132 (sensor pixel clocks)
Vertical Blanking	6 + Reg0x22:0[2:0] rows

Output Timing

Figure 10: Vertical Timing

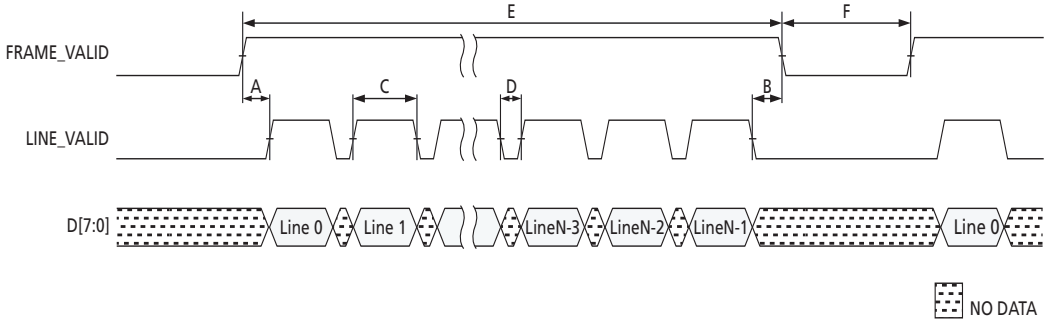
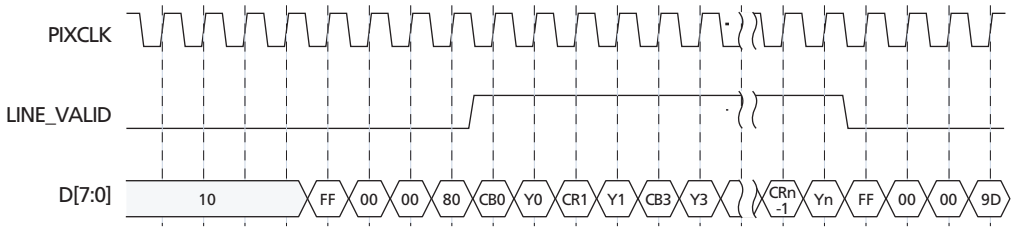


Figure 11: Horizontal Timing



Typical Resolutions, Modes, and Timing

The parameters listed in Table 17 are illustrated in a waveform diagram, *Figure 10, Vertical Timing, on page 45*. *Figure 26, AC Electrical Characteristics, on page 53* provides values for these parameters in some common resolutions and operating modes.

Table 17: Blanking Definitions

Designation	Definition
(A)	FRAME_VALID (rising edge) to LINE_VALID (rising edge) delay
(B)	LINE_VALID (falling edge) to FRAME_VALID (falling edge) delay
(C)	LINE_VALID (HIGH/valid) time
(D)	LINE_VALID (LOW/horizontal blanking) time
(E)	FRAME_VALID (HIGH/valid) time
(F)	FRAME_VALID (LOW/vertical blanking) time

RESET, Clocks, and STANDBY

RESET

Power-up reset is asserted/de-asserted on RESET#. It is active LOW. In this reset state, all control registers have the default values.

Soft reset is asserted/de-asserted by the two-wire serial interface program. In soft-reset mode, the two-wire serial interface and register ring bus are still running. All control registers are reset using default values. See R13:0.

Clocks

The MT9V112 has two primary clocks; a master clock coming from the CLKIN signal, and a pixel clock via a clock-gated operation running at half frequency of the master clock. All device clocks are turned off in power-down mode. When the MT9V112 operates in sensor stand-alone mode, the image flow pipeline clocks can be shut off to conserve power. See R13:0.

When the MT9V112 is operated with the MT9M111 in a dual-camera application, the MT9V112 employs a divide-by-two clock option, allowing a 54 MHz input to the master clock. For more information about this feature, see the R13:0 register description on page 36 in Table 13.

STANDBY

STANDBY is a multifunctional signal that controls power-down, device addressing, and tri-state functions. Table 18 shows how STANDBY affects the output signal state.

Hard standby is asserted/de-asserted on STANDBY. It is active HIGH. In this hard standby state, all internal clocks are turned off and the analog block is in STANDBY mode to save power consumption. The signal state is High-Z when R13[4] = 0 and R13[6] = 0.

Two-wire interface ID addressing is based on the result of SADDR XOR R13:0[10]. (The R13:0[10] default is “0”.) the R13:0[10] bit is not writable when STANDBY is asserted “1.”

Soft standby is asserted/de-asserted by a two-wire serial interface to R13:0[2]. In soft standby, all internal clocks are turned off, the analog block is in standby mode, but the signal state is not affected. Following the assertion of either hard or soft STANDBY, the analog circuitry completes reading the current row and then enters the standby state. It is necessary to keep clocking the sensor for an entire row time to ensure proper entry into the standby state.

In either case CLKIN must be running for standby to work properly

Table 18: STANDBY Effect on the Output State

Output Disable R13:0[4]	Drive Signal R13:0[6]	STANDBY	Output State
0	0	0	Driven
0	0	1	High-Z
0	1	x	Driven
1	x	x	High-Z

Electrical Specifications

Operating Conditions

Table 19: Operating Conditions

Symbol	Definition	MIN	Typical	MAX	Units
V_{DDQ}	I/O Digital Voltage	1.7	V_{DD}	3.1	V
V_{DD}	Core Digital Voltage (condition 1)	2.5	2.8	3.1	V
	Core Digital Voltage (condition 2)	1.7	1.8	1.9	V
V_{AA}	Analog Voltage	2.5	2.8	3.1	V
V_{AAPIX}	Pixel Supply Voltage	2.5	2.8	3.1	V
T_C	Operating temperature (At Junction)	–30	30	70	°C

Note: Recommended die operating temperature range is from Ta = –20°C to 40°C. The sensor image quality may degrade above 40°C.

Table 20: Absolute Maximum Ratings

Symbol	Parameter	Condition	Rating		Unit
			MIN	MAX	
V_{DD}	Digital power (2.8V)		-0.3	4.0	V
V_{DDQ}	I/O power		-0.3	4.0	V
V_{AA}	Analog power (2.8V)		-0.3	4.0	V
VAAPIX	Pixel array power		-0.3	4.0	V
V_{IN}	DC Input Voltage		-0.3	V_{DDQ}+0.3	V
V_{OUT}	DC Output Voltage		-0.3	V_{DDQ}+0.3	V
T_{STG}[1]	Storage temperature		-40	85	°C
I_{LZ}	High Impedance Output Leakage Current	V_{IN} = V_{DDQ} or DGND	-10	10	µA

Notes: 1. Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the product specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Table 21: DC Electrical Characteristics (Condition 1)

V_{DD} = 2.8V, V_{AA} = 2.8V, V_{AAPIX} = 2.8V, V_{DDQ} = 2.8V, f_{CLKIN} = 27 MHz (50% duty cycle), Ta = 30°C, Light Condition = Dark

Symbol	Definition	MIN	Typical	MAX	Units
V_{IH}	Voltage Input High	2.5	2.8	3.1	V
V_{IL}	Voltage Input Low	–0.3	0	0.3	V
I_{IL}	Current Input leakage Low	–5		5	µA
I_{IH}	Current Input leakage High	–5		5	µA
V_{OH}	Voltage Output High	V_{DDQ}-0.3		V_{DDQ}	V
V_{OL}	Voltage Output Low	0	0	0.3	V
I_{OH}	Current Output High	12		15	mA
I_{OL}	Current Output Low	14		17	mA

Table 22: DC Electrical Characteristics (Condition 2)

V_{DD} = 1.8V, V_{AA} = 2.8V, V_{AAPIX} = 2.8V, V_{DDQ} = 1.8V, f_{CLKIN} = 27 MHz (50% duty cycle), Ta = 30°C, Light Condition = Dark

Symbol	Definition	MIN	Typical	MAX	Units
V_{IH}	Voltage Input High	1.7	1.8	1.9	V
V_{IL}	Voltage Input Low	–0.3	0	0.3	V
I_{IL}	Current Input leakage Low	–5		5	µA
I_{IH}	Current Input leakage High	–5		5	µA
V_{OH}	Voltage Output High	V_{DDQ}-0.3		V_{DDQ}	V
V_{OL}	Voltage Output Low	0	0	0.3	V
I_{OH}	Current Output High	8		10	mA
I_{OL}	Current Output Low	10		12	mA

I/O Parameters

Table 23: I/O Parameters

V_{AA} = 2.8V, V_{AAPIX} = 2.8V, fCLKIN = 27 MHz (50% duty cycle), Ta = 30°C, Light Condition = Dark

Signal	Parameter	Definitions	Condition	Min	Typical	Max	Units
All Outputs		Load capacitance				30	pF
		Output signal slew	VDD = VDDQ = 2.8V, 30pF load	0.25		1.25	V/ns
			VDD = VDDQ = 1.8V, 30pF load	0.1		0.6	V/ns
All Inputs	Signal CAP	Input signal capacitance				5	pF
CLKIN	freq	Master clock frequency	Absolute minimum	2			MHz
			VGA at 30 fps	24		27	MHz

Note: I/O pins exhibit the characteristics of either the input signals or the output signals as stated, depending on the state of the I/O pins.

Power Consumption

Table 24: Operating Power Consumption

V_{AA} = 2.8V, VAAPIX = 2.8V, f_{CLKIN} = 27 MHz (50% duty cycle), Ta = 30 °C, Light Condition = 90 lux

Mode	fps	Definition	(V_{DD},V_{DDQ} = 2.8V)		(V_{DD},V_{DDQ} = 1.8V)		Units
			TYP	MAX	TYP	MAX	
VGA	30 fps	Operating I_{DD}	15	25	9	16	mA
		Operating I_{AA}	19	22	19	22	mA
		Operating I_{DDQ}	11	30	5	17	mA
		Operating I_{AAPIX}	1	1	1	1	mA
VGA	30 fps	Total power consumption w/o I_{DDQ}	98	136	72	94	mW
VGA	15 fps	Operating I_{DD}	15	20	9	12	mA
		Operating I_{AA}	19	22	19	22	mA
		Operating I_{DDQ}	10	19	5	11	mA
		Operating I_{AAPIX}	1	1	1	1	mA
VGA	15 fps	Total power consumption w/o I_{DDQ}	98	122	72	88	mW
QVGA	30 fps	Operating I_{DD}	15	25	9	15	mA
		Operating I_{AA}	19	22	19	22	mA
		Operating I_{DDQ}	9	14	4	8	mA
		Operating I_{AAPIX}	1	2	1	2	mA
QVGA	30 fps	Total power consumption w/o I_{DDQ}	98	136	72	94	mW
QVGA	15 fps	Operating I_{DD}	15	20	9	12	mA
		Operating I_{AA}	19	22	19	22	mA
		Operating I_{DDQ}	8	11	4	7	mA
		Operating I_{AAPIX}	1	1	1	1	mA
QVGA	15 fps	Total power consumption w/o I_{DDQ}	98	121	72	88	mW

STANDBY Power Consumption

Table 25: STANDBY Power Consumption

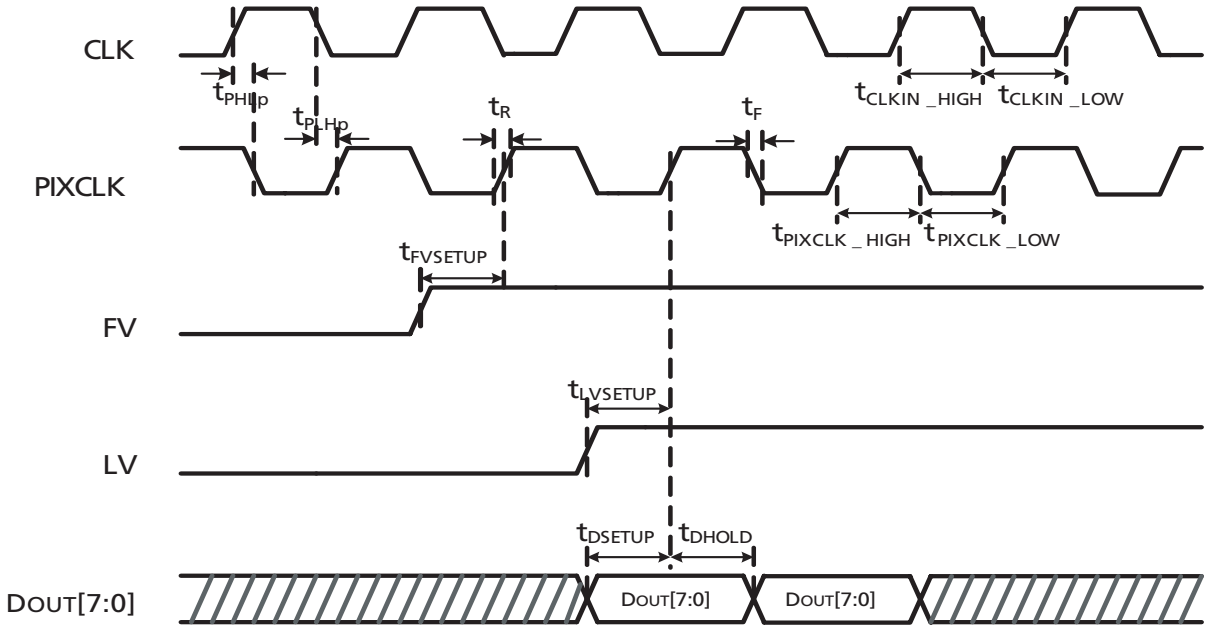
V_{AA} = 2.8V, V_{AAPIX} = 2.8V, f_{CLKIN} = 27 MHz (50% duty cycle), Ta = 30 °C

Definition	MAX (V_{DD},V_{DDQ} = 2.8V)	MAX (V_{DD},V_{DDQ} = 1.8V)	Units
Hard STANDBY I_{DD} (without clock)	1	1	µA
Hard STANDBY I_{DDQ} (without clock)	4	2	µA
Hard STANDBY I_{AA} (without clock)	1	1	µA
Hard STANDBY I_{AAPIX} (without clock)	1	1	µA
Total Power Consumption (without clock)	20	11	µW
Hard STANDBY I_{DD} (with clock)	821	487	µA
Hard STANDBY I_{DDQ} (with clock)	22	8	µA
Hard STANDBY I_{AA} (with clock)	1	1	µA
Hard STANDBY I_{AAPIX} (with clock)	1	1	µA
Total Power Consumption (with clock)	2366	897	µW

I/O Timing

By default, the MT9V112 launches pixel data, FRAME_VALID, and LINE_VALID synchronously with the falling edge of PIXCLK. The expectation is that the user captures data, FRAME_VALID, and LINE_VALID using the rising edge of PIXCLK. The timing diagram is shown in Figure 12. As an option, the polarity of the PIXCLK can be inverted from the default. this is achieved by programming R58:1[9] or R155:1[9] to "0."

Figure 12: AC Output Timing Diagram



AC Electrical Characteristics

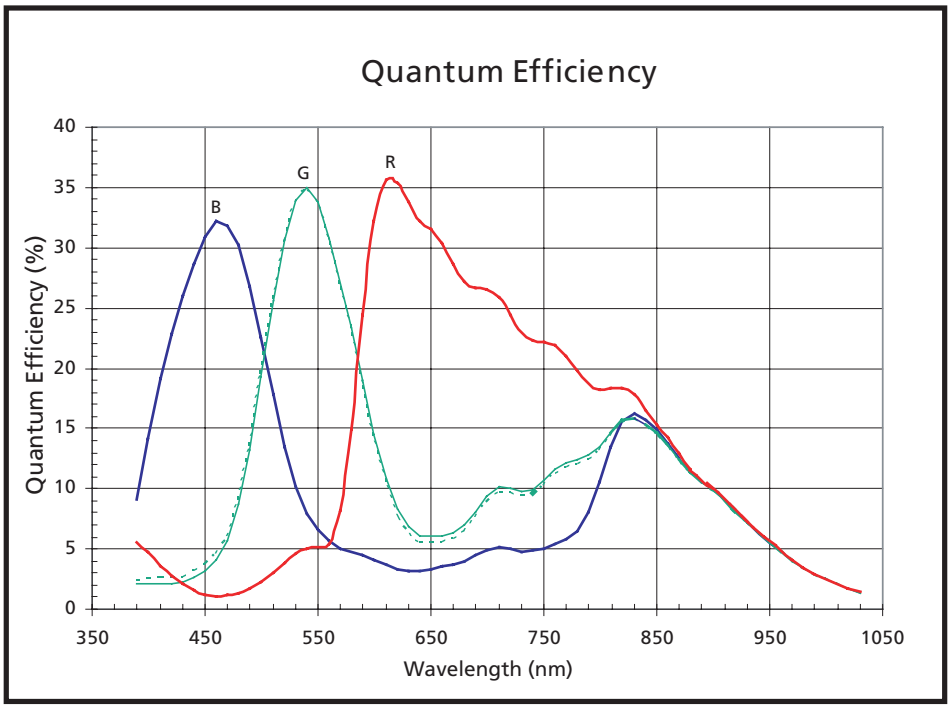
Table 26: AC Electrical Characteristics

V_{DD} = 2.8V, V_{AA} = 2.8V, V_{AAPIX} = 2.8V, V_{DDQ} = 2.8V, f_{CLKIN} = 27 MHz (50% duty cycle), Ta = 30°C, Light Condition = Dark

Symbol	Definition	MIN	Typical	MAX	Units
f_{CLKIN}	Input clock frequency		13.5	27	MHz
t_R	Pixel clock rise time		10		ns
t_F	Pixel clock fall time		10		ns
t_{PLHP}	CLKIN to PIXCLK propagation delay (L–H)		48		ns
t_{PHLP}	CLKIN to PIXCLK propagation delay (H–L)		48		ns
$t_{LVSETUP}$	Setup time for LINE_VALID before rising edge of PIXCLK		1/2 PIXCLK Period		ns
$t_{FVSETUP}$	Setup time for FRAME_VALID before rising edge of PIXCLK		1/2 PIXCLK Period		ns
t_{DSETUP}	Setup time for DOUT before rising edge of PIXCLK		1/2 PIXCLK Period		ns
t_{DHOLD}	Hold time for DOUT after rising edge of PIXCLK		1/2 PIXCLK Period		ns
t_{CLKIN_HIGH}	Master clock duty cycle (High time)	40	50	60	%
t_{CLKIN_LOW}	Master clock duty cycle (Low time)	40	50	60	%
t_{PIXCLK_HIGH}	Pixel clock duty cycle (High time)	40	50	60	%
t_{PIXCLK_LOW}	Pixel clock duty cycle (Low time)	40	50	60	%

Spectral Characteristics

Figure 13: Typical Spectral Characteristics



Appendix A

Serial Bus Description

Registers are written to and read from the MT9V112 through the two-wire serial interface bus. The sensor is a serial interface slave controlled by the serial clock (SCLK), which is driven by the serial interface master. Data is transferred in and out of the MT9V112 through the serial data (SDATA) line. The SDATA line is pulled up to VDDQ off-chip by a 1.5KΩ resistor. Either the slave or the master device can pull the SDATA line down—the serial interface protocol determines which device is allowed to pull the SDATA line down at any given time.

Protocol

The two-wire serial interface defines several different transmission codes, as follows:

- Start bit
- (No) Acknowledge bit
- 8-bit message
- Stop bit
- Slave device 8-bit address

SADDR and R13:0[10] are used to select between two different addresses in case of conflict with another device. If SADDR XOR R13:0[10] is LOW, the slave address is 0x90; if SADDR XOR R13:0[10] is HIGH, the slave address is 0xBA. See Table 27.

Table 27: Two-Wire Interface ID Switching

SADDR	R13:0[10]	Two-Wire Interface ID
0	0	0x90
0	1	0xBA
1	0	0xBA
1	1	0x90

Sequence

A typical read or write sequence begins with the master sending a start bit. After the start bit, the master sends the 8-bit slave device address. The last bit of the address determines if the request is a read or a write, where a “0” indicates a write and a “1” indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master transfers the 8-bit register address for where a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data, eight bits at a time, with the slave sending an acknowledge bit after each eight bits.

The MT9V112 uses 16-bit data for its internal registers, thus requiring two 8-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. The master sends the write mode slave address and 8-bit register address, just as in the write request. The master then sends a start bit and the read mode slave address. The master clocks out the register data, eight

bits at a time, and sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of 7 bits of address and 1 bit of direction. A "0" in the LSB of the address indicates write mode, and a "1" indicates read mode. The write address of the sensor is 0xBA; the read address is 0xBB. This applies only when the SADDR is set HIGH.

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock—it can only change when the serial clock is LOW. Data is transferred eight bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver signals an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No-Acknowledge Bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Two-Wire Serial Interface Sample

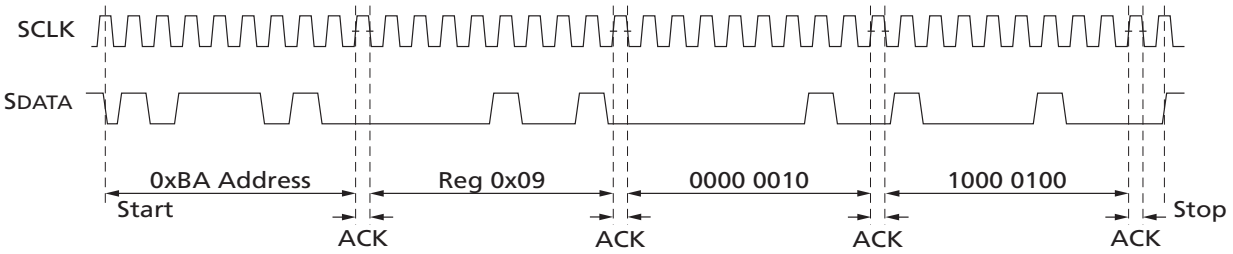
Write and read sequences (SADDR = 1).

16-Bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in *Figure 14*. A start bit sent by the master starts the sequence, followed by the write address. The image sensor sends an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each 8-bit transfer, the image sensor sends an acknowledge bit.

All 16 bits must be written before the register is updated. After 16 bits are transferred, the register address is automatically incremented so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

Figure 14: Write Timing to R0x09:0—Value 0x0284

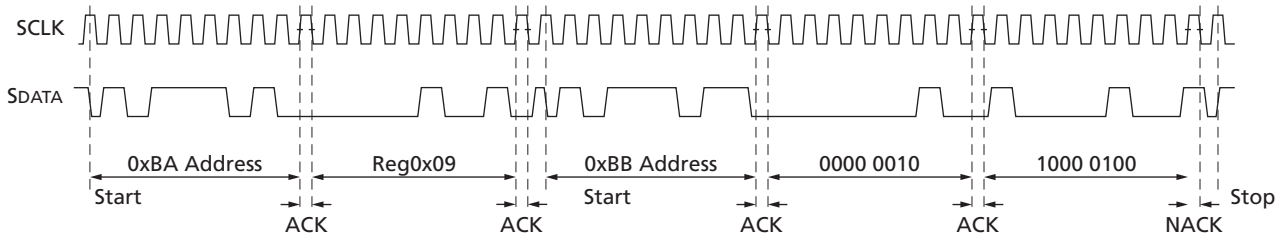


16-Bit Read Sequence

A typical read sequence is shown in *Figure 15*. The master writes the register address, as in a write sequence. Then a start bit and the read address specify that a read is about to occur from the register. The master then clocks out the register data, 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer.

The register address should be incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

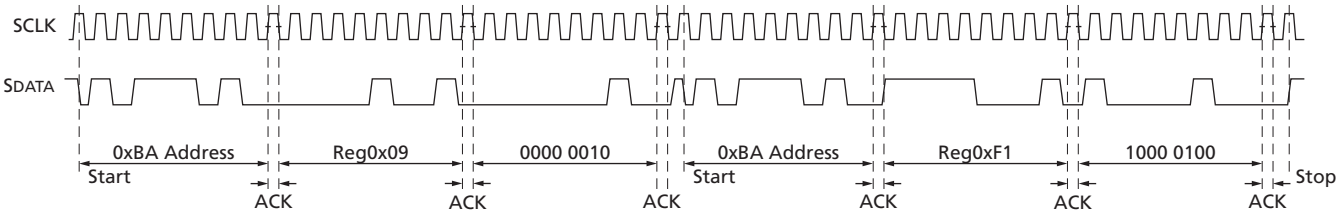
Figure 15: Read Timing from R0x09:0; Returned Value 0x0284



8-Bit Write Sequence

To be able to write one byte at a time to the register, a special register address is added. The 8-bit write is started by writing the upper eight bits to the desired register, then writing the lower eight bits to the special register address (R0xF1:0). The register is not updated until all 16 bits have been written. It is not possible to update just half of a register. In *Figure 16*, a typical sequence for an 8-bit write is shown. The second byte is written to the special register (R0xF1:0).

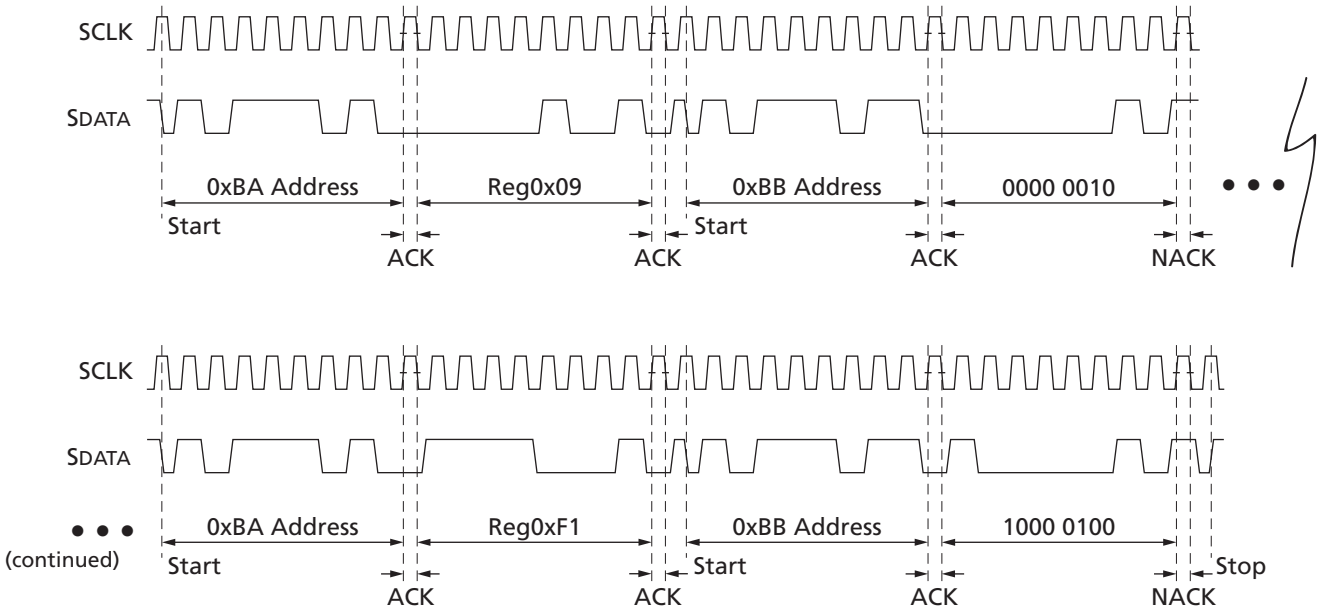
Figure 16: Write Timing to R0x09:0—Value 0x0284



8-Bit Read Sequence

To read one byte at a time, the same special register address is used for the lower byte. The upper eight bits are read from the desired register. By following this with a read from the special register (R0xF1:0), the lower eight bits are accessed (*Figure 17*). The master sets the no-acknowledge bits.

Figure 17: Read Timing from R0x09:0; Returned Value 0x0284



Two-wire Serial Bus Timing

The two-wire serial interface operation requires a certain minimum of master clock cycles between transitions. These are specified in the table below in master clock cycles.

Table 28: Two-wire Serial Bus Timing

Symbol	Definition	MIN	TYP	MAX	Units
tic	Two-Wire Serial Bus Clock time period		60/MCLK	20/MCLK	ns
ticl	Two-Wire Serial Bus Clock Low period *1	8T			ns
tich	Two-Wire Serial Bus Clock High period *1	8T			ns
tiss	Setup time for start condition	4T			ns
tihs	Hold time for start condition	4T			ns
tisd	Setup time for input data	4T			ns
tihd	Hold time for input data	4T			ns
toaa	Output delay time			4T	ns
toda	Hold time for output data	3T			ns
tisp	Setup time of stop condition	4T			ns
tihp	Hold time for stop condition	4T			ns

Note: T = one master clock cycle

Figure 18: Two-wire Serial Bus Signal Timing at the Pins of the Sensor

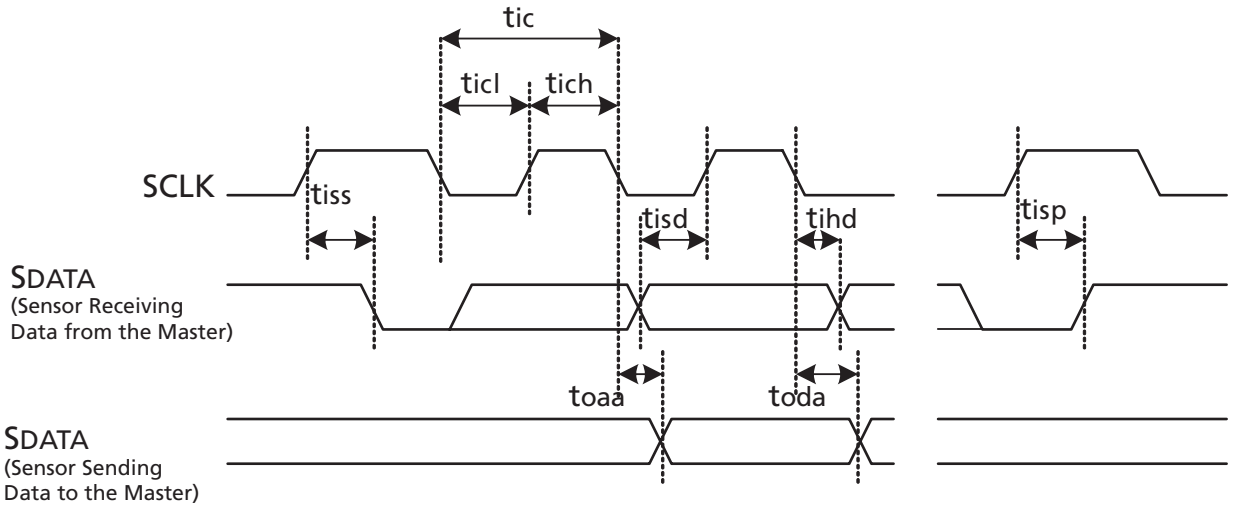
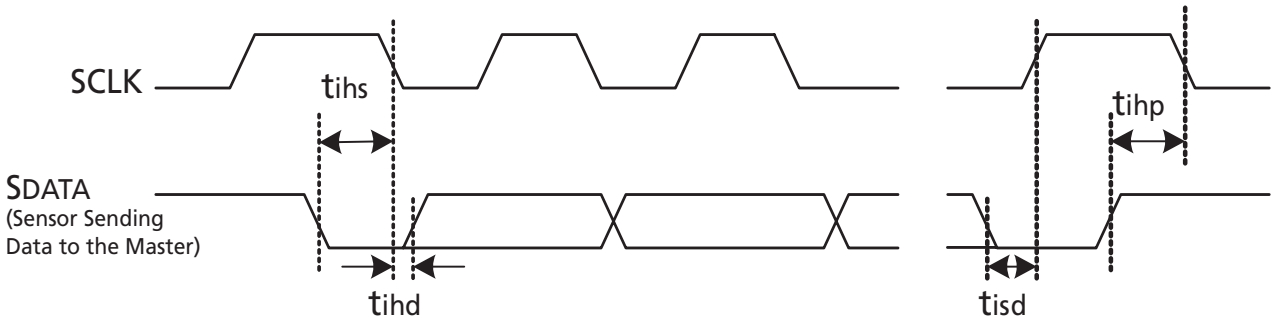
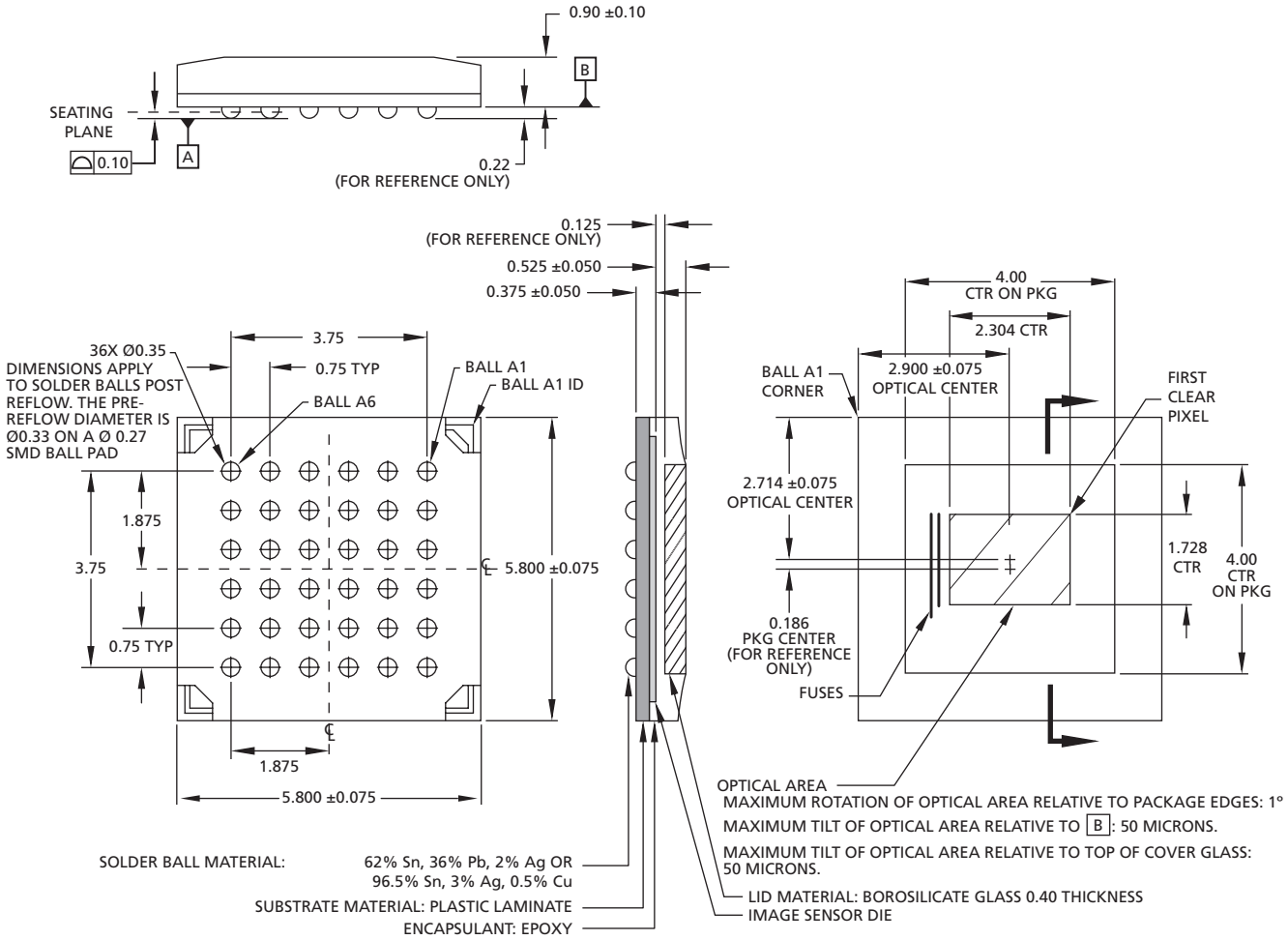


Figure 19: Two-wire Serial Bus Signal Timing at the Pins of the Sensor(2)



36-Ball ICSP Package

Figure 20: 36-Ball ICSP Package



Note: All dimensions in millimeters.

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Revision History

Rev. H 3/13/2006

- Documentum numbers corrected, data sheet designation updated and title updated.
- Updated notes 1 and 2 in Table 3 on page 11.

Rev. G 3/2/2006

- Updated Table 28 on page 59 for output delay time from 3T to 4T and hold time for output data from 4T to 3T.

Rev. F 2/2/2006

- Moved value of Output Delay Time (3T) from Min column to Max column in Table 28 on page 59.
- Updated descriptions of SDATA in Figure 18 on page 59 and Figure 19 on page 59.

Rev. E 1/19/2006

- Figure 9 on page 43 added more detail and Figure 11: Horizontal Timing on page 45 updated last data out value to 9D (was 90).
- Table 3 on page 11 definition of RESET changed from async to sync, Table 13 on page 36 R0x00D Reset Bit 12 definition expanded, Table 18 on page 47 columns swapped, and Table 23 on page 50 note added, Table 25 on page 51 column headings changed from Typical to MAX.

Rev. D 8/3/2005

- New outline drawing (36_ICSP(5_8x5_8)SMD_MTG-341.eps) per PCN1543-K12A_PHC, Figure 20 on page 60.

Rev. C 7/29/2005

- R161 changed to R161:1, new description and bits definition
- R161 changed to R164:1, new description
- R13:0[4] new description
- R32:0[10] is now reserved
- R33:0[10] is now reserved
- R40:2[12] new description
- IFP Block Diagram Edit
- Table 1 Edit, conversion to 1 column template

Rev. B 11/15/2004

- Operating Conditions
- DC Electrical Characteristics (two conditions)
- Operating Power Consumption
- STANDBY Power Consumption
- Two-Wire Serial Bus Timing
- Two-Wire Serial Bus Signal Timing (two figures)
- AC Electrical Characteristics
- AC Timing Diagram
- Register Summary 0x format
- Register Description - standardized bit value definitions and register format

Rev. A 10/6/2004

- Initial release