Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

DESCRIPTION

PT6312 is a Vacuum Fluorescent Display (VFD) Controller driven on a 1/4 to 1/11 duty factor. Eleven segment output lines, 6 grid output lines, 5 segment/grid output drive lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip micro computer. Serial data is fed to PT6312 via a three-line serial interface. It is housed in a 44-pin plastic LQFP Package and is functionally compatible with μpD16312.

FEATURES

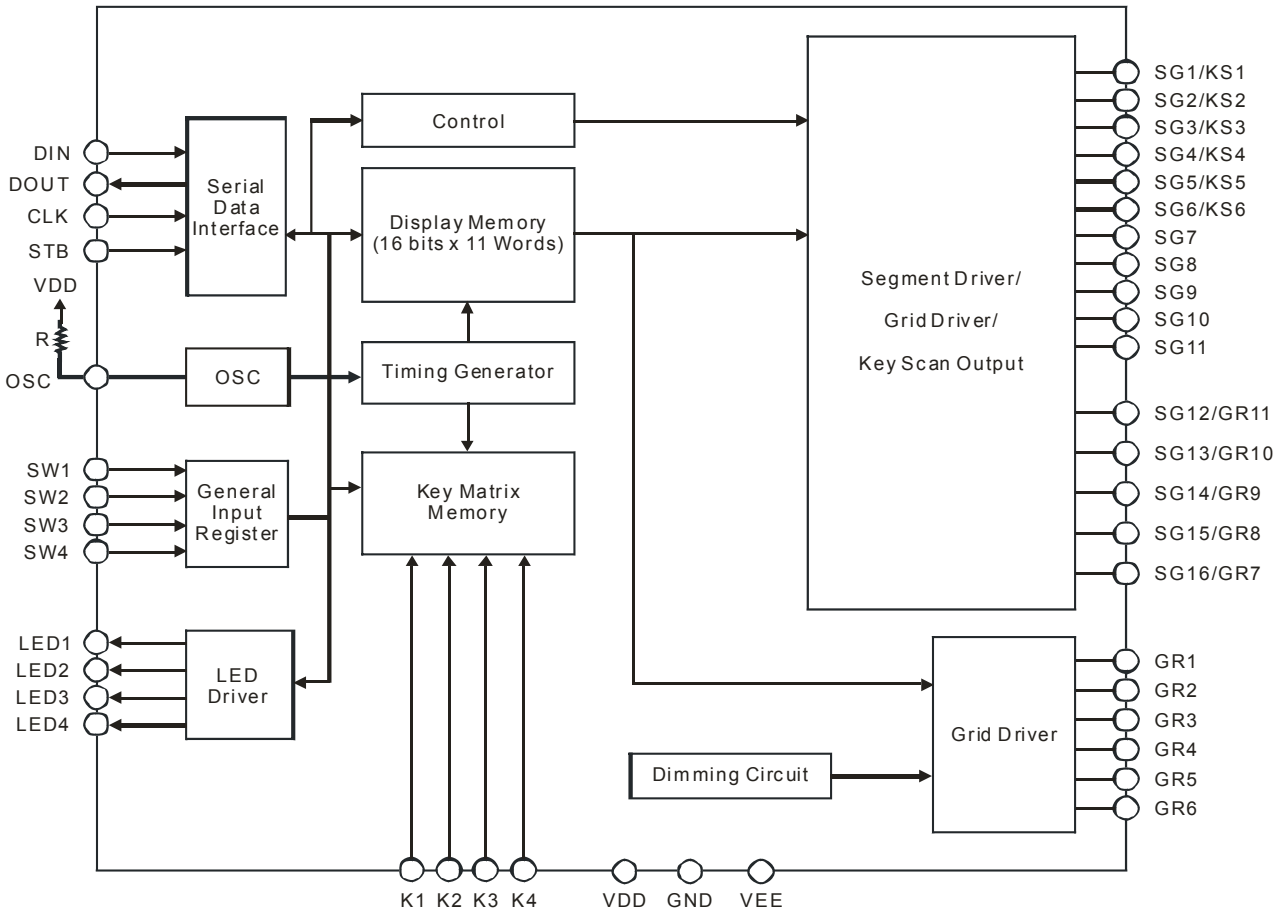
- CMOS technology
- Low power consumption
- Key scanning (6 x 4 matrix)
- Multiple display modes: (11 segments, 11 digits to 16 segments, 6 digits)
- 8-Step dimming circuitry
- LED ports provided (4 channels, 20mA max.)
- 4- Bits general purpose input ports provided
- Serial interface for Clock, Data Input, Data Output, Strobe pins
- No external resistors needed for driver outputs
- Functional compatibility with μpD16312
- Available in 44-pin, LQFP package

APPLICATION

- Microcomputer peripheral devices

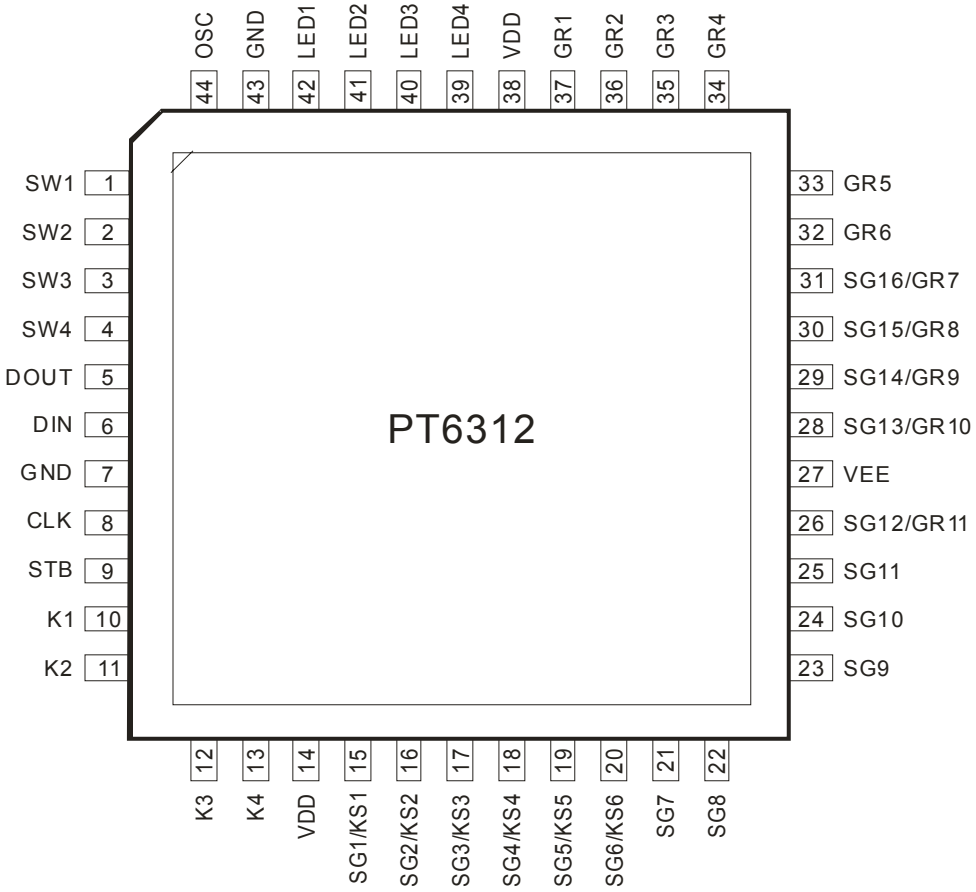
Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

BLOCK DIAGRAM



Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
SW1 to SW4	I	General purpose input pins	1 to 4
DOUT	O	Data output pin (N-Channel, Open-drain) This pin outputs serial data at the falling edge of the shift clock (starting from the lower bit).	5
DIN	I	Data input pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit).	6
GND	-	Ground pin	7, 43
CLK	I	Clock input pin This pin reads serial data at the rising edge and outputs data at the falling edge.	8
STB	I	Serial interface strobe pin The data input after the STB has fallen is processed as a command. When this in is “HIGH”, CLK is ignored.	9
K1 to K4	I	Key data input pins The data inputted to these pins is latched at the end of the display cycle.	10 to 13
VDD	-	Logic power supply	14, 38
SG1/KS1 to SG6/KS6	O	High-voltage segment output pins Also acts as the key source.	15 to 20
SG7 to SG11	O	High-voltage segment output pins	21 to 25
SG12/GR11 SG13/GR10 to SG16/GR7	O	High-voltage segment/grid output pins	26 28 to 31
VEE	-	Pull-down level	27
GR6 to GR1	O	High-voltage grid output pins	32 to 37
LED1 to LED4	O	LED output pin	42 to 39
OSC	I	Oscillator input pin A resistor is connected to this pin to determine the oscillation frequency.	44

Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

FUNCTION DESCRIPTION

COMMANDS

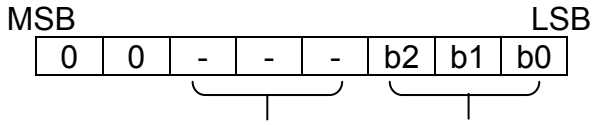
Commands determine the display mode and status of PT6312. A command is the first byte (b0 to b7) inputted to PT6312 via the DIN Pin after STB Pin has changed from “HIGH” to “LOW” State. If for some reason the STB Pin is set to “HIGH” while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

COMMAND 1: DISPLAY MODE SETTING COMMANDS

PT6312 provides 8 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to PT6312 via the DIN Pin when STB is “LOW”. However, for these commands, the bits 4 to 6 (b3 to b5) are ignored, bits 7 & 8 (b6 to b7) are given a value of “0”.

The Display Mode Setting Commands determine the number of segments and grids to be used (1/4 to 1/11 duty, 11 to 16 segments). When these commands are executed, the display is forcibly turned off, the key scanning stops. A display “ON” command must be executed in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.

When Power is turned “ON”, the 11-digit, 11-segment modes is selected.



Not relevant

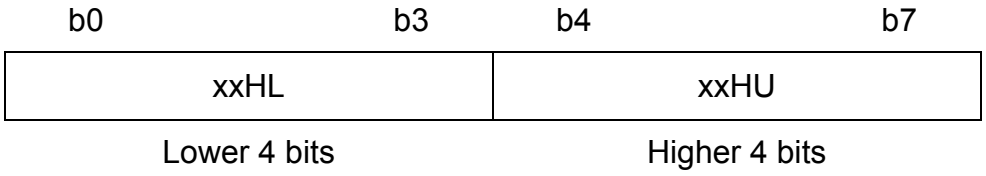
Display mode settings:
000: 4 digits, 16 segments
001: 5 digits, 16 segments
010: 6 digits, 16 segments
011: 7 digits, 15 segments
100: 8 digits, 14 segments
101: 9 digits, 13 segments
110: 10 digits, 12 segments
111: 11 digits, 11 segments

Display Mode and RAM Address

Data transmitted from an external device to PT6312 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM Addresses of PT6312 are given below in 8 bits unit.

SG1	SG4	SG5	SG8	SG9	SG12	SG13	SG16	
00HL		00HU		01HL		01HU		DIG1
02HL		02HU		03HL		03HU		DIG2
04HL		04HU		05HL		05HU		DIG3
06HL		06HU		07HL		07HU		DIG4
08HL		08HU		09HL		09HU		DIG5
0AHL		0AHU		1BHL		1BHU		DIG6
1CHL		1CHU		0DHL		0DHU		DIG7
1EHL		1EHU		1FHL		1FHU		DIG8
10HL		10HU		11HL		11HU		DIG9
12HL		12HU		13HL		13HU		DIG10
14HL		14HU		15HL		15HU		DIG11

-

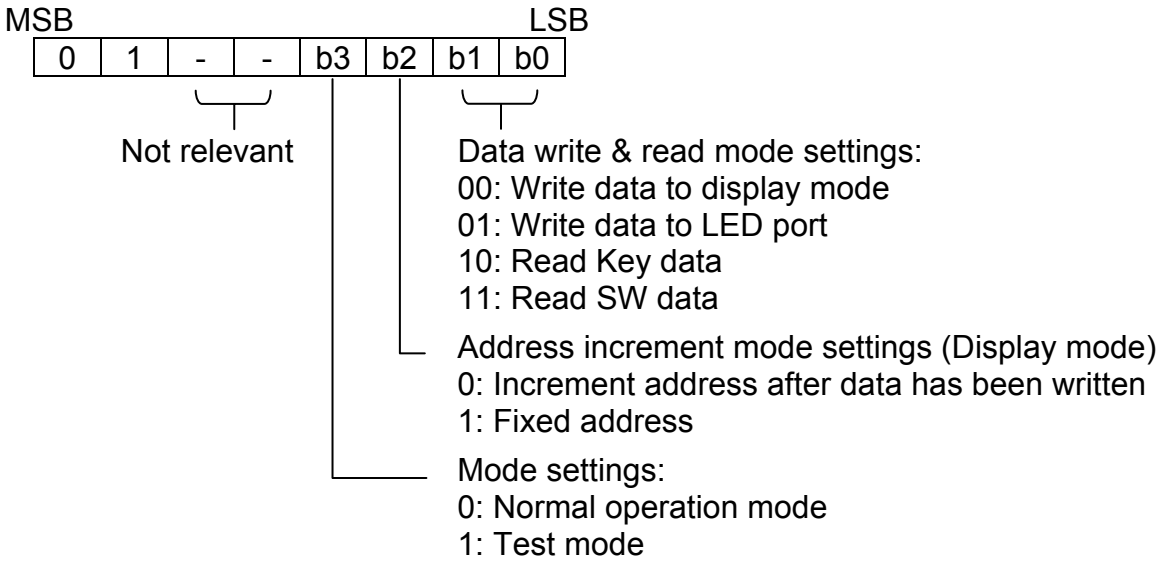


Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

COMMAND 2: DATA SETTING COMMANDS

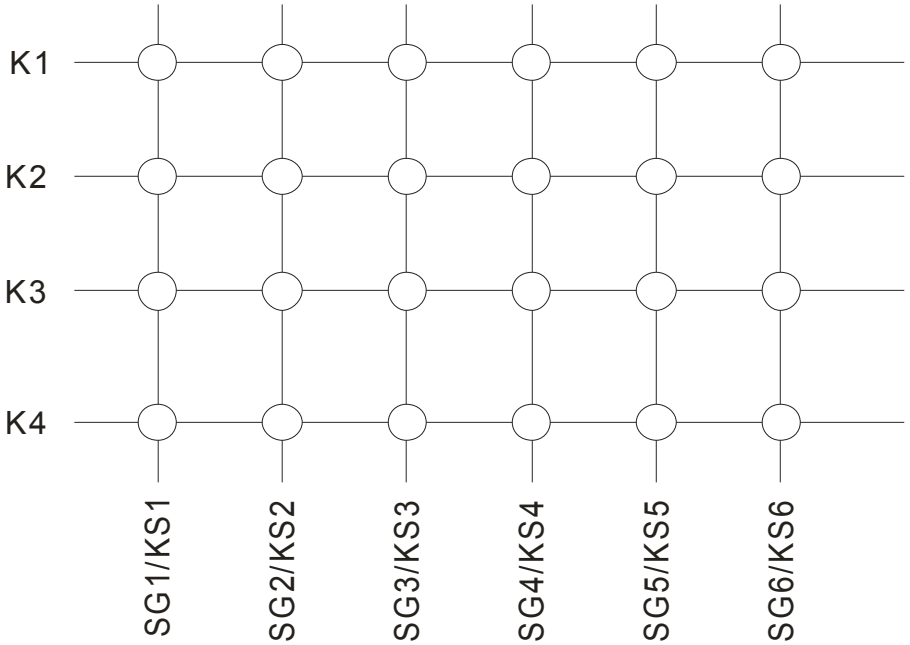
The Data Setting Commands executes the Data Write or Data Read Modes for PT6312. The data Setting Command, the bits 5 and 6 (b4, b5) are ignored, bit 7 (b6) is given the value of “1” while bit 8 (b7) is given the value of “0”. Please refer to the diagram below.

When power is turned ON, the bit 4 to bit 1 (b3 to b0) are given the value of “0”.



PT6312 Key Matrix & Key Input Data Storage RAM

PT6312 Key Matrix consists of 6 x 4 array as shown below:



Each data inputted by each key are stored as follows. They are read by a READ Command, starting from the last significant bit. When the most significant bit of the data (SG6 b7) has been read, the least significant bit of the next data (SG1 b0) is read.

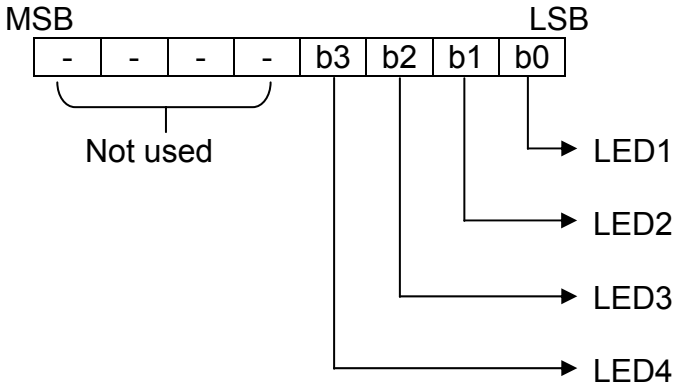
K1……K4	K1……K4
SG1/KS1	SG2/KS2
SG3/KS3	SG4/KS4
SG5/KS5	SG6/KS6
b0……b3	b4……b7

Reading Sequence

LED Display

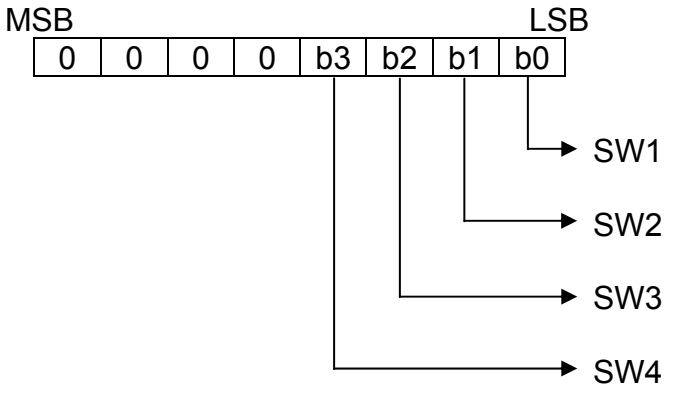
PT6312 provides 4 LED Display Terminals, namely LED1 to LED4. Data is written to the LED Port starting from the least significant bit (b0) of the port using a WRITE Command. Each bit starting from the least significant (b0) activates a specific LED Display Terminal -- b0 corresponds LED1 Display, b1 activates LED2 and so forth. Since there are only 4 LED display terminals, bits 5 to 8 (b4 ~ b7) are not used and therefore ignored. This means that b4 to b7 does NOT in anyway activate any LED Display, they are totally ignored.

When a bit (b0 ~ b3) in the LED Port is "0", the corresponding LED is ON. Conversely, when the bit is "1", the LED Display is turned OFF. For example, Bit 1 (as designated by b0) has the value of "0", then this means that LED1 is ON. It must be noted that when power is turned ON, bit 4 to bit 1 (b3 to b0) are given the value of "1". Please refer to the diagrams below.



Switch Data

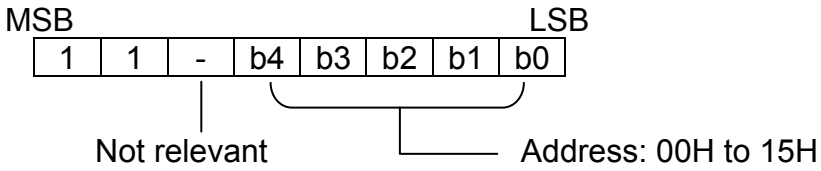
PT6312 provides 4 Switch Inputs, namely SW1 to SW4. SW Data is read starting from the least significant bit (b0) using a READ Command. Each bit starting from the least significant (b0) correspond to a specific Switch Input -- b0 corresponds SW1, b1 to SW2 and so forth. Since there are only 4 Switch Inputs, Bits 5 to 8 (b4 to 7) are given the value of "0". Please refer to the diagram below.



COMMAND 3: ADDRESS SETTING COMMANDS

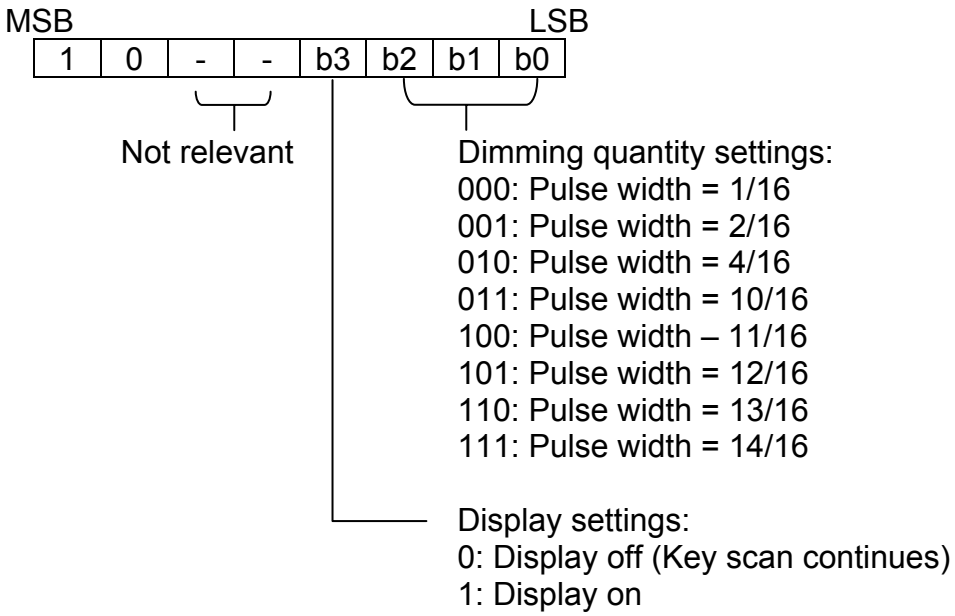
Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of “00H” to “15H”. If the address is set to 16H or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at “00H”.

Please refer to the diagram below.



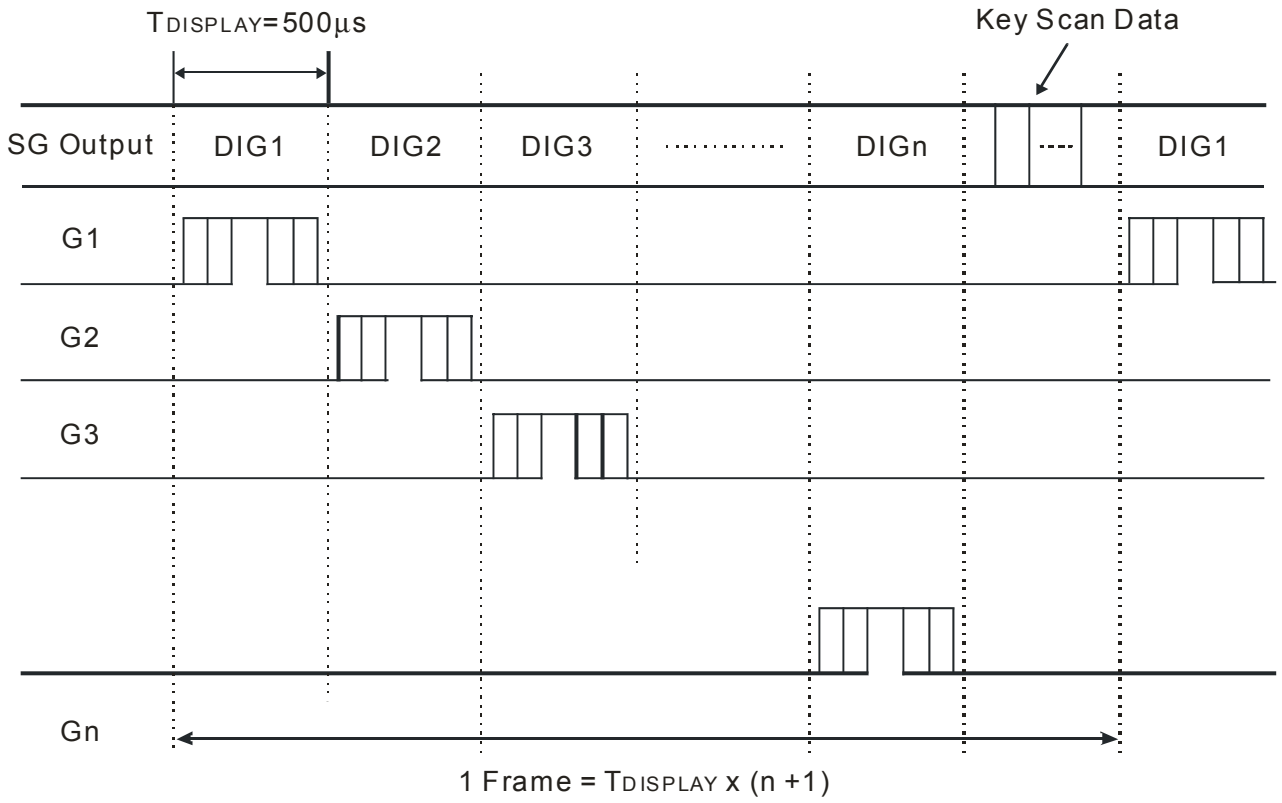
COMMAND 4: DISPLAY CONTROL COMMANDS

The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF (the key scanning is stopped).



SCANNING AND DISPLAY TIMING

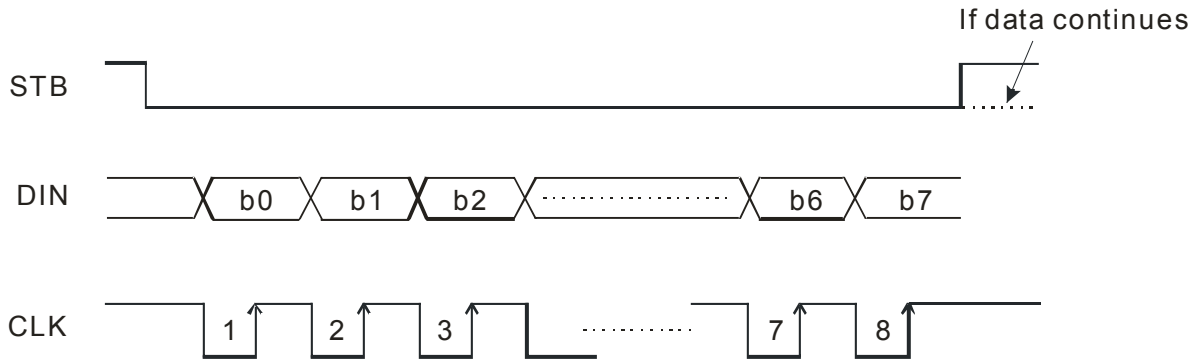
The Key Scanning and display timing diagram is given below. One cycle of key scanning consists of 1 frame. The data of the 6 x 4 matrix is stored in the RAM.



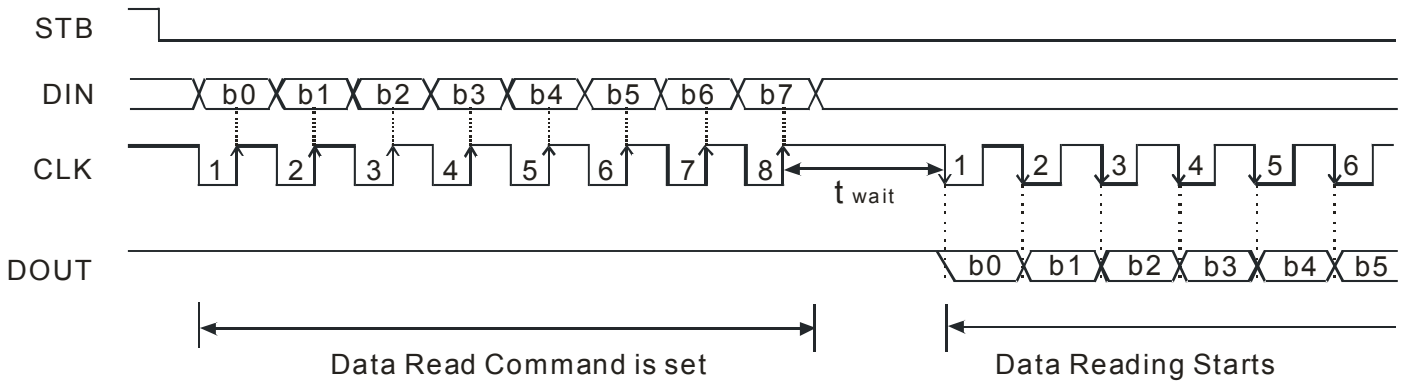
SERIAL COMMUNICATION FORMAT

The following diagram shows the PT6312 serial communication format. The DOUT Pin is an N-channel, open-drain output pin, therefore, it is highly recommended that an external pull-up resistor (1 KΩ to 10 KΩ) must be connected to DOUT.

Reception (Data/Command Write)



Transmission (Data Read)



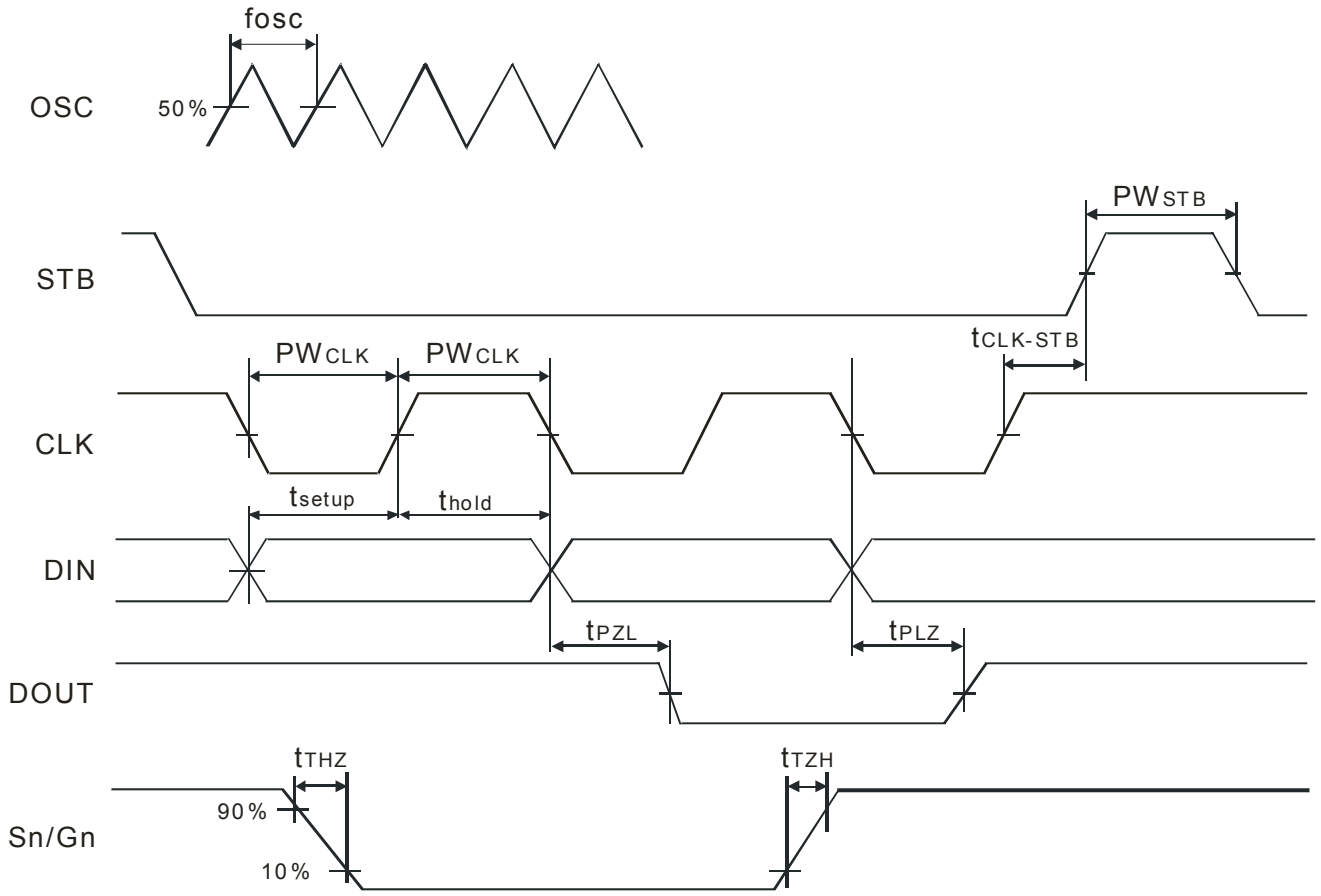
where: twait (waiting time) ≥ 1μs

It must be noted that when the data is read, the waiting time (twait) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to 1μs.

Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

SWITCHING CHARACTERISTIC WAVEFORM

PT6312 Switching Characteristics Waveform is given below.

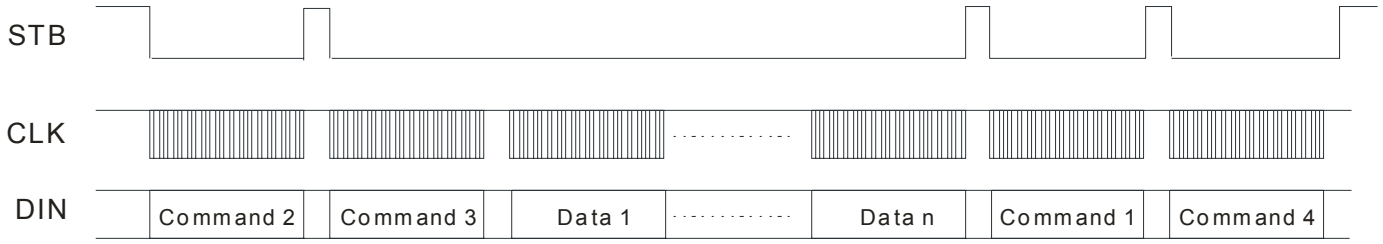


where:

PW CLK (Clock Pulse Width) ≥ 400ns
PW STB (Strobe Pulse Width) ≥ 1μs
t setup (Data Setup Time) ≥ 100ns
thold (Data Hold Time) ≥ 100ns
tCLK-STB (Clock - Strobe Time) ≥ 1μs
tTHZ (Fall Time) ≤ 120μs
tTZH (Grid Rise Time) ≤ 0.5μs
tPZL (Propagation Delay Time) ≤ 100ns
tTZH (Segment Rise Time) ≤ 2μs
tPLZ (Propagation Delay Time) ≤ 300ns
fosc = Oscillation Frequency

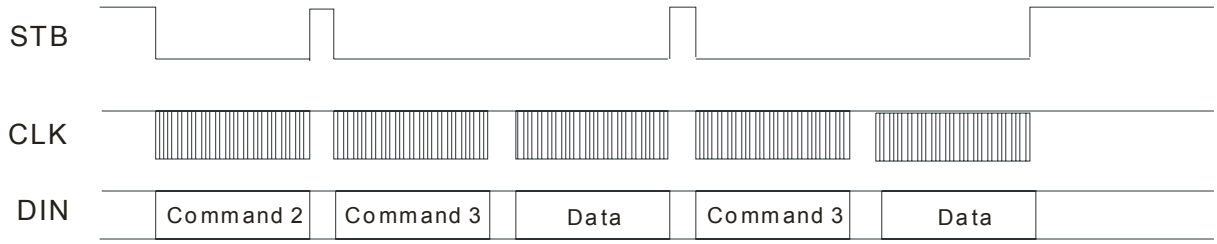
APPLICATIONS

Display memory is updated by incrementing addresses. Please refer to the following diagram.



where:
Command 1: Display mode setting command
Command 2: Data setting command
Command 3: Address setting command
Data 1 to n: Transfer display data (2 bytes max.)
Command 4: Display control command

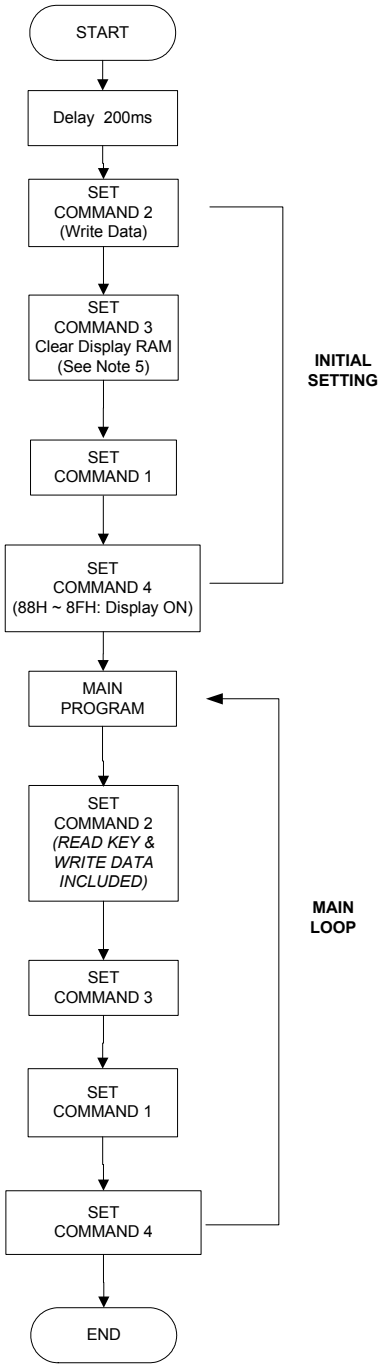
The following diagram shows the waveforms when updating specific addresses.



where:
Command 2: Data setting command
Command 3: Address setting command
Data: Display data

Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

RECOMMENDED SOFTWARE FLOWCHART



Notes:
1. Command 1: Display Mode Commands
2. Command 2: Data Setting Commands
3. Command 3: Address Setting Commands
4. Command 4: Display Control Commands
5. When IC power is applied for the first time, the contents of the Display RAM is not defined; thus, it is strongly suggested that the contents of the Display RAM be cleared during the initial setting.

ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta=25℃, GND=0V)

Parameter	Symbol	Ratings	Unit
Logic supply voltage	VDD	-0.5 to +7	V
Driver supply voltage	VEE	VDD +0.5 to VDD -40	V
Logic input voltage	V1	-0.5 to VDD +0.5	V
VFD driver output voltage	V0	VEE -0.5 to VDD +0.5	V
LED driver output current	IOLED	+25	mA
VFD driver output current	IVOFD	-40 (Grid) -15 (Segment)	mA
Operating temperature	Topr	-40 to +85	℃
Storage temperature	Tstg	-65 to +150	℃

RECOMMENDED OPERATING RANGE

(Unless otherwise stated, Ta=-40 to +85℃, GND=0V)

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Logic supply voltage	VDD	3.0	5	5.5	V
High-level input voltage	VIH	0.7VDD	-	VDD	V
Low-level input voltage	VIL	0	-	0.3VDD	V
Driver supply voltage	VEE	VDD -35	-	0	V

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, VDD=5V, GND=0V, VEE=VDD-35V, Ta=25℃)

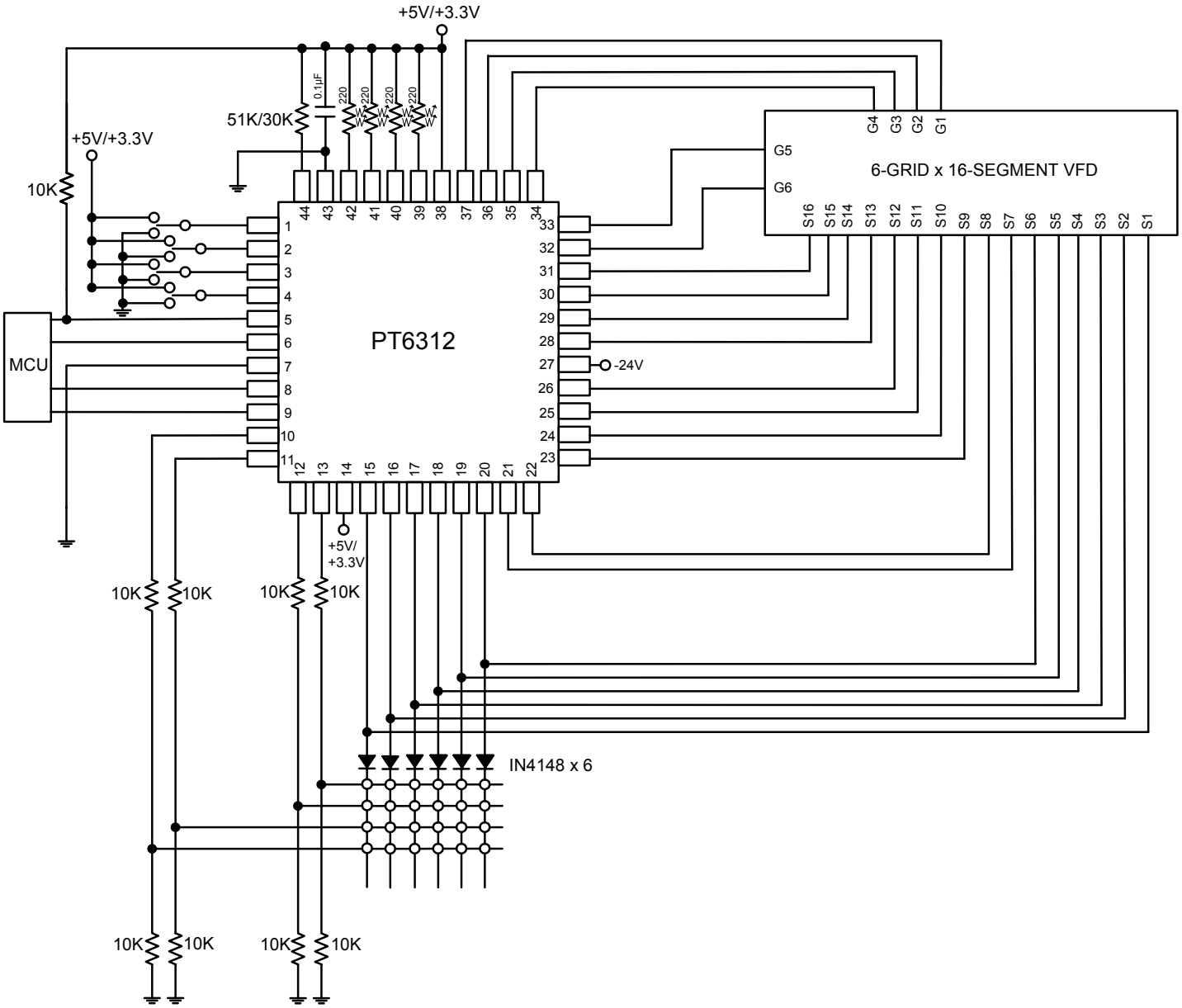
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-level output voltage	VOHLED	IOHLED=-1mA LED1 to LED4	0.9VDD	-	-	V
Low-level output voltage	VOLLED	IOLLED=+20mA LED1 to LED4	-	-	1	V
Low-level output voltage	VOLDOUT	DOUT, IOLDOUT=4mA	-	-	0.4	V
High-level output current	IOHSG	VO=VDD -2V SG1 to SG11	-3	-	-	mA
High-level output current	IOHGR	VO=VDD -2V GR1 to GR6, SG12/GR11 to SG16/GR7	-15	-	-	mA
High-level input voltage	VIH	-	0.7VDD	-	-	V
Low-level input voltage	VIL	-	-	-	0.3VDD	V
Oscillation frequency	fosc	R=51KΩ	350	500	650	KHz
Input current	II	VI=VDD or VSS	-	-	±1	μA
Dynamic current consumption	IDDdyn	Under no load display off	-	-	5	mA

(Unless otherwise stated, VDD=3.3V, GND=0V, VEE=VDD-35 V, Ta=25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-level output voltage	VOHLED	IOHLED=-1mA LED1 to LED4	0.9VDD	-	-	V
Low-level output voltage	VOLLED	IOLLED=+20mA LED1 to LED4	-	-	1	V
Low-level output voltage	VOLDOUT	DOUT, IOLDOUT=4mA	-	-	0.4	V
High-level output current	IOHSG	VO=VDD -2V SG1 to SG8	-1.5	-	-	mA
High-level output current	IOHGR	VO=VDD -2V GR1 to GR6, SG9 to SG16/GR7	-6	-	-	mA
High-level input voltage	VIH	-	0.7VDD	-	-	V
Low-level input voltage	VIL	-	-	-	0.3VDD	V
Oscillation frequency	fosc	R=30KΩ	350	500	650	KHz
Input current	II	VI=VDD or VSS	-	-	±1	μA
Dynamic current consumption	IDDdyn	Under no load display off	-	-	3	mA

Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

6-GRID X 6-SEGMENT VFD APPLICATION CIRCUIT



Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

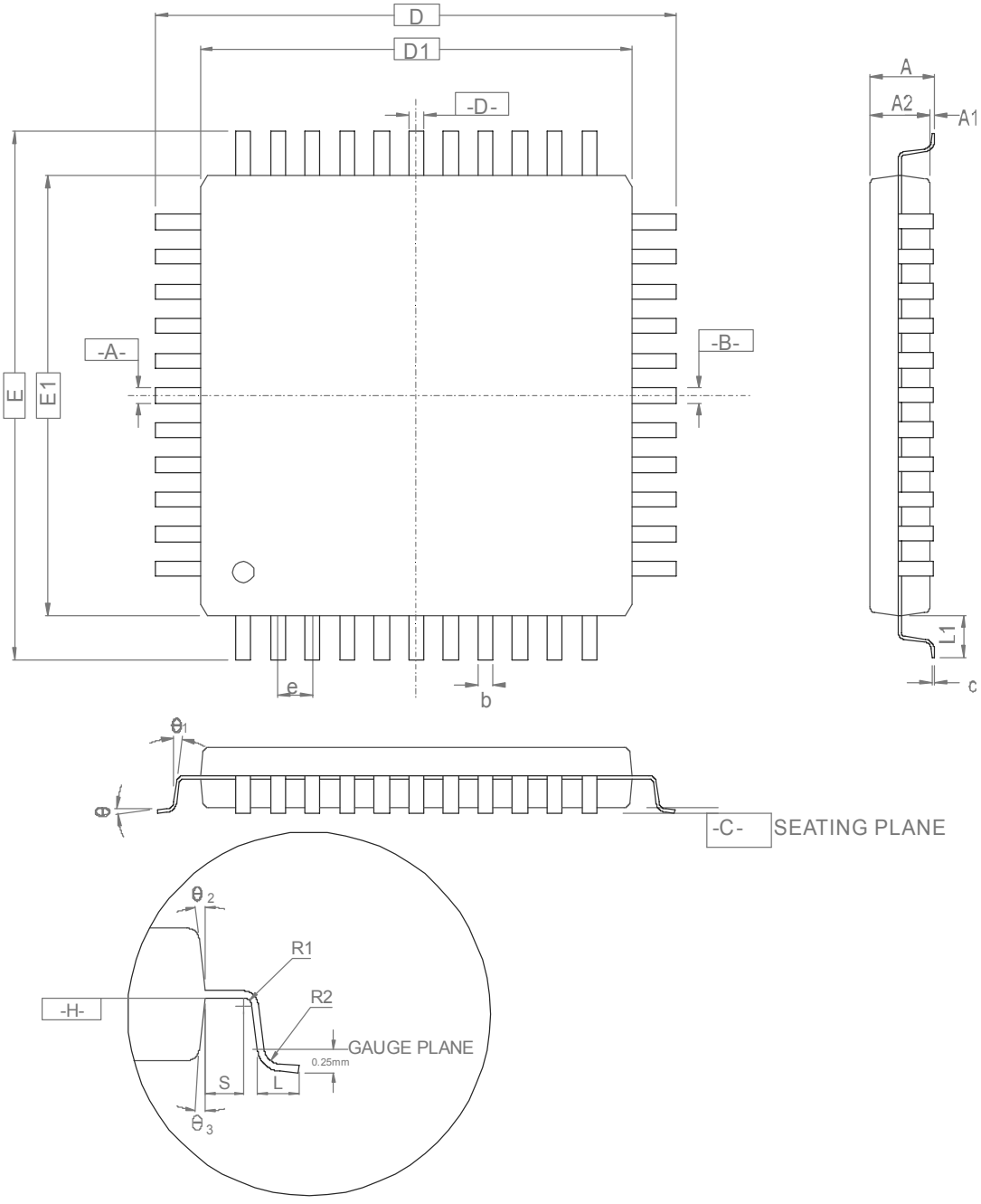
ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6312LQ	44-pin, LQFP	PT6312LQ

Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

PACKAGE INFORMATION

44 PINS LQFP (BODY SIZE: 10MM X 10MM; PITCH=0.80MM; THK BODY: 1.40MM)



Symbol	Min.	Nom.	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
b1	0.30	0.35	0.40
D	12.00 BASIC		
D1	10.00 BASIC		
e	0.80 BASIC		
E	12.00 BASIC		
E1	10.00 BASIC		
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°
C	0.09	-	0.20
L	0.45	0.60	0.75
L1	1.00 REF		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-

Notes:
1. Controlling Dimensions are in millimeters .
2. Dimensioning and tolerancing per ASME Y14.5M-1994.
3. The top package body size may be smaller than the bottom package size by as much as 0.15mm.
4. Datums A-B and D to be determined at datum plane H.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
6. Details of pin1 identifier are optional but must be located within the zone indicated.
7. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm pitch packages.
8. A1 is defined as the distance from the seating plane to the lowest point on the package body.
9. Refer to JEDEC STD MS-026 Variation BCB

JEDEC is the trademark of JEDEC SOLID STATE TECHNOLOGY ASSOCIATION