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2W × 2 Class AB Audio Power Amplifier **PT2303**

DESCRIPTION

The PT2303 is a power amplifier utilizing CMOS Technology specially designed for audio purpose. It can deliver 2W × 2 power output to the 5V power voltage. The power consumption is very low in stand-by. Total harmonic distortion is lower than 0.03%. The output mode can be switched between the SE (Single-Ended) or BTL (Bridge-Tied Load) mode. Built-in over-temperature protection, package size is not occupies PCB space. It is suitable for small or portable products.

FEATURES

- CMOS Technology
- Stereo input
- Output power 2W × 2 (4Ω)
- Low harmonics distortion (0.03%)
- SE and BTL modes operation
- Suppress the pop and click noise when mode changed
- Shutdown function, turn on can into save mode (Icc<0.5μA)
- Built-in overheat protect

APPLICATIONS

- LCD monitor (for TV)
- Portable audio
- Multimedia speakers
- Other audio applications

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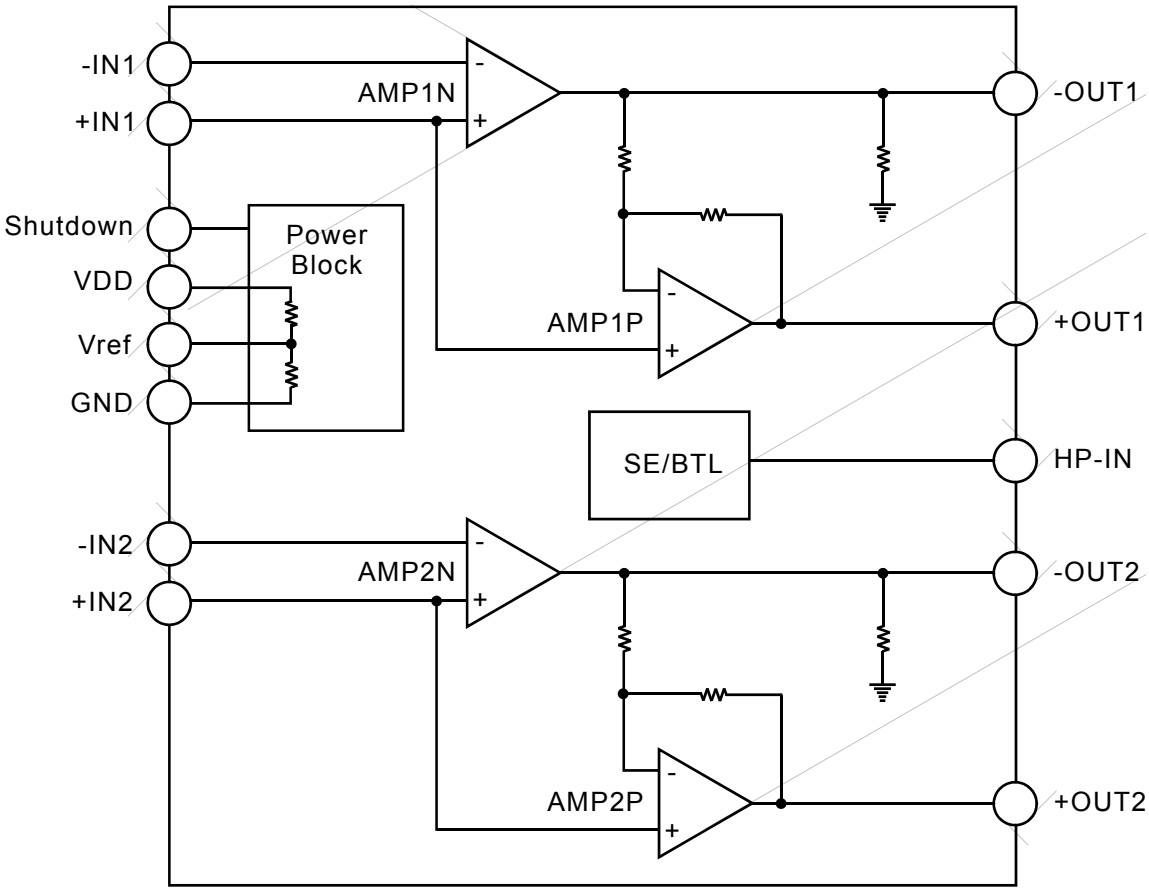
BLOCK DIAGRAM



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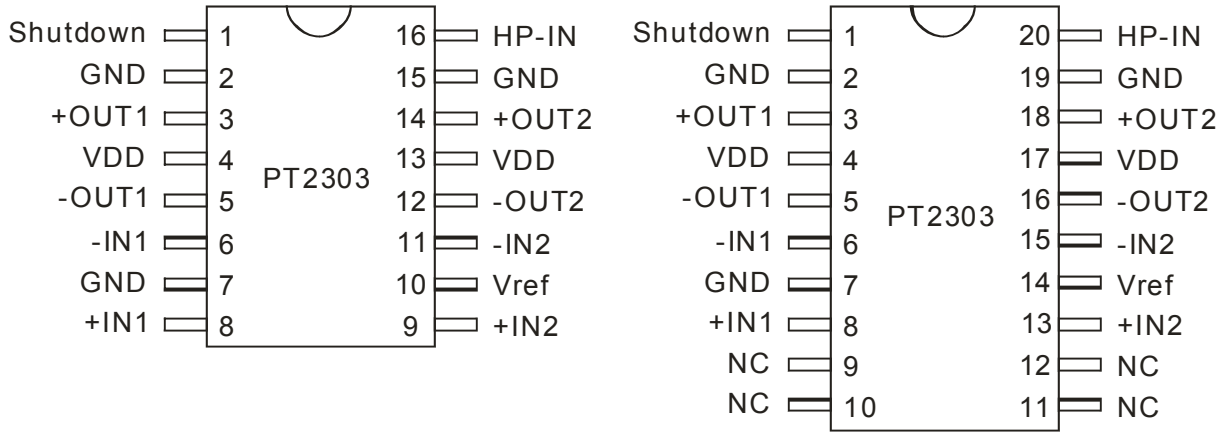
PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.	
			16 Pins	20 Pins
Shutdown	I	Shutdown pin ◦ Entire IC into the shutdown mode when this pin connected to the Vcc.	1	1
GND	-	Ground	2	2
+OUT1	O	Channel 1 output (+)	3	3
VDD	-	Supply voltage input	4	4
-OUT1	O	Channel 1 output (-)	5	5
-IN1	I	Channel 1 input (-)	6	6
GND	-	Ground	7	7
+IN1	I	Channel 1 input (+)	8	8
+IN2	I	Channel 2 input (+)	9	13
Vref	I	Bias reference bypassing	10	14
-IN2	I	Channel 2 input (-)	11	15
-OUT2	O	Channel 2 output (-)	12	16
VDD	-	Supply voltage input	13	17
+OUT2	O	Channel 2 output (+)	14	18
GND	-	Ground	15	19
HP-IN	I	Output mode select, connected to the VDD for SE mode or GND for BTL mode	16	20
NC	-	No Connect	-	9 ~ 12

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FUNCTION DESCRIPTION

POWER SUPPLY

The operating voltage of PT2303 is from 3V to 5V, In general operation 5V is recommended, it can deliver higher power output. When the supply voltage less then 3V the IC can work properly, but the distortion will rise. After the supply voltage exceed 6V the temperature of package outside will rising quickly due to higher stand-by current consumption.

SHUTDOWN

When the supply still powered the chip, pull-up the shutdown pin to VDD level will take chip into the shutdown mode. After the shutdown mode is active, the total current consumption is less than 0.5μA and the all of input or output pins no voltage output. When shutdown pin set to GND, the IC is back to the normal operation.

Shutdown Pin	Output State
VDD	Shutdown ON
GND	Normal

VOLTAGE GAIN ADJUST

The output stage structure of the PT2303 is Bridge Tied Loaded (BTL), the close loop voltage gain can be get from following formula.

Gain = 20log (Rf ÷ Ri) + 6dB

The close loop gain can be adjusted by external resistance, in general purpose the 6dB gain setting is recommended, please reference to the application circuit. If the amplitude of input voltage in lower level (ex. < 2Vpp), it can raise the voltage gain to get enough power output. Recommended of the minimum series resistance (Ri) is 10KΩ to ensure IC have appropriate input impedance. Please refer to following table.

External Resistance	Gain= 0dB	Gain= 6dB	Gain=12dB
Ri	20KΩ	20KΩ	10KΩ
Rf	10KΩ	20KΩ	20KΩ

If the amplitude of input signal exceed the VDD-GND range, or voltage gain setup too high, the input stage is very easy overload and distorted. Please make sure the amplitude of audio source (Vin) and setting the best gain value, in general use the gain setup to +6dB is recommended. Please refer to following table.

Operating Voltage	Gain= 0dB	Gain= 6dB	Gain=12dB
VDD=3V	Vin <5Vpp	Vin <2.5Vpp	Vin <1.25Vpp
VDD=5V	Vin <8Vpp	Vin<4Vpp	Vin<2Vpp

SE/BTL MODE SWITCHING

PT2303 have two output modes, SE (Single-Ended) or BTL (Bridge-Tied Load). When driving a 4Ω speaker load suggestion set to the BTL mode for get the more power output. And driving a 32Ω headphone load, it can be set to SE mode and turn-off the un-work amplifier to decrease stand-by power consumption. Switching between the SE/BTL modes is controlled by the HP-IN pin, please refer to following table:

HP-IN	Output Mode
VDD	SE
GND	BTL

OVER TEMPERATURE PROTECTION

The PT2303 has a built-in over temperature protection circuit, it will turn off all output when the chip temperature over 130℃, the chip will return to normal operation automatically after the temperature cool down to 100℃.

POP AND CLICK SURPRESS

A power amplifier uses single supply voltage may almost have inrush noise on output in the power-on/off period. It is because of the output DC potential needs time to stable on 1/2VDD, the period relative with the capacitance (CB) on the Vref pin. Larger CB value will extend the stable time, and also can suppress the noise happened in power-on. In supply voltage=5V and CB=2.2μF, stable time is about 300mS. The value of CB also relative with the value of the DC blocking capacitor connected in input terminal. In general condition the time constant of DC blocking capacitor should be less than CB stable time. The recommended value of DC blocking capacitor is 1μF, and the capacitor of output terminal connected to 32Ω headphone is 220μF. Smaller capacitance can shorten the charge time to suppress the pop noise, both the input and output capacitance will limited the low frequency extend range.

HEAT DISSIPATION

During normal operation, the chip only consumes very little stand-by current. In high output power conditions, the package temperature will rise. For proper operating temperature, a modest heat sink mounted on the top side of the chip is required. The thermal resistance requirement of the heat sink demand may be obtained by the formula below:

$\theta JA = (T_J\,(max) - T_A)/P_{DISS}$

P_{DISS} = IC dissipation power
T_J (max) = Maximum chip conjunction temperature
T_A = external environment temperature
θ_{JA} = thermal resistance from chip conjunction to ambience environment

With 60% estimated efficiency (eff), PT2303 in 2W + 2W output power dissipation is probably

$P_{DISS} = (Po \div eff) - Po = 2.6W$

The maximum chip conjunction temperature is 150℃, Exceed this temperature will damage the chip, assuming the outside environment air temperature is 50℃. From the chip conjunction dissipation to external environment thermal resistance θ_{JA} should be:

$\theta_{JA} = (150 – 50) \div 2.6 = 38.4℃/W$

The PT2303 chip conjunction to case thermal resistance θ_{JC} is 26℃ /W. Therefore the heat sink thermal resistance should be:

$\theta_{JA} - \theta_{JC} = 12.4℃/W$

In normal operating, PT2303 needs at least 2 sq inch PCB for heat dissipate; it should be use whole copper foil to cover on it for enough heat dissipation space. We suggest using two-layer PCB for better heat dissipation. The track connected to the output and power pin of IC should be as thick as possible for better heat dissipation ability. If IC doesn't have enough heat dissipation space (>1 sq inch), and IC is always in full power output situation, an additional heat sink should placed on the chip.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Min.	Max.	Unit
Supply voltage	VDD		0	7	V
Operating temperature	Tamb		-40	+85	℃
Storage temperature	Tstg		-65	+150	℃
Maximum input voltage	Vimax		-0.3	Vcc+0.3	V
Maximum input current	Iimax	*	-10	+10	mA

*Input pins surge current can be reached 100mA will not induce the CMOS latched up.

PACKAGE THERMAL CHARACTERISTICS

PACKAGE TYPE: SOP16L, 300MIL

Parameter	Symbol	Condition	Value	Unit
From chip conjunction dissipation to external environment	θ_{JA}	Ta=25℃	88.8	℃/W
From chip conjunction dissipation to package surface	θ_{JC}		26	℃/W

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ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, VDD=5V, bandwidth=22~22KHz)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Supply voltage	VDD			3	5	6	V
Operating current	Is	SE Mode		4	6	10	mA
		BTL Mode		6	8	12	
		Shutdown=ON		0.1	0.5	1	μA
Two channels gain error	Gerr	Ri=Rf=20KΩ		-1	0	+1	dB
THD+N	THD	Po=0.2W, RL=4Ω		0.03	0.05	0.07	%
		Po=1W, RL=4Ω		0.06	0.08	0.15	
		Po=50mW, RL=32Ω		0.03	0.05	0.08	
Power output	Po	BTL	THD=1%, RL=8Ω	1.0	1.1	1.2	W
			THD=10%, RL=8Ω	1.2	1.4	1.6	
			THD=1%, RL=4Ω	1.4	1.6	1.8	
			THD=10%, RL=4Ω	1.8	2.0	2.1	
		SE	THD=1%, RL=32Ω	80	85	90	mW
			THD=10%, RL=32Ω	100	110	120	
Signal-to-Noise	SNR	A-Weighted		95	100	-	dB
Residual noise	Vno	A-weighted		-	35	50	μV
Output offset	Voff	+OUT ~ -OUT		2	10	30	mV
Channel separation	CS	BTL	F=1KHz	80	90	100	dB
		SE		80	85	95	
Power Signal-to-Noise repel rate	PSRR	BTL	F=100Hz	60	70	80	dB
		SE		40	45	50	
Temperature protect	TH	Overheat close	-	-	130	140	℃
		Back to work	-	85	100	-	
Shutdown voltage	VSD	Shutdown ON	VDD=3~5V Shutdown pin	0.45	0.6	-	VDD
		Shutdown OFF		-	0.15	0.2	
SE/BTL voltage	VSB	SE	VDD=3~5V	0.75	0.8	-	VDD
		BTL		-	0.2	0.3	

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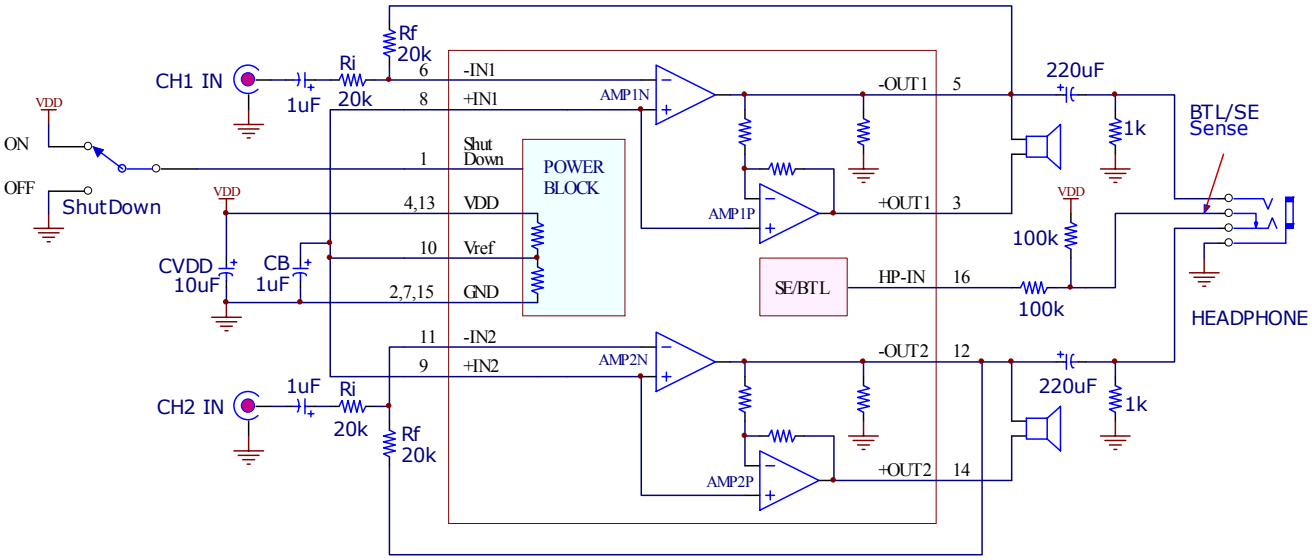
APPLICATION CIRCUIT



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ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2303-D	16 Pins, DIP, 300mil	PT2303-D
PT2303-S	16 Pins, SOP, 300mil	PT2303-S
PT2303-TX	20 Pins, TSSOP	PT2303-TX

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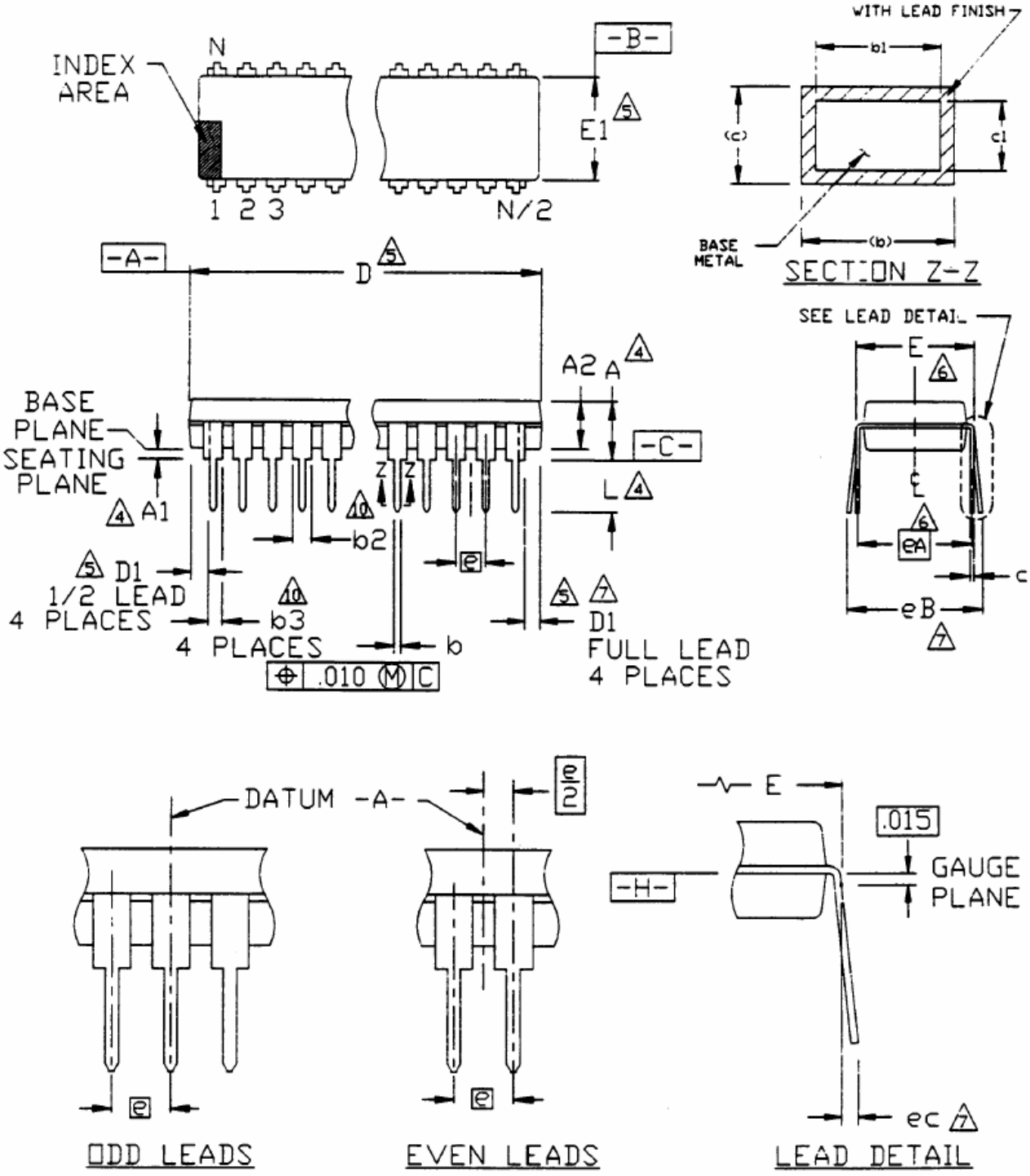
PACKAGE INOFRMATION

16PINS, DIP, 300MIL



Symbol	Min.	Nom.	Max.
A	-	-	0.210
A1	0.015	-	-
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	0.780	0.790	0.800
D1	0.005	-	-
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e		0.100 bsc	
eA		0.300 bsc	
eB	-	-	0.430
eC	0.000	-	0.060
L	0.115	0.130	0.150

Notes:
1. Controlling Dimension: INCHES.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimensions A, A1 and L are measured with the package seated in JEDEC Seating Plane Gauge GS-3.
4. D, D1 and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
5. E and eAmeasured with the leads constrained to be perpendicular to datum -C-.
6. eB and eA are measured at the lead tips with the leads unconstrained.
7. N is the maximum number of terminal positions (N=16).
8. Pointed or rounded lead tips are preferred to ease insertion.
9. b2 and b3 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25mm).
10. Variation AB is a full lead package.
11. Distance between leads including dambar protrusions to be 0.005 in minimum.
12. Datum plane -H- coincident with the bottom of lead where lead exits body.
13. Refer to JEDEC MS-001 Variation AB.

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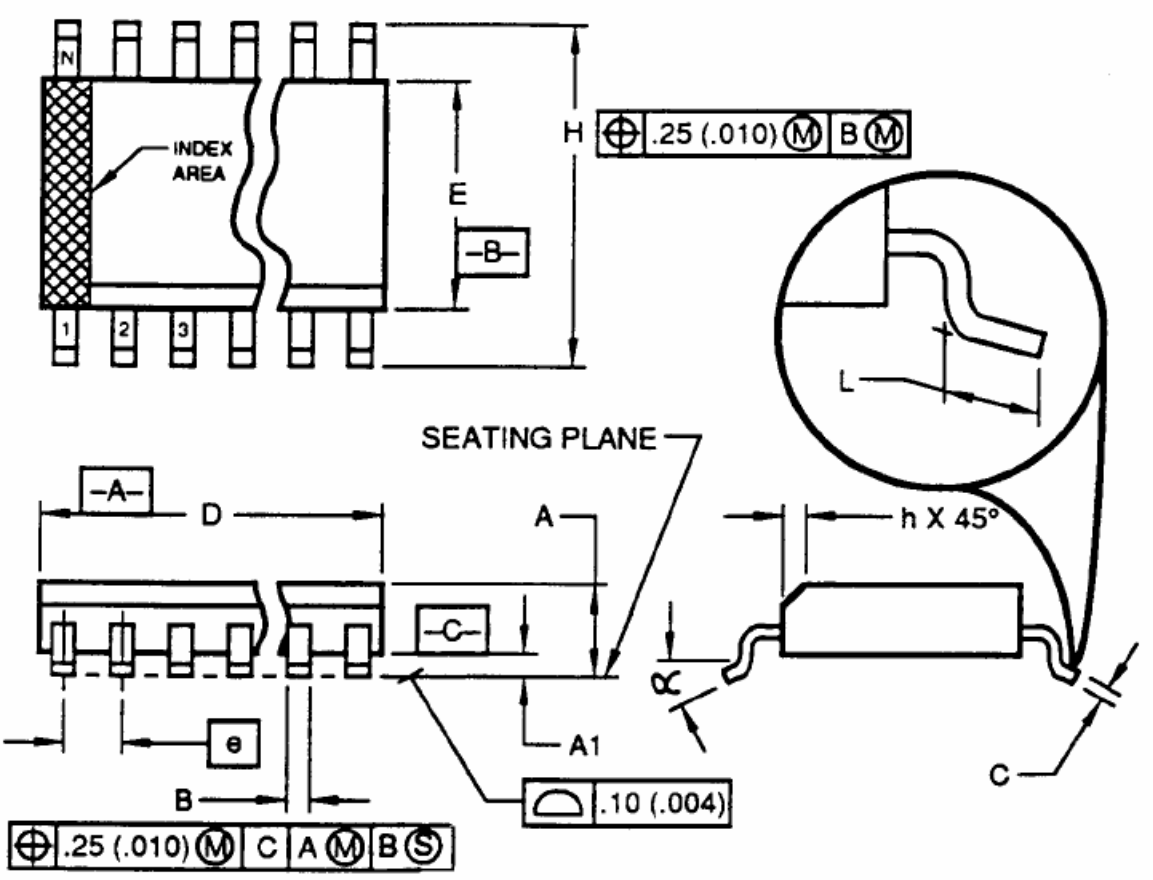
16 PINS, SOP, 300 MIL



Symbol	Min.	Max
A	2.35	2.65
A1	0.10	0.30
B	0.33	0.51
C	0.23	0.32
D	10.10	10.50
E	7.40	7.60
e	1.27 BSC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0^o	8^o

Notes:
1. Controlling Dimension: MILLIMETER
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.15mm (0.006 in) per side.
4. Dimension E does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25 mm (0.010 in.) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. L is the length of the terminal for soldering to a substrate.
7. N is the number of terminal positions (N=16).
8. The lead width B, as measured 0.36 mm (0.014in) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024in.)
9. Refer to JEDEC MS-013 Variation AA.

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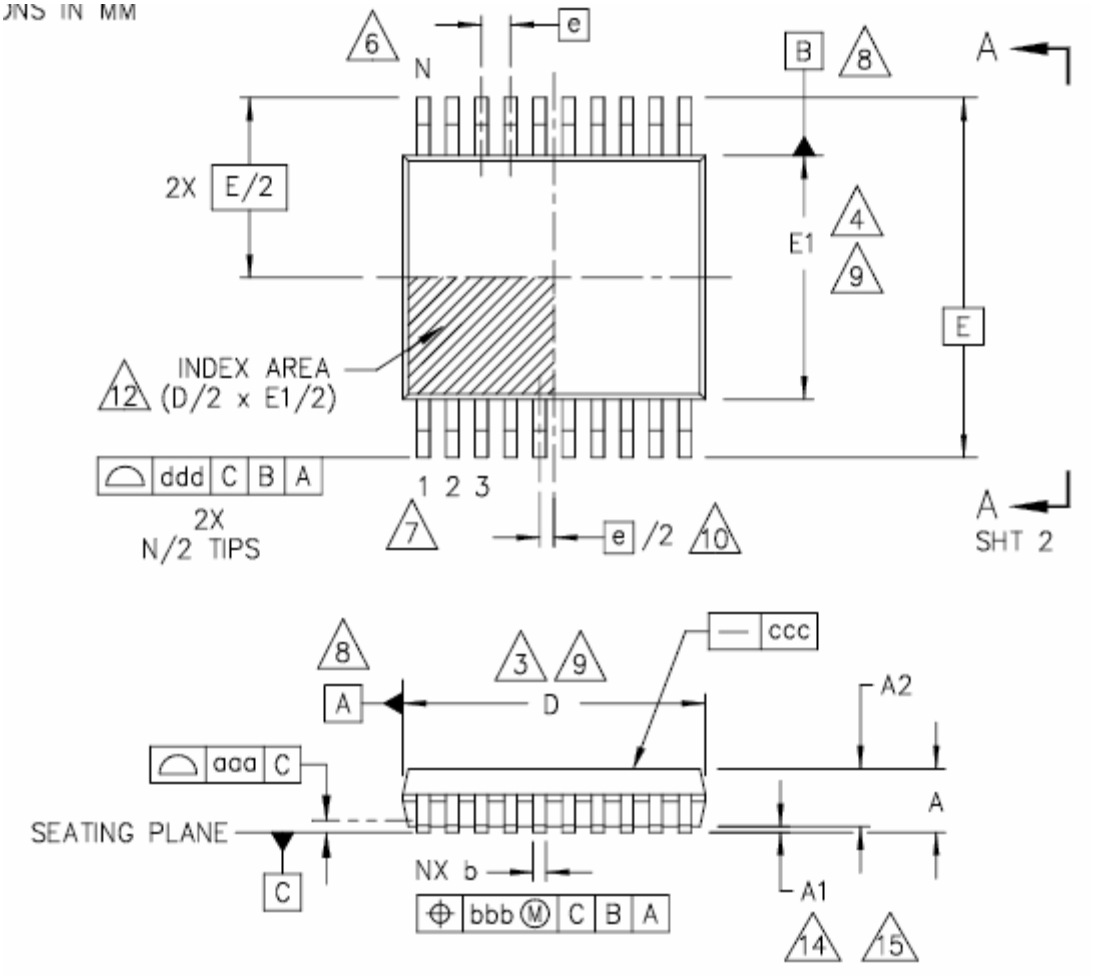
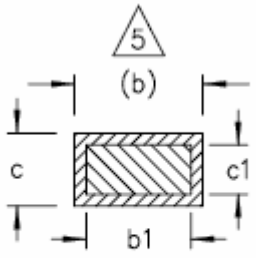
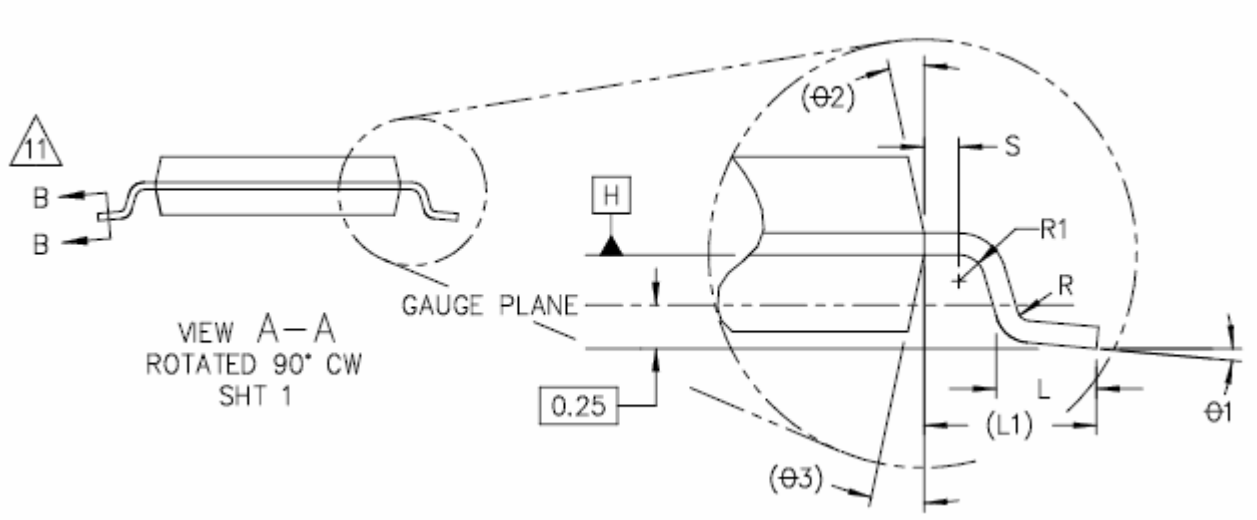
20PINS, TSSOP, 173MIL





SECTION B–B



Symbols	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
b1	0.19	0.22	0.25
c	0.09	-	0.20
c1	0.09	-	0.16
D	6.40	6.50	6.60
E		6.40 BSC.	
E1	4.30	4.40	4.50
e		0.65 BSC.	
L	0.45	0.60	0.75
L1		1.00 REF.	
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
θ1	0°	-	8°
θ2		12 REF.	
θ3		12 REF.	

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Controlling Dimension: Millimeters
3. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per end.
4. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
5. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
6. N is the maximum number of terminal positions for the specified package length. Depopulation is allowed, but only under the following conditions:
   - Depopulation may reduce N by increments of four leads only.
   - Only end leads may be removed.
   - Leads must be symmetrically arranged with respect to datum A (Note 10) to avoid any array shifting.
7. Terminal numbers are shown for reference only.
8. Datum A and B to be determined at datum plane H.
9. Dimensions D and E1 to be determined at datum plane H.
10. This dimension applies only to variations with an even number of leads per side. For variations with an odd number of leads per side, the center lead must be coincident with the package centerline, datum A.
11. Cross section B-B to be determined at 0.10 to 0.25 mm from the lead tip.
12. Details of the pin 1 identifier are optional, but must be located within the zone indicated.
13. D1 and E2 minimum dimensions of thermally enhanced types are variables depending on device function (die paddle size). D1 and E2 maximum dimensions can be equal to D/E1 maximum dimensions. End user should verify actual size of exposed thermal pad for specific device application.
14. A1 is defined as the vertical distance from the seating plane to the lowest point on the package body excluding the lid and or thermal enhancement on cavity down package configurations.
15. Caution should be taken during design, assembly and processing to prevent deposited board solder from holding the leads up off the board. This is applicable to thermal enhanced variations where A1 dimension is allowed to be zero.
16. Refer to JEDEC MO-153 Variation AC

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