



DESCRIPTION

PT2312 is a four-channel digital control audio processor utilizing CMOS Technology. Volume, Bass, Balance, Front/Rear Fader Processor, Selectable Input Gain are incorporated into a single chip having the highest performance and reliability with the least external components. All functions are programmable using the I²C Bus. PT2312 is housed in 32-pin, SOP Package. 4 stereo inputs with selectable input gain, 2-band tone control (treble & bass), balance, fader and loudness function are incorporated into a single chip having the highest performance and reliability. Pin assignments and application circuits are optimized for easy PCB layout and cost saving advantages.

FEATURES

- CMOS technology
- Least external components
- Treble and Bass control
- Loudness function
- 4 stereo inputs with selectable input gain
- Input/output for external noise reduction system/equalizer
- 4 independent speaker controls for Fader and Balance
- Independent mute function
- Volume control in 1.25dB/step
- Low distortion
- Low noise and DC stepping
- Controlled by I²C bus micro-processor interface
- Available in 32 pins, SOP package

APPLICATIONS

- Car stereo (Audio)
- Hi-Fi audio system
- LCD monitor

Note:

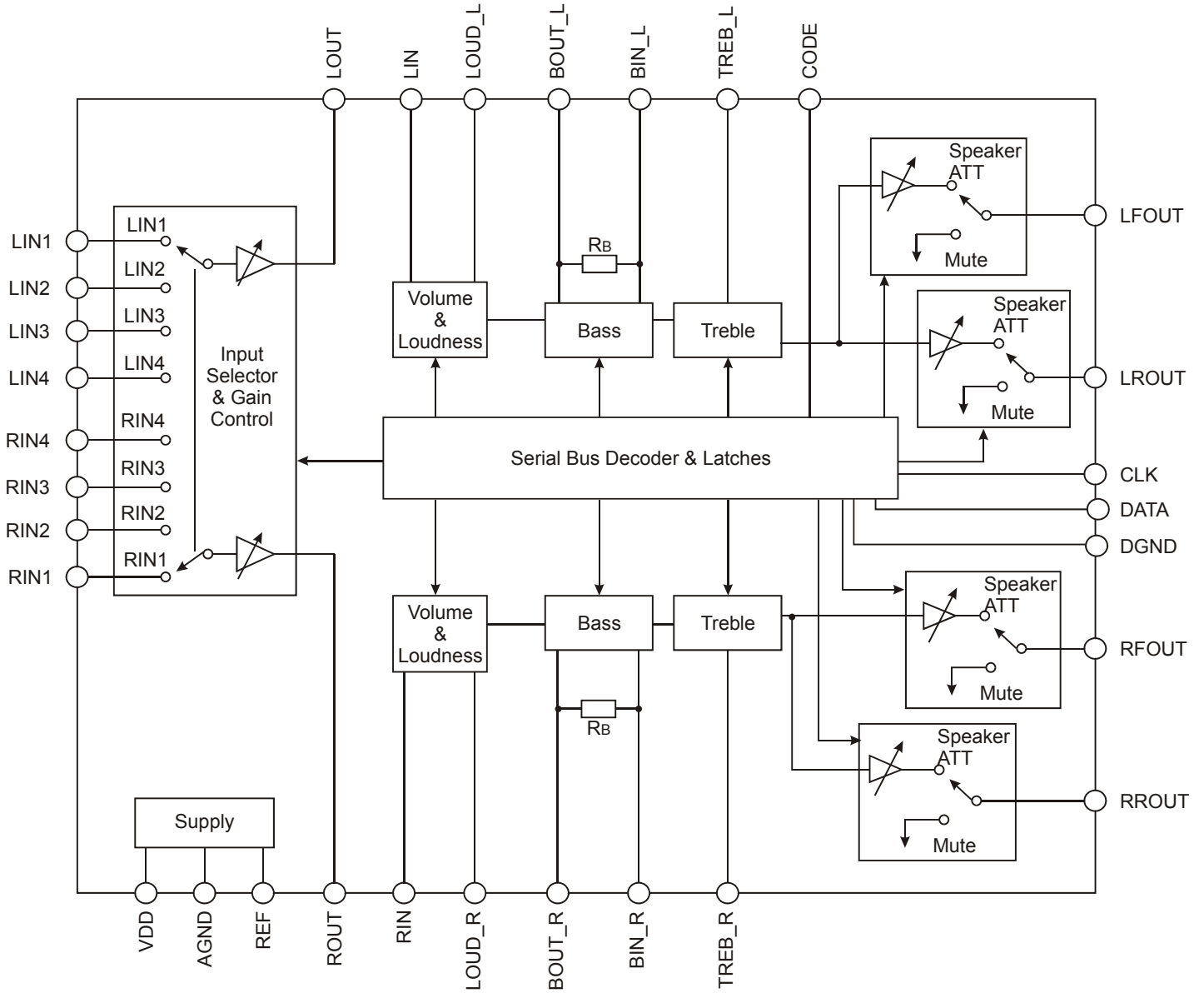
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4 Channel Audio Processor

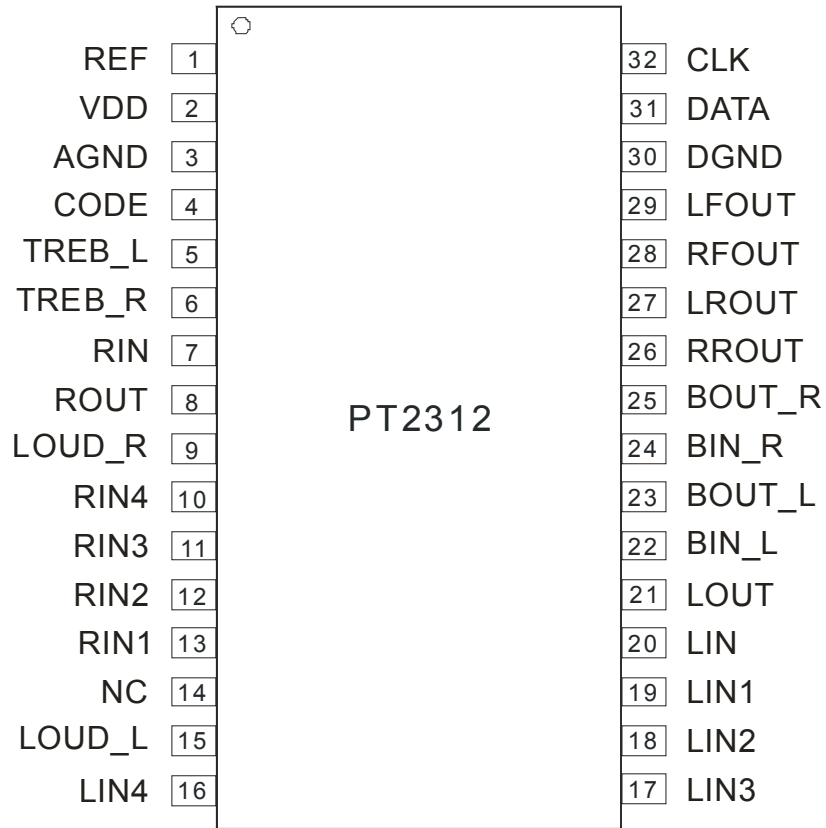
PT2312

BLOCK DIAGRAM





PIN CONFIGURATION





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PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
REF	-	Analog Reference Voltage (1/2VDD)	1
VDD	-	Supply Input Voltage	2
AGND	-	Analog Ground	3
CODE	I	Address Select Pin This pin must always be Pull-High.	4
TREB_L	I	Left Channel Input for Treble Controller	5
TREB_R	I	Right Channel Input for Treble Controller	6
RIN	I	Audio processor Right Channel Input	7
ROUT	O	Gain Output and Input Selector for Right Channel	8
LOUD_R	I	Right Channel Loudness Input	9
RIN4	I	Right Channel Input 4	10
RIN3	I	Right Channel Input 3	11
RIN2	I	Right Channel Input 2	12
RIN1	I	Right Channel Input 1	13
NC	-	No Connection	14
LOUD_L	I	Left Channel Loudness Input	15
LIN4	I	Left Channel Input 4	16
LIN3	I	Left Channel Input 3	17
LIN2	I	Left Channel Input 2	18
LIN1	I	Left Channel Input 1	19
LIN	I	Audio Processor Left Channel Input	20
LOUT	O	Gain Output and Input Selector for Left Channel	21
BIN_L	I	Left Channel Input for Bass Controller	22
BOUT_L	O	Left Channel Output for Bass Controller	23
BIN_R	I	Right Channel Input for Bass Controller	24
BOUT_R	O	Right Channel Output for Bass Controller	25
RROUT	O	Right Rear Speaker Output	26
LROUT	O	Left Rear Speaker Output	27
RFOUT	O	Right Front Speaker Output	28
LFOUT	O	Left Front Speaker Output	29
DGND	-	Digital Ground	30
DATA	I	Control Data Input	31
CLK	I	Clock Input for Serial Data Transmission	32



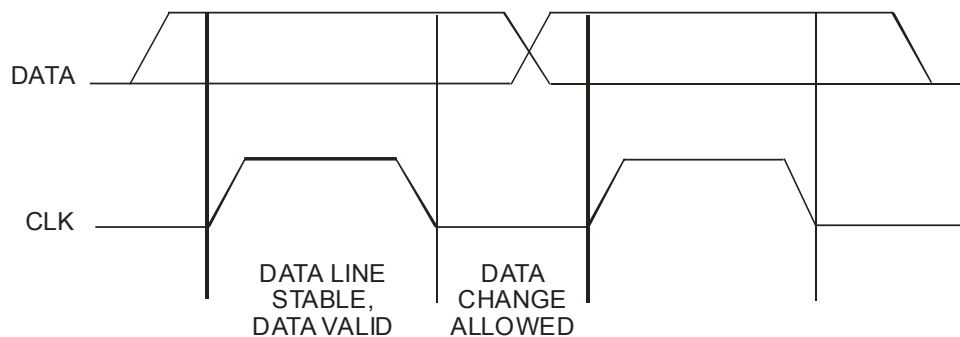
FUNCTION DESCRIPTION

BUS INTERFACE

Data are transmitted to and from the microprocessor to the PT2312 via the DATA and CLK. The DATA and CLK make up the BUS Interface. It should be noted that the pull-up resistors must be connected to the positive supply voltage.

DATA VALIDITY

A data on the DATA Line is considered valid and stable only when the CLK Signal is in HIGH State. The HIGH and LOW States of the DATA Line can only change when the CLK signal is LOW. Please refer to the figure below.



START AND STOP CONDITIONS

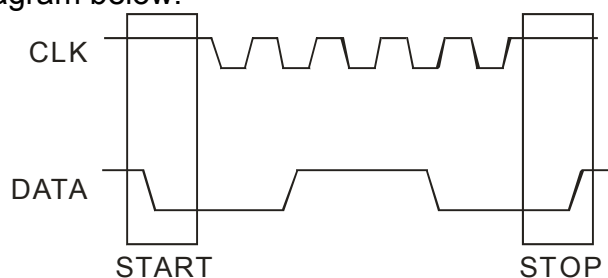
A Start Condition is activated when

1. the CLK is set to HIGH and
2. DATA shifts from HIGH to LOW State.

The Stop Condition is activated when

1. CLK is set to HIGH and
2. DATA shifts from LOW to HIGH State.

Please refer to the timing diagram below.



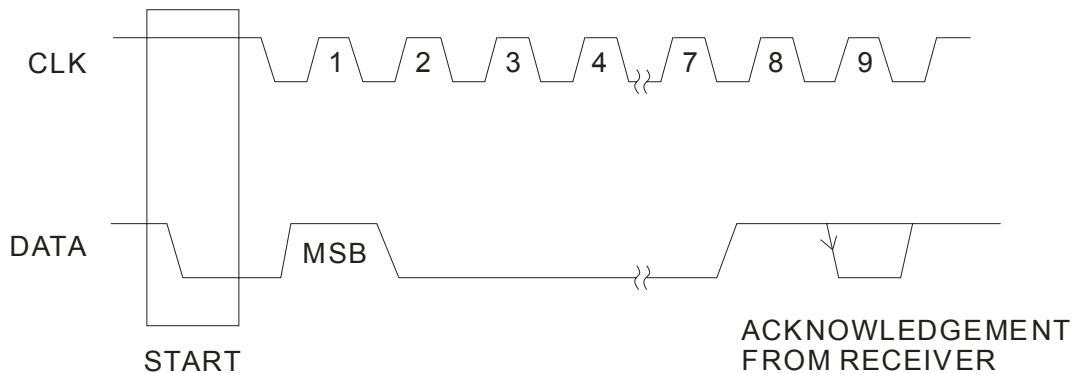


BYTE FORMAT

Every byte transmitted to the DATA Line consists of 8 bits. Each byte must be followed by an Acknowledge Bit. The MSB is transmitted first.

ACKNOWLEDGE

During the Acknowledge Clock Pulse, the master (μ P) puts a resistive HIGH level on the DATA Line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the DATA line during the Acknowledge Clock Pulse so that the DATA Line is in a Stable Low State during this Clock Pulse. Please refer to the diagram below.



The audio processor that has been addressed has to generate an Acknowledge after receiving each byte, otherwise, the DATA Line will remain at the High Level during the ninth (9th) Clock Pulse. In this case, the master transmitter can generate the STOP Information in order to abort the transfer.

TRANSMISSION WITHOUT ACKNOWLEDGE

If you want to avoid the acknowledge detection of the audio processor, a simpler μ P transmission may be used. Wait one clock and do not check the slave acknowledge of this same clock then send the new data. If you use this approach, there are greater chances of faulty operation as well as decrease in noise immunity.



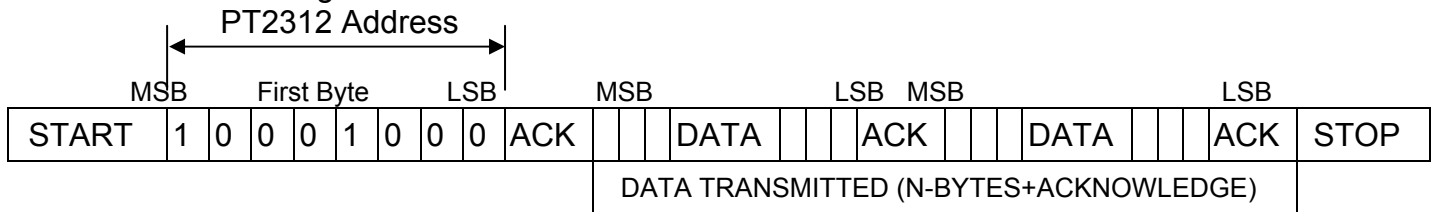
4 Channel Audio Processor **PT2312**

INTERFACE PROTOCOL

The interface protocol consists of the following:

- A Start Condition
- A Chip Address Byte including the PT2312 address. The 8th Bit of the Byte must be "0". PT2312 must always acknowledge the end of each transmitted byte.
- A Data Sequence (N-Bytes + Acknowledge)
- A Stop Condition

Please refer to the diagram below:



Notes:

1. ACK=Acknowledge
2. Max. Clock Speed=100K BITS/S



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SOFTWARE SPECIFICATION

PT2312 ADDRESS

PT2312 Address is shown below.

1	0	0	0	1	0	0	0
MSB							LSB

DATA BYTES

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	1	0	B1	B0	A2	A1	A0	Speaker ATT LR
1	1	1	B1	B0	A2	A1	A0	Speaker ATT RR
1	0	0	B1	B0	A2	A1	A0	Speaker ATT LF
1	0	1	B1	B0	A2	A1	A0	Speaker ATT RF
0	1	0	G1	G0	S2	S1	S0	Audio Switch
0	1	1	0	C3	C2	C1	C0	Bass Control
0	1	1	1	C3	C2	C1	C0	Treble Control

where: Ax=1.25dB steps; Bx=10dB steps; Cx=2dB steps; Gx=3.75dB/steps

VOLUME

The table below gives a detailed description of the Volume Data Bytes. For example, a volume of -37.5 dB is given by 0 0 0 1 1 1 1 0.

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume 1.25dB steps
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
0	0	B2	B1	B0	A2	A1	A0	Volume 10dB steps
		0	0	0				0
		0	0	1				-10
		0	1	0				-20
		0	1	1				-30
		1	0	0				-40
		1	0	1				-50
		1	1	0				-60
		1	1	1				-70



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SPEAKER ATTENUATORS

The table below gives a detailed description of the speaker attenuators data bytes. For example, an attenuation of 30dB on the Speaker IF (Right Front) is given by: 10111000.

MSB							LSB	Function
1	0	0	B1	B0	A2	A1	A0	Speaker LF
1	0	1	B1	B0	A2	A1	A0	Speaker RF
1	1	0	B1	B0	A2	A1	A0	Speaker LR
1	1	1	B1	B0	A2	A1	A0	Speaker RR
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
			0	0				0
			0	1				-10
			1	0				-20
			1	1				-30
			1	1	1	1	1	Mute

AUDIO SWITCH DATA BYTE

The following table shows the detailed description of the Audio Switch Data Bytes. For example, a Stereo 1 Input with Gain of +11.25dB Loudness ON is given by: 01000000.

MSB							LSB	Function
0	1	0	G1	G0	S2	S1	S0	Audio Switch
						0	0	Stereo 1
						0	1	Stereo 2
						1	0	Stereo 3
						1	1	Stereo 4
					0			Loudness ON
					1			Loudness OFF
			0	0				+11.25dB
			0	1				+7.5dB
			1	0				+3.75dB
			1	1				0dB



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BASS AND TREBLE DATA BYTES

The following table shows a detailed description of the Bass and Treble Data Byte. For example a Treble at -12dB is given by: 01110001.

MSB							LSB	Function
0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treble
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14

Unit: dB



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Operating supply voltage	Vs	10.5	V
Operating temperature	Topr	-40 to 85	°C
Storage temperature	Tstg	-65 to +150	°C

QUICK REFERENCE DATA

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vs	6	9	10	V
Max. input signal handling	VCL	2	2.5		Vrms
Total harmonic distortion (V=1Vrms, f=1KHz)	THD		0.07	0.15	%
Signal to noise ratio	S/N		95		dB
Channel separation (f=1KHz)	Sc		85		dB
Volume control 1.25dB step		-75		0	dB
Bass & treble control 2dB step		-14		+14	dB
Fader & balance control 1.25dB step		-37.5		0	dB
Input gain 3.75dB step	GIN	0		16	dB
Mute attenuation	AMUTE		75		dB



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ELECTRICAL CHARACTERISTICS

(Unless otherwise specified: Ta=25°C, Vc=9V, RL=10KΩ, Rg=600Ω, all controls flat (G=0), f=1KHz)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Supply						
Supply voltage	Vcc		6	9	10	V
Supply current	Is			30	40	mA
Input Selectors						
Input resistance	RII	Input 1, 2, 3	80	100	120	KΩ
Clipping level	VCL	Av=-8.75 dB; d=0.3%	2	2.5		Vrms
Input separation (2)	SIN		80	100		dB
Min. input gain	GINmin		-1	0	1	dB
Max. input gain	GINmax			11.25		dB
Volume Control						
Input resistance	RIV		30	40	50	KΩ
Control range	CRANGE		65	70	75	dB
Min. attenuation	AVMIN		-1	0	1	dB
Max. attenuation	AVMAX		65	70	75	dB
Step resolution	ASTEP		0.5	1.25	1.75	dB
Attenuation set error	EA	AV=0 to -20dB AV=-20 to -60dB	-1.25 -3.0	0	1.25 2	dB dB
Speaker Attenuators						
Control range	CRANGE		35	37.5	40	dB
Step resolution	SSTEP		0.5	1.25	1.75	dB
Attenuation set error	EA				1.5	dB
Output mute attenuation	AMUTE		70	75		dB
Bass Control (1)						
Control range	Gb	Max. Boost/Cut	±12	±14	±16	dB
Step resolution	BSTEP		1	2	3	dB
Internal feedback resistance	RB		34	44	58	KΩ
Treble Control (1)						
Control range	Gt	Max. Boost/Cut	±13	±14	±15	dB
Step resolution	TSTEP		1	2	3	dB
Audio Outputs						
Clipping level	VOCL	d=0.3%	2	2.5		Vrms
Output resistance	ROUT		-	40	45	Ω
DC voltage level	VOUT		4.2	4.5	4.8	V



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Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
General						
Output noise	eNO	BW=20~20KHz, Flat Output Muted All gains=0dB		-97 -92		dB dB
		A Curve All Gains=0dB		-100		dB
Signal to noise ratio	S/N	All Gains=0dB Vo=1Vrms		95		dB
Distortion	d	AV=0, VIN=1Vrms		0.1	0.3	%
		AV=-8.75dB, VIN=1Vrms,		0.07	0.15	%
		AV=-8.75dB, VIN=0.3Vrms		0.03	0.1	%
Channel separation left/right	Sc		80	90		dB
Bus Inputs						
Input low voltage	VIL				1	V
Input high voltage	VIH		3			V
Input current	IIN		-5		+5	μA
Output voltage SDA acknowledge	Vo	Io=1.6mA			0.4	V

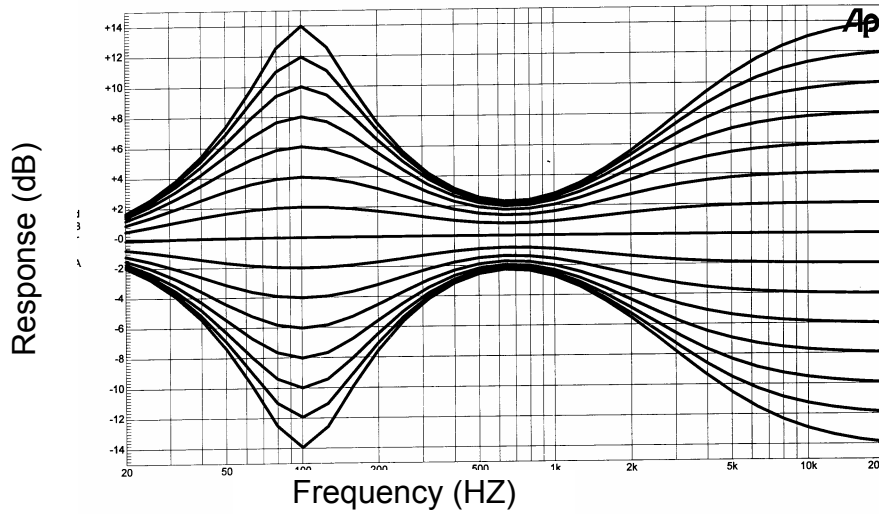
Notes:

1. For the Bass and Treble Response, please, refer to the diagram below. The center frequency and quality of the resonance behavior can be selected by the external circuitry. A standard first order bass response can realized by a standard feedback network.
2. The selected input is grounded thru the 2.2μF capacitor.

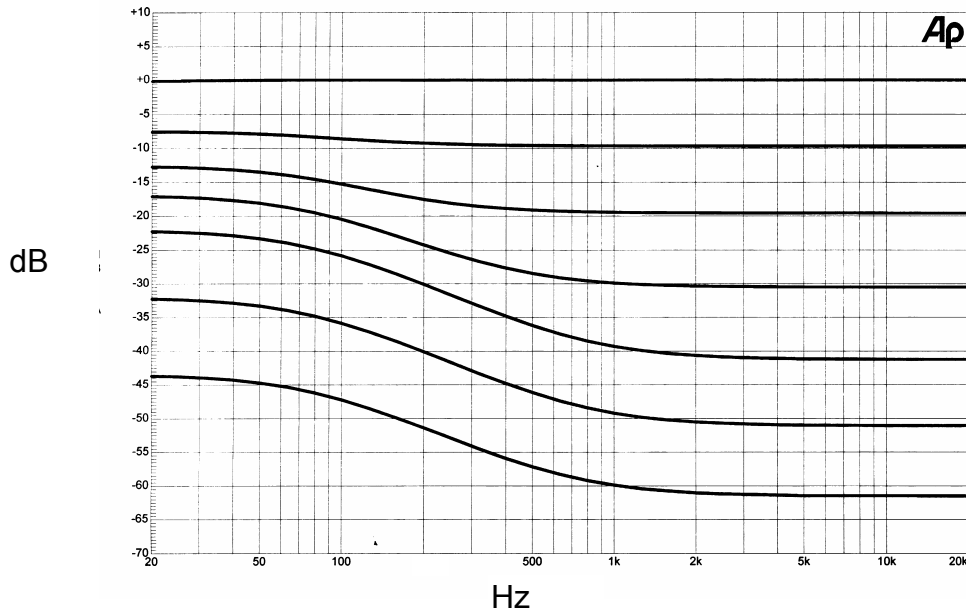


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Typical Tone Response (with the ext. Components indicated in the test circuit)

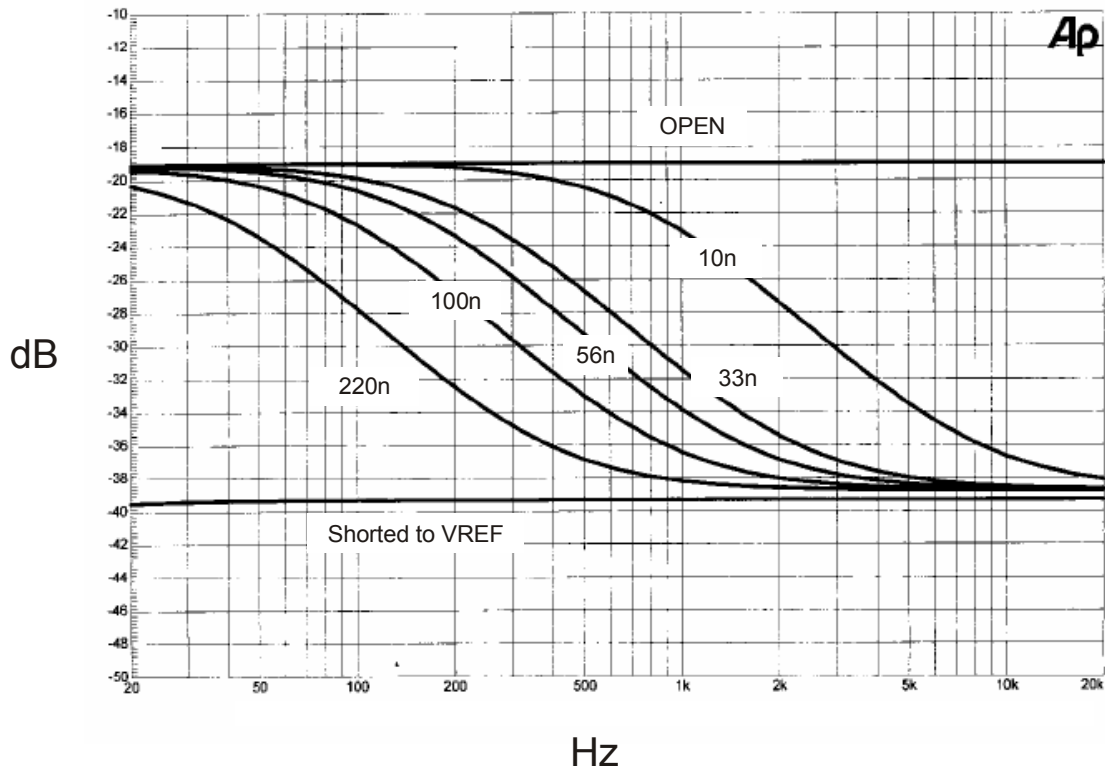


PT2312: Loudness vs. Volume Attenuation Frequency Response (C10=C11=100nF)



4 Channel Audio Processor

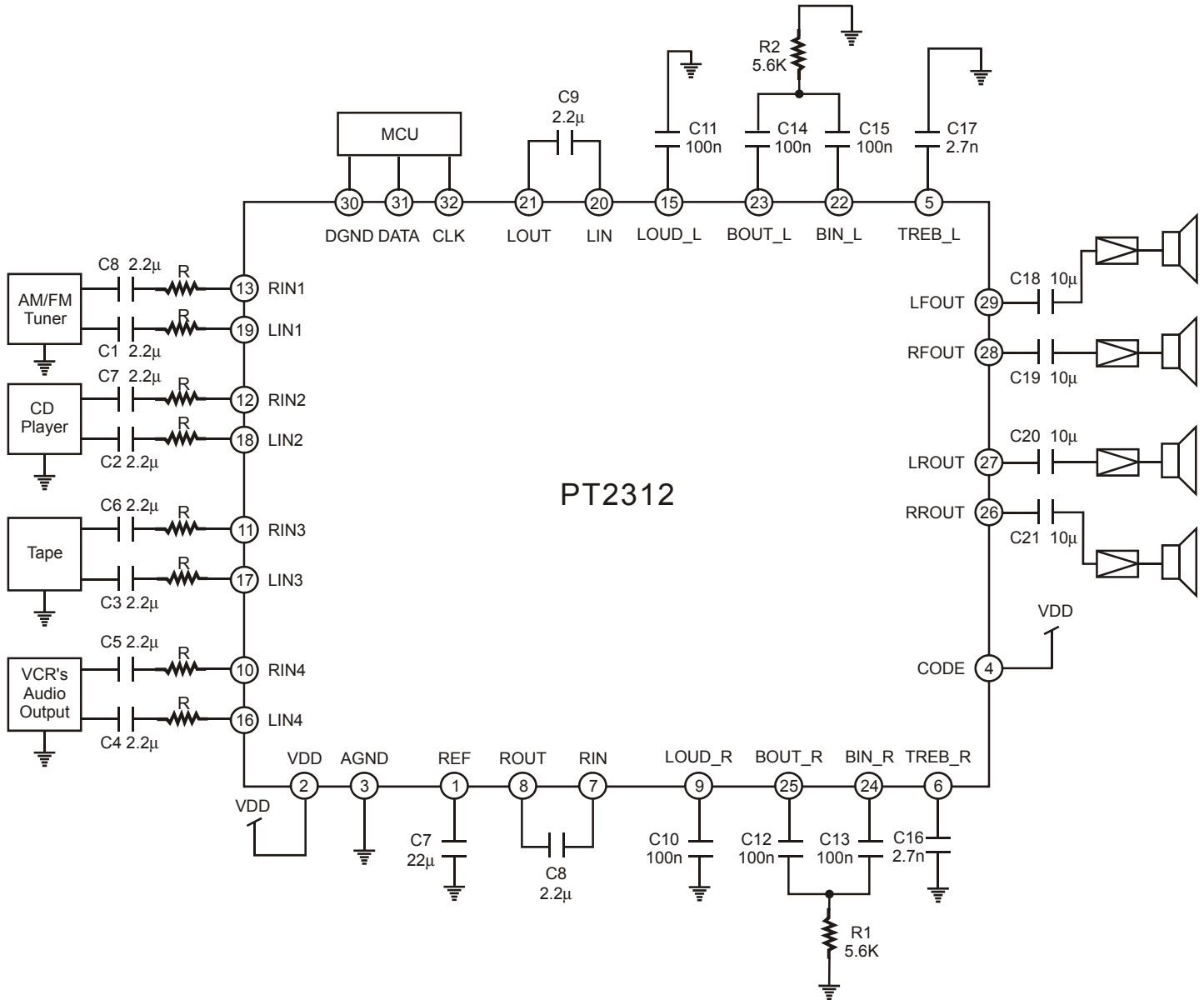
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PT2312: C10, C11 vs Loudness Frequency Response (Volume=-40dB, All other controls are flat)



APPLICATION CIRCUIT





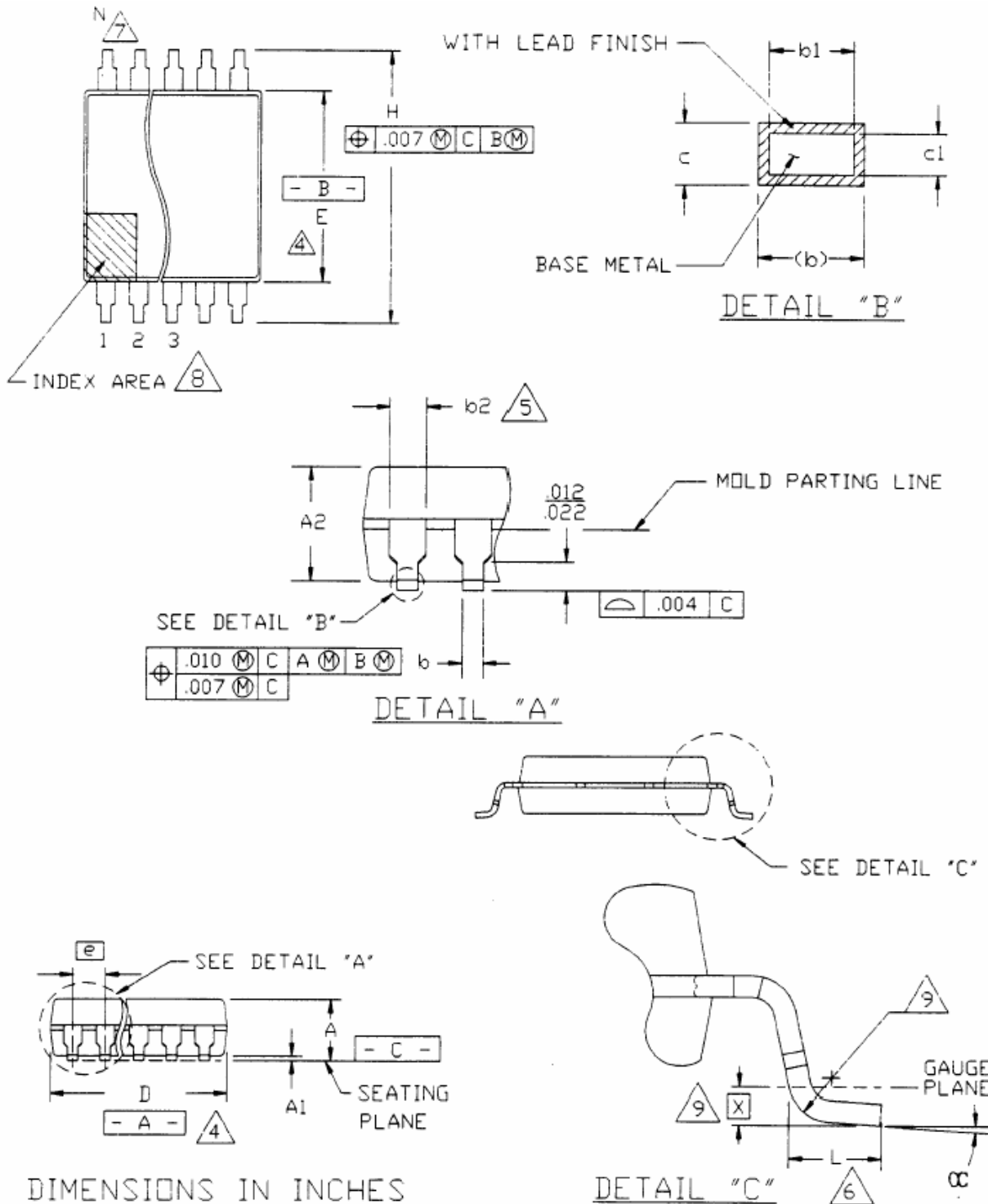
ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2312	32 Pins, SOP, 300mil	PT2312



PACKAGE INFORMATION

32 PINS, SOP, 300MIL





4 Channel Audio Processor

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Symbols	Min.	Nom.	Max.
A	-	-	0.104
A1	0.004	-	-
A2	0.082	0.088	0.094
b	0.014	0.016	0.020
b1	0.014	0.016	0.018
b2	0.026	0.028	0.032
c	0.007	0.008	0.0125
c1	0.007	0.008	0.010
D	0.812	0.818	0.824
E	0.292	0.296	0.299
e	0.050 BSC.		
H	0.405	0.412	0.419
L	0.021	0.031	0.041
α	0°	4°	8°

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5-1982.
2. Dimension D does not include mold flash, protrusions or gate burrs. Mold Flash, protrusion or gate burrs shall not exceed 0.15mm (0.006 in) per side.
3. Dimension E does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. The chamfer on the body is optional. It is not present, a visual index feature must be located within the crosshatched area.
5. L is the length of the terminal for soldering to a substrate.
6. The lead width B as measured 0.36 mm (0.014 in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.24 in)
7. Controlling dimension: Inch
8. N=Number of terminal position (N=32)
9. Refer to JEDEC MO-119 variation AC.

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